



NXP Aero dual-band W-CDMA RF frequency synthesizer AERO4133*

Low-power RF synthesizer for W-CDMA in an 85% smaller footprint with reduced overall cost

This highly integrated circuit improves power efficiency and isolation, eliminates external interference, and, because it integrates VCOs, loop filters, and varactor diodes, significantly reduces external passive chip-count.

Key features

- ▶ Dual-band RF synthesizer
 - RF1 VCO range = 2.3 to 2.6 GHz
 - RF2 VCO range = 750 MHz to 1.5 GHz
- ▶ IF synthesizer
 - IF output range = 62.5 MHz to 1.0 GHz
- ▶ Fully integrated VCOs
- ▶ Programmable loop filters
- ▶ Programmable power-down modes
- ▶ Only two external passive components
- ▶ Automatic selection of optimal phase-detector gain and modulus-prescaler values
- ▶ Low phase noise
- ▶ Fast settling times: 200 μ S for GSM applications
- ▶ Standby current at 3 V = 5 μ A
- ▶ Supply current at 3 V = 18 mA
- ▶ Operation: 2.9 to 3.6 V
- ▶ Process technology: 0.35- μ m CMOS
- ▶ 28-lead MLP package

* Formerly available as the Si4133W from Silicon Labs

Applications

- ▶ 3G wireless communications
- ▶ UMTS/W-CDMA mobile handsets
- ▶ High-speed wireless data terminals
- ▶ Broadband wireless communications

The NXP Aero dual-band W-CDMA RF frequency synthesizer AERO4133 performs IF and dual-band, low-noise RF frequency synthesis with very low power consumption and in a footprint that is 75% smaller than competing solutions. It is available in versions optimized for GSM/GPRS and W-CDMA.

Very high integration serves to reduce external component count and shrink the design footprint. It includes three voltage-controlled oscillators (VCOs), loop filters, reference and VCO dividers, and phase detectors.

A three-wire serial interface (Data, Clock, Enable) and a 22-bit internal shift register serve to simplify system configuration and design. Channel selection and power-down settings are programmable, as are variables for dividers and settings for phase-detector gains.

Featuring fast settling times, the AERO4133 signal output stabilizes to an accuracy of 0.1 ppm frequency error in 200 μ sec, and thereby meets the requirements of compressed mode in W-CDMA.

The unprecedented level of integration can reduce board space by as much as 85% over conventional frequency-synthesizer architectures that use a dual-band synthesizer IC, external VCOs, varactor diodes, and up to 35 additional passive components. Designers can also realize a cost savings of 33% over conventional solutions.

The robustness and consistency of an integrated solution makes manufacturing easier and lowers the cost of assembly and test for high-volume applications.

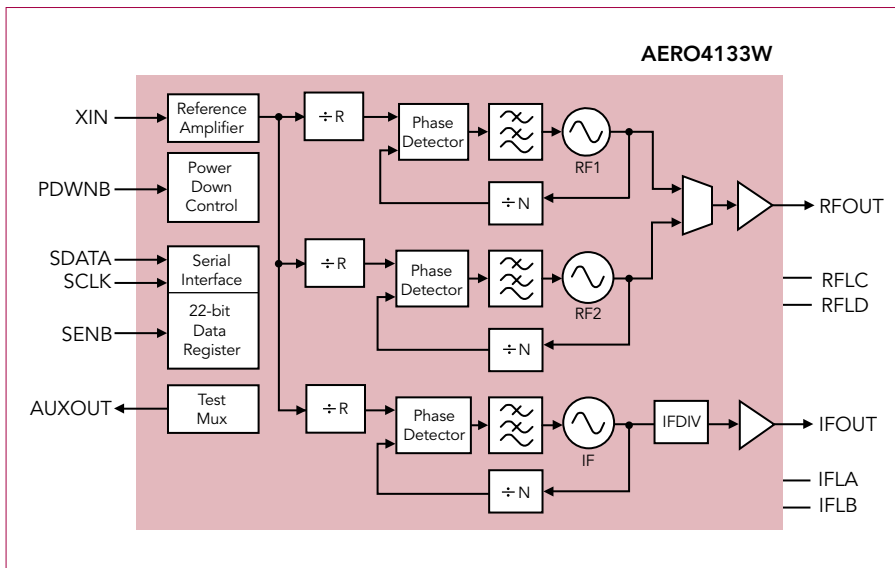
The synthesizer uses a proprietary, self-calibrating architecture that not only results in fast settling times, but also significantly reduces power consumption in the phase-lock loop (PLL).

That, in combination with the flexible power-down scheme, provides the lowest overall power consumption in RF synthesizer applications.

Integrating all the components of the frequency-synthesis function into a monolithic CMOS device gives the designer greater control of the power consumption of the entire function block, since there is a single control interface.

Reducing the number of components simplifies the local oscillator (LO) design of the W-CDMA radio, and accelerates time-to-market. RF designers no longer need to optimize hardware-based loop filters to satisfy the requirements for phase noise or settling time – all they do is program the desired settings via software control to configure the AERO4133.

The synthesizer comes standard in a low-profile, 28-lead micro leadframe (MLP) package, and is available with an evaluation board, user-friendly software, and other development tools.



AERO4133 block diagram

NXP part no.	Standard	IF output	RF1 output	RF2 output
AERO4133	W-CDMA	62.5 MHz to 1.0 GHz	2.3 to 2.6 GHz	750 MHz to 1.7 GHz

AERO4133 ordering information

www.nxp.com



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