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## **Turning consumer electronics green**

*Achieving low power consumption in future consumer electronics devices*

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It's an accepted fact that human activity is changing the world's climate. Greenhouse gas emissions, global warming and rising sea levels and all hot topics in the media and the subject of global summits. In most countries, electricity generation accounts for a significant proportion of greenhouse gas emissions. As a result, reducing electrical energy consumption is seen as an important factor in combating global warming. Studies have shown that around 4% of the world's electricity generation is used to power consumer electronics devices. In the USA alone, this amounted to 147 TWh (Terrawatt.hours) in 2006, equivalent to the output of several large-scale nuclear power plants.

In the past, energy consumption in CE devices was always regarded as less important than the energy used for heating/cooling and lighting, except of course for mobile devices where battery lifetime is critical. However, with world-wide initiatives already underway to produce 'zero carbon footprint' buildings and shift people over to using energy efficient lighting, the contribution of all types of CE device to energy consumption is becoming increasingly significant. As a result, limitations on the power consumption of CE devices are beginning to enter into regulatory requirements and guidelines. There is also growing public awareness of energy efficiency issues, which means that low-power consumption can be successfully marketed as a product feature.

Of the most common CE devices, televisions consume more energy than any other single product category, with computers coming a close second. However, other ubiquitous devices such as set-top-boxes, VCRs and PVRs also consume considerable amounts. What is even more worrying is that less than 50% of the energy used by these devices is typically consumed while they are carrying out their primary function. Over 50% is consumed while they are in idle or standby modes. Equally significant amounts are consumed by the power-plug chargers that come with equipment such as mobile phones and personal media players, which are often left plugged in even when they are not connected to the devices they are designed to power.

Achieving low power consumption therefore requires a system-level approach that addresses power consumption both at chip level and system level. With so many of today's consumer devices hooked into networks such as in-home digital networks or the Internet, power saving may even need to be considered at network level.

## **Chip-level considerations**

The dynamic power consumption of CMOS digital chips is approximated by the equation:

$$P_{\text{dynamic}} \propto CV^2f$$

Where  $C$  = switched capacitance  
 $V$  = voltage  
 $f$  = switching frequency

Because the capacitance and chip area for a given number of gates are fixed by the CMOS process/library technology, dynamic power dissipation can only be reduced by reducing the clock frequency, the supply voltage ( $V_{\text{dd}}$ ), or a combination of both. In addition, supply voltage and clock frequency are interdependent, with higher  $V_{\text{dd}}$  values being required to sustain higher clock frequencies.

Because of its simplicity and ease of implementation, dynamic frequency switching in the form of clock gating (reducing the clock frequency to zero) has been used for some time to reduce dynamic power dissipation in areas of a chip that are temporarily idle. However, this crude on-off control does nothing to save power consumption once these areas of the chip once again become active.

An alternative approach, which addresses active as well as idle-state power consumption, is dynamic frequency scaling. This technique progressively reduces the chip's clock frequency as the computational load on its processing resources falls, the selected frequencies being chosen such that computational tasks still complete within real-time constraints of the application.

Dynamically scaling the clock to lower frequencies also opens up the possibility of saving additional power by reducing the supply voltage. Dynamic power consumption is directly proportional to the clock frequency but proportional to the square of the supply voltage. As a result, even small reductions in supply voltage can have a significant effect.

This ability to reduce the clock frequency to parts of the chip and run those parts at reduced supply voltage is already beginning to be exploited in NXP SoCs. It is being done in the form of 'voltage islands', in which nearby IP blocks with a common maximum clock frequency are grouped together and powered from a separate  $V_{\text{dd}}$  supply (Figure 1a)

In current SoCs that employ voltage islands, each island typically operates at a fixed  $V_{\text{dd}}$  voltage. However, the existence of these voltage islands also opens up the possibility of applying another technique, called Dynamic Voltage and Frequency Scaling (DVFS) to further reduce power consumption. DVFS adds voltage scaling on top of frequency scaling to automatically adjust each island's  $V_{\text{dd}}$  to the lowest possible voltage needed to sustain its selected clock speed (Figure 1b).

DVFS can be implemented either as an open-loop or closed-loop process. In open-loop DVFS, several discrete frequency and voltage operating points are defined for the target system, and the system is set to the nearest operating point that guarantees the required processing performance (see Figure 2a). In practice the number of different operating points is typically limited to between 2 and 4, each of which must guarantee performance under specific processor loading, also taking into account worst-case process variations (variation in system performance due to process technology variations) and operating temperatures. However, because open-loop DVFS has to make decisions based on worst-case process variations and operating temperatures, this means that in many cases the supply voltage may still have to be set somewhat high.

Closed-loop DVFS overcomes the problem by providing direct feedback on actual silicon performance in the system. To do so it incorporates a performance monitor within each DVFS domain that measures the domain's actual clock-speed capability at any point in time. The output of this performance monitor passes information to a voltage regulator that adjusts the domain's  $V_{dd}$  voltage to the minimum level needed to meet the performance requirements of the silicon under actual conditions (see Figure 2b).

Another technique that has been proposed for use in combination with DVFS to optimize performance and power consumption is body biasing – controlling a CMOS transistor's body potential to alter its threshold voltage and hence adjust its switching performance. This technique has the potential advantages of being able to improve both dynamic and static power dissipation (the transistors can be forced more fully off) and can also be used to improve production yields by compensating for process technology variations that would render a conventional SoC out-of-specification.

However, body biasing significantly increases design complexity. In addition, it is unlikely that its benefits can be extended beyond 65-nm CMOS, making the associated research and development effort needed to perfect the technique questionable.

Static (standby) power consumption in deep sub-micron CMOS chips is dominated by leakage currents, which makes adjustment of  $V_{dd}$  and  $V_t$  (via back-biasing) the preferred ways of fine-tuning static power consumption in a SoC.

As with frequency switching, switching off the  $V_{dd}$  supply to areas of the chip that are not in use is the simplest form of adjustment and has the advantage of reducing static power consumption in these areas to zero. However, this inevitably leads to a loss of state in the de-powered logic blocks, which means that the power consumption saved by switching these components off has to be weighed against the additional power needed to save/restore their state on entry/exit from the standby condition.

## **System level considerations**

An increasingly important system-level aspect of consumer devices is the amount of software they rely on. As their operating systems become more complex, they may take several tens of seconds to boot up from mass storage, such as a hard disk, after being turned on. Because this is unacceptable to many consumers, such devices are often designed to never shut down. They merely switch into an idle or standby mode in which they maintain their state but continue to consume a significant amount of power.

One way of allowing such devices to enter a near zero-power shut-down mode whenever they are not in use is to give them an 'instant-on' capability. Ideally this would mean equipping them with high-speed non-volatile memory such as MRAM, FeRAM or Phase-Change Memory that can also be used as their main execution memory. However, this will only become practical when these memories are available at the right price points for consumer product applications.

In hard disk based devices such as PVRs, a partial solution can be obtained by using the hard disk to store/restore the state of the device rather than rebooting its operating system. This is typically the technique used to implement the hibernation mode of many PCs.

System-level requirements for instant-on devices will become even more complex as devices increasingly become wireless networked. When one device is turned on, it might require other devices in the system to turn on, for example, to act as media servers. However, if these remotely networked devices are powered down at the time, how can they be told to turn on? The solution may require the development of highly sensitive RF devices that can scavenge sufficient energy from an RF carrier to activate closure of a power connection.

Figure 1a

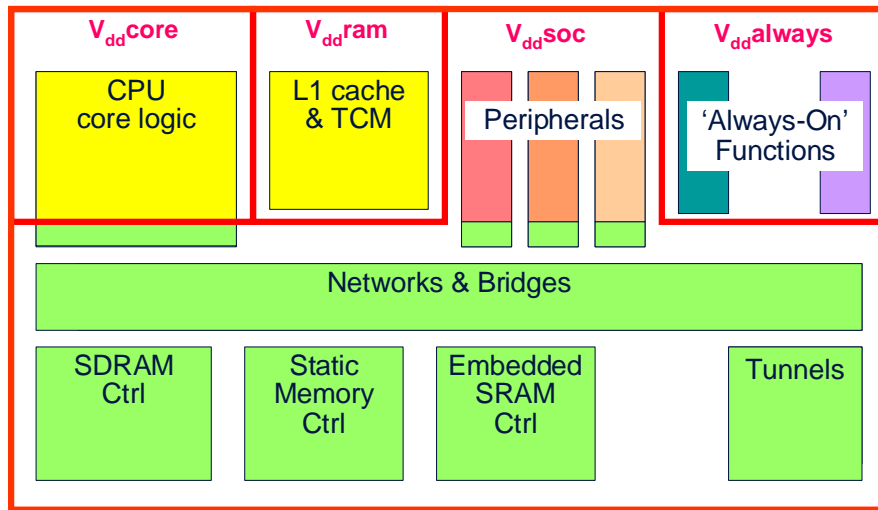


Figure 1b

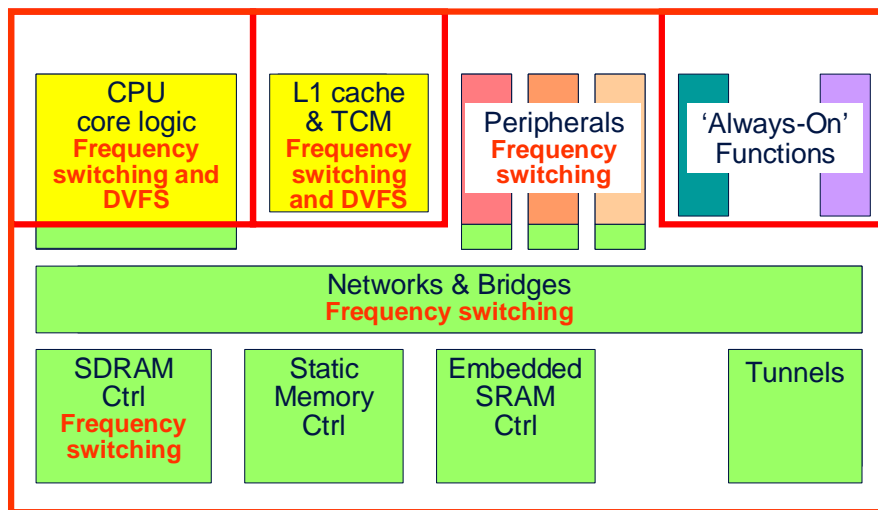


Figure 2a

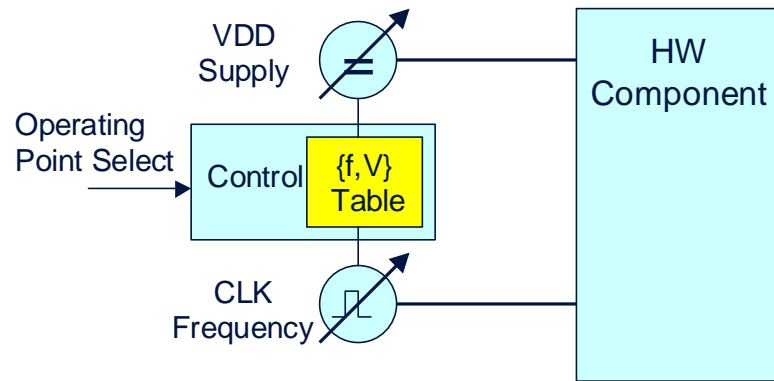


Figure 2b

