

IDEAS FOR DESIGN

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POWER/BATTERY SWITCHING USING VD-MOS FETS

A Power switch can be used to disconnect a load during a period of non use. The load may be anything from a light bulb, an electronic valve, a stepper or brush motor to electronic components in a lap top computer that is not in use all the time. There is a choice between a low-side switch (LSS) located between the load and the power supply return input, and a high-side switch (HSS), between the load and the power supply return. With an LSS the control is referenced to ground, whilst with an HSS the control is referenced to V_{DD} (see Fig.1). This makes the control for an HSS more complicated than for an LSS, and the design is more expensive and has a higher risk.

For power switching purposes MOSFETs have some important advantages over bipolar transistors. Firstly they are voltage controlled instead of current controlled, and secondly they have no thermal runaway or secondary breakdown. This is due to the fact that a MOSFET has a negative temperature coefficient of drain current, while a bipolar transistor has a positive temperature coefficient of collector current. Also the on-resistance of the FET can be reduced simply by connecting two or more in parallel.

Although more expensive, an HSS may perform better during fault conditions. The most probable fault that will

occur is a short from the output of the switch to ground. Since most environments are connected to ground, damage to the output wire of the switch may be sufficient for an output short to ground to cause the load to remain active. In the case of an HSS the short will be across the load, thus preventing its activation.

It is often required to control power switches from the output of digital logic. The most common logic families use levels of +2.4 V (TTL) or +5 V (CMOS). Figures 2 to 5 illustrate how to switch loads from these logic levels. In Fig.2 the 2.4 volt gate drive will fully turn on a MOSFET with a gate-source threshold voltage ($V_{GS_{th}}$) of less than 1.5 V. However, when using a FET with $V_{GS_{th}}$ of less than 3 V (see Fig.3), a gate pull-up resistor connected to +5 V is necessary to generate a full 5 volt swing from the TTL output. Using CMOS levels makes life easier. Since these levels equal the $V+$ and $V-$ values, a MOSFET is simply chosen with a $V_{GS_{th}}$ somewhere between $V+$ and $V-$. If the load is returned to ground, a P-channel FET is recommended (see Fig.4), or N-channel (see Fig.5) otherwise.

If the load is inductive, the use of a series gate resistor is recommended, as the drain-gate capacitance of the FET could couple inductive transients of the load back to the delicate logic circuitry.

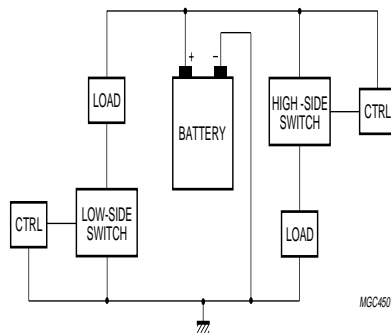
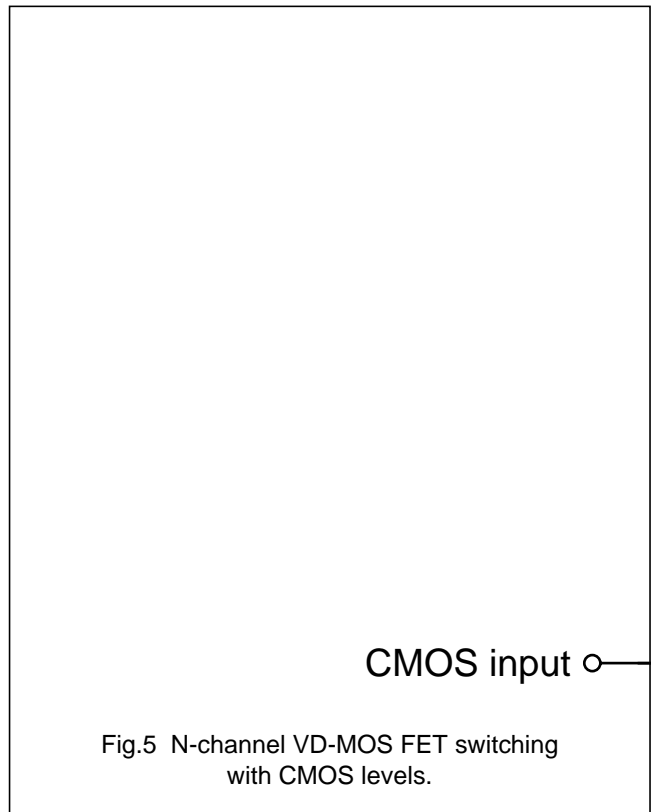
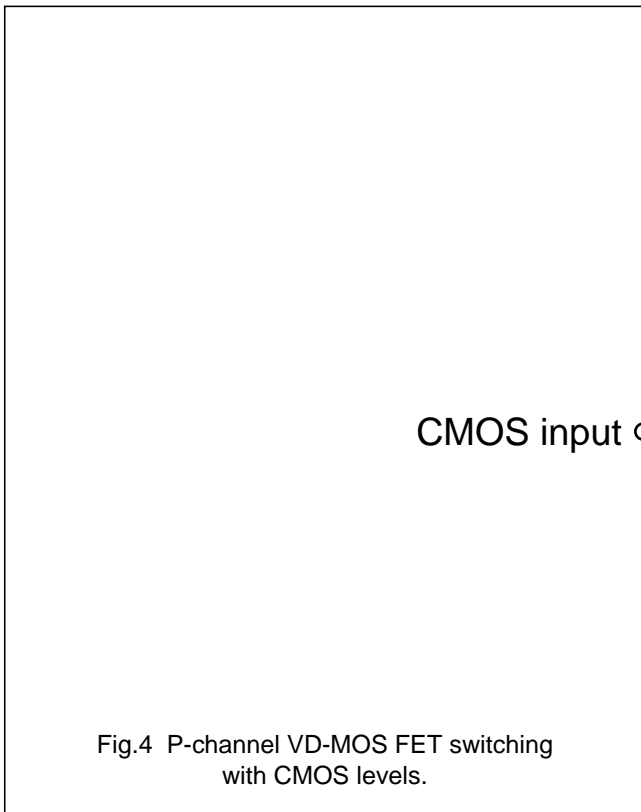
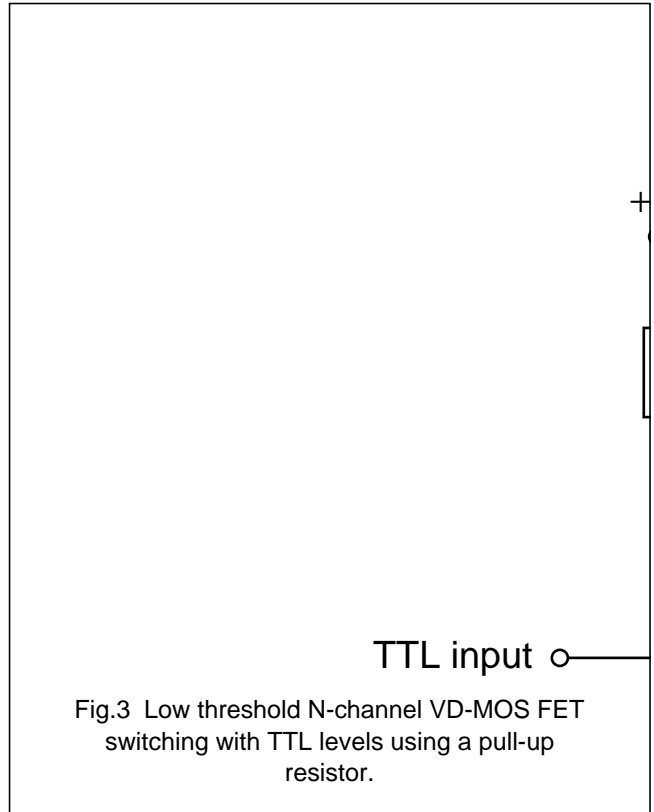
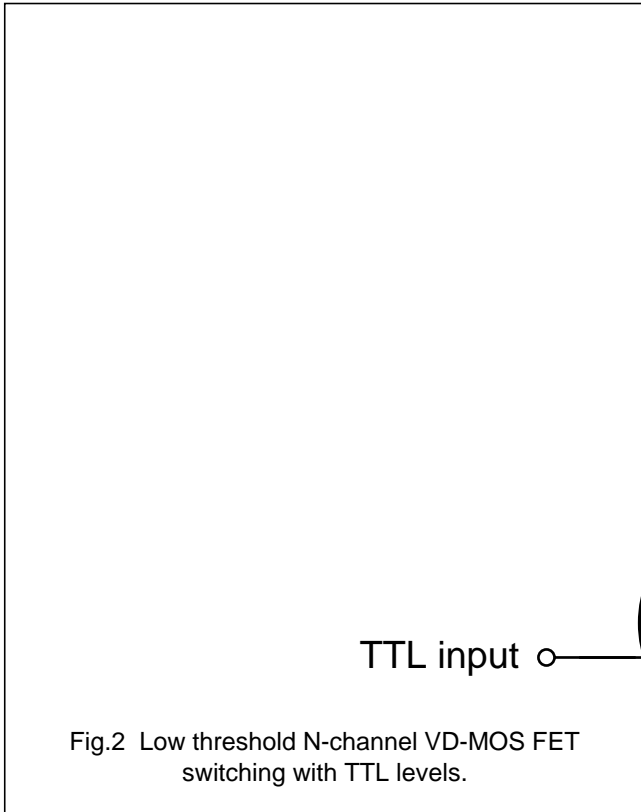


Fig.1 Power/Battery switching using VD-MOS FETs circuit diagram.

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DRIVERS FOR BRUSHLESS DC MOTORS

Brushless DC motors normally have a permanent magnet rotor and a wire-wound stator. They are very efficient and provide rapid acceleration, high speed, and smooth, quiet operation. The current to the stator coils is switched electronically as shown in Fig.6 and the switches are arranged in three half-bridge configurations to allow current flow in both directions.

In this example, the complementary P and N channel VD-MOS FETs are shown, but it is also possible to use only N channel switches, depending on the control circuitry. The PHILIPS Integrated Circuit TDA5142T has been chosen as the controller, and three of the PHC21025 MOSFETs (one 100 mΩ N-channel and one 250 mΩ P-channel type in a SO8 package) as motor drivers. These FETs can drive motors that require currents of up to 4 A (when soldering point temperature of drain pins does not exceed 80 °C) with gate drive coming directly from the IC.

A characteristic of inductive loads (such as stator windings) is the flyback energy that occurs when the drive current through a winding is switched off. This energy needs to be absorbed by the intrinsic source-drain diode of

the FET. The flyback current is equal to the motor current, which is at a maximum during acceleration and (active) braking. The flyback power is the product of both this current and the forward voltage drop over the diode, and of the duty cycle which in turn depends on the inductance of the windings. This dissipation is a substantial part of the total dissipation.

We can take a practical example and calculate the power dissipation of the intrinsic diodes during flyback, and the FETs when in the 'on' state.

Assume that we have a motor with 6000 rpm (100 rps) and 6 pole-pairs (600 'electrical' rps). The period time for one 'electrical revolution' is 1.667 ms. In each 'electrical revolution' all of the six FETs are switched, giving a switching frequency of 3600 Hz. A FET is therefore switching once every 278 μs, which is also the maximum time that the diode can be conducting. The FETs themselves are conducting at two periods, 278 μs and 556 μs, which is at a duty factor of 33%. The dissipation per half bridge (per SO8) is: $\{0.33 \times (I_{MOTOR})^2 \times R_{DSonP}\} + \{0.33 \times (I_{MOTOR})^2 \times R_{DSonN}\} + \text{flyback}_P + \text{flyback}_N$.

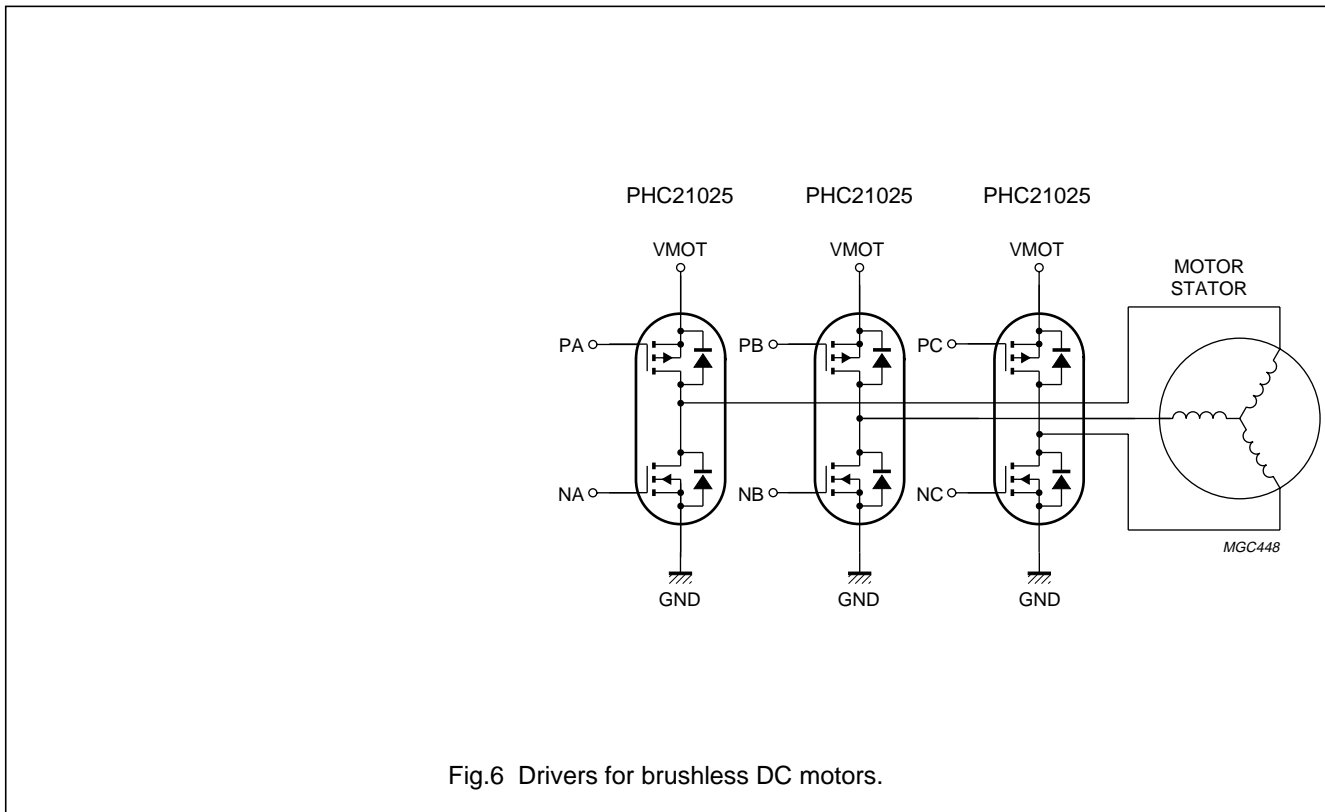


Fig.6 Drivers for brushless DC motors.

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To calculate the dissipation during flyback for this example, values of $2\ \Omega$ for the ohmic resistance of the windings, and $540\ \mu\text{H}$ for the inductance have been assumed. With a 12 V, 1 A motor, SPICE simulations show that the dissipation in the diode during flyback starts at 1.6 W at time zero, decreasing to 0 W after $60\ \mu\text{s}$. This is repeated every 1.667 ms and gives an average dissipation of 29 mW. The dissipation in the N-channel FET is 33 mW and in the P-channel FET 83 mW. This gives a total dissipation of 174 mW, of which 58 mW (33%) is in the diodes and cannot be neglected.

During acceleration and (active) braking, the motor current is much higher than during normal operation, and a current limiter may be necessary. The circuit design must be based on this higher current, because acceleration may last for up to a few seconds, long enough to heat up the FETs. During flyback, not only is the current much higher but it also lasts longer. In the simulation example, if the motor current is increased to 3 A, the flyback will last for $120\ \mu\text{s}$. The diode forward voltage will also be higher at this current level, and for one SO8 package the total dissipation increased to 1.5 W.

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USING THE PHN708 AND PHN405 IN HARD DISK DRIVES

Philips Semiconductors has introduced two low-ohmic VD-MOS FET arrays, which are primarily designed for use in hard disk drives. Together with the demand for ever increasing storage capacity and decreasing access times of hard disk drives, also the problems for the design engineers are increasing.

The table below shows what solution we offer for these problems.

For high- and mid-end drives, market developments show a clear trend of moving the power stages from inclusion onto the controller ICs to external discrete field effect transistors.

With the introduction of the two new VD-MOS FET arrays, Philips Semiconductors now offers a cost effective and highly integrated solution to the requirements for external power stages, using up to 35% less printed circuit board area compared with a solution using five or six SO8 packages.

The key feature in the design of these new arrays is that they contain seven (PHN708) or four (PHN405) separate pieces of silicon in one package.

PHN708 – power stage for spindle drive

The PHN708 is an array with seven N-channel FETs, with a maximum on-resistance of 80 mΩ for each FET, and is intended to drive a spindle motor. The maximum drain-source voltage is 30 V, so both 5 and 12 V motors can be used.

The FETs are configured as shown in Fig.7. Six of them form three half-bridges, needed to drive a three-phase brushless DC motor. The seventh is a so called 'isolation transistor', supplying the power to the half-bridges. This transistor can also be used for the break-function. This of course depends on the controller IC that is used. Together with Philips Semiconductors' TDA5149 combined spindle and voice coil motor controller, a complete solution for spindle-motor drives is provided. (See Fig.8.)

The PHN708 comes in a surface-mount SSOP24 package.

Table 1 Hard disk system design considerations

REQUIREMENT	IMPLEMENTATION	PROBLEM	SOLUTION
decreased seek time regarding actuator arm movement	more power in voice coil motor driver stage	controller chip runs too hot	external VD-MOS FET array
decreased seek time regarding rpm	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
faster acceleration and deceleration	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
increased form-factor	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
increased number of platters	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
controlled temperature	less resistance in the circuit	larger MOSFETs required	external VD-MOS FET array
minimal board space	smaller or fewer packages	replacement required for single or dual external FETs	external VD-MOS FET array

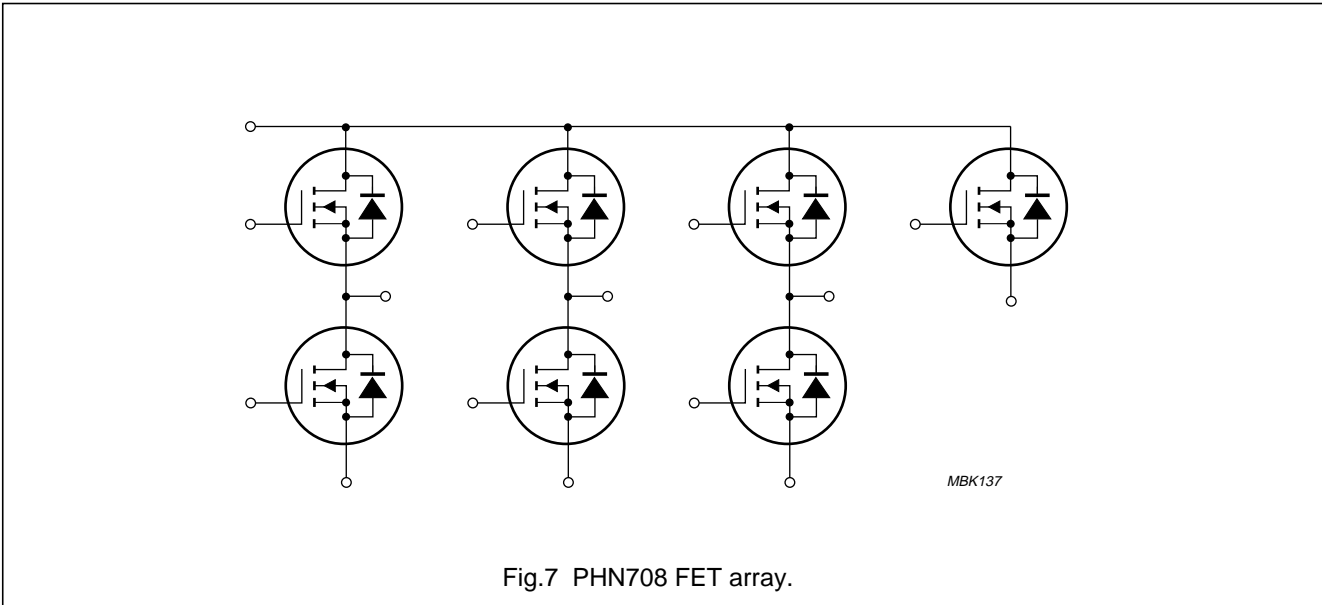


Fig.7 PHN708 FET array.

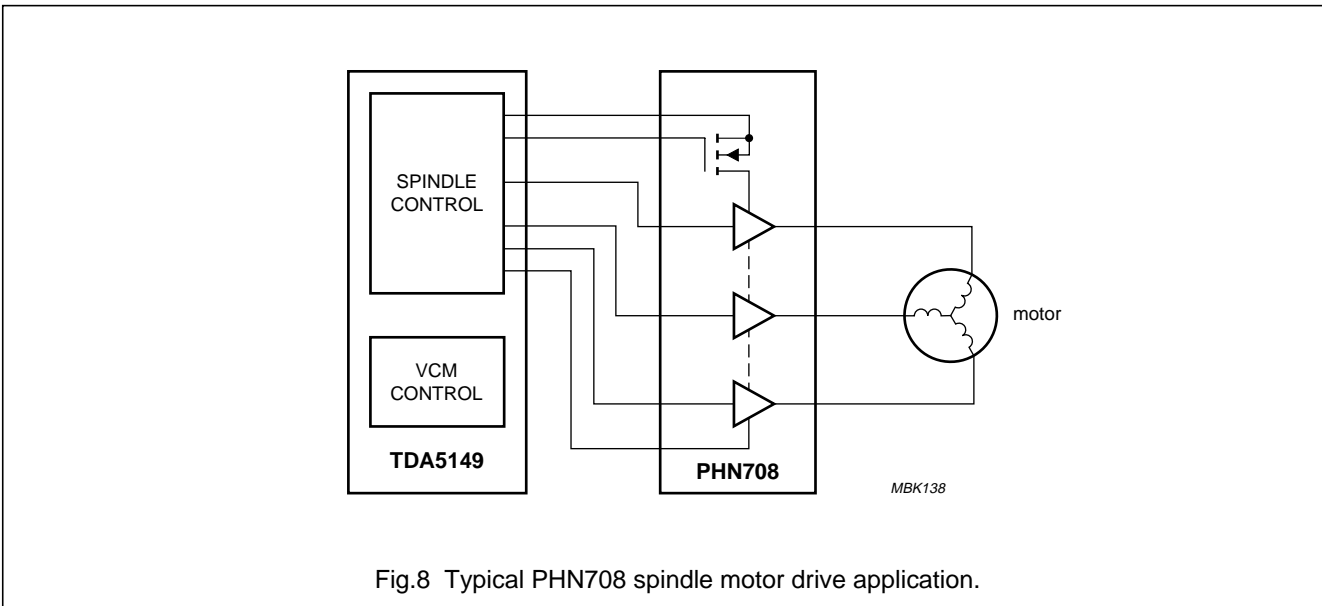


Fig.8 Typical PHN708 spindle motor drive application.

PHN405 – power stage for voice coil motor control

The PHN405 consists of four 50 mΩ max N-channel FETs, two of which have current-sense capability. It is designed for driving voice coil motors. The maximum drain-source voltage is 30 V.

The FETs are configured as shown in Fig.9. The top two FETs have shared drain terminals, while the bottom two FETs have all terminals available to the outside world. To obtain the required accuracy to position the read/write heads of the drive, it is necessary to monitor the current flowing through the motor for each stage. Conventional

solutions require series resistors, which are controversial as they need to have a very low resistance value for reasons of power dissipation. Yet they can't be too small because this would produce a too small reference signal for feedback. These contradicting design requirements were solved by using the top two FETs as 'senseFETs', in fact current mirrors, that represent the current through the voice coil motor in a ratio of 1:36.

The PHN405 comes in a surface-mount SSOP16 package.

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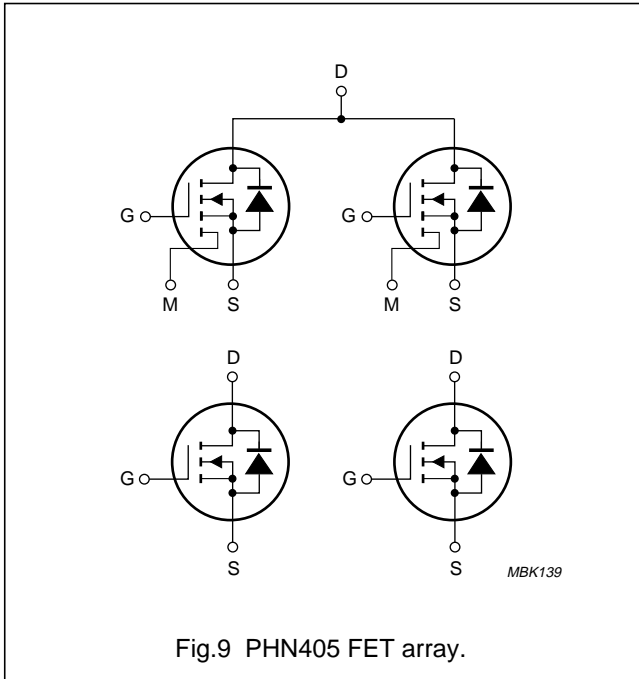


Fig.9 PHN405 FET array.

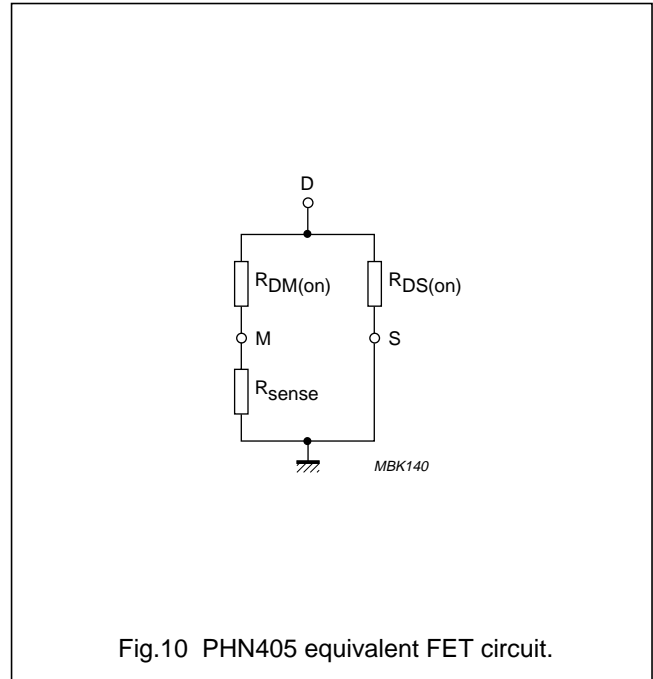


Fig.10 PHN405 equivalent FET circuit.

Current monitoring using senseFETs

Current sensing is often done by means of an external resistor, which is rather expensive due to its required 1-2% accuracy. Also, sensing of the voltage drop would require two extra IC pins and causes performance loss due to the added power dissipation in the resistor. SenseFETs are a better alternative, effectively eliminating all of these problems at the expense of less than 3% more silicon.

A senseFET is a MOSFET that splits the load current into a power and a sense component. In the PHN405, the current ratio is 36 to 1. It is important to know that this ratio is only valid for the condition where the source (S) and monitor (M) terminals are at the same voltage level. If this is not the case, the accuracy of the ratio will decrease, as is explained below.

Think of the FET as a voltage-controlled resistor between drain (D) and source (S) respectively monitor (M) terminals. The equivalent resistance model is shown in Fig.10.

The voltage drop across the sense resistor is:

$$V_{\text{sense}} = R_{\text{sense}} \times \frac{I_D \times R_{\text{DS(on)}}}{R_{\text{DM(on)}} + R_{\text{sense}}}$$

If $R_{\text{sense}} \gg R_{\text{DM(on)}}$ then $V_{\text{sense}} = I_D \times R_{\text{DS(on)}}$.

This is the maximum sense voltage that can be obtained.

Applying these formulas to the PHN405:

$$V_{\text{sense max}} = 5 \times 0.05 = 0.25 \text{ V, and}$$

$$R_{\text{sense max}} = \frac{V_{\text{sense max}}}{I_{\text{sense}}} = \frac{0.25}{5 \div 36} = 1.8 \ \Omega$$

This is the same value as $R_{\text{DM(on)}}$.

Due to the addition of R_{sense} , the current ratio will be:

$$n' = \frac{R_{\text{DM(on)}} + R_{\text{sense}}}{R_{\text{DS(on)}}} \text{ instead of } n = \frac{R_{\text{DM(on)}}}{R_{\text{DS(on)}}$$

The values of both $R_{\text{DM(on)}}$ and $R_{\text{DS(on)}}$ are temperature dependent, and because the currents are different, also the temperatures will be different.

The total accuracy of the system depends on the value of R_{sense} . If R_{sense} is kept smaller than $R_{\text{DM(on)}}$, then an overall accuracy of 5% is achieved. However, if direct current sensing is used, meaning that no sense resistor is used, while keeping the M and S pins at the same voltage level, an overall accuracy of 2% is achieved. This can easily be implemented with today's controller ICs using an op-amp to detect the voltage difference. The voltage difference is compensated with a voltage or current source.

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SIREN DRIVER CIRCUIT FOR CAR ALARMS

Figure 11 shows a siren driver circuit created with VD-MOS FETs. Power is supplied by a 12 V battery, and the driver inputs are complementary pulse waveforms from a microprocessor.

Chosen for our example are two BSN20 VD-MOS FETs in small SOT23 packages and two PHC21025, each comprising two FETs in one SO8 package. In its minimum configuration the circuit requires six components (excluding the speaker) and its maximum configuration is eight components. All components can be surface mounted.

The two push-pull stages X2/X3 and X5/X6 drive the speaker directly. Either X2 and X6 are conducting or X5 and X3, reversing the current through the speaker. Driver stages X1 and X4 convert the 5 V input swing from the microprocessor to the 12 V switching level.

During microprocessor reset and with no alarm, both driver input pins must have the same potential. (0 or 5 V; 0 V is preferred). With the FETs X1 and X4 not conducting, the gates of FETs X2, X3, X5 and X6 will be high, and X2 and X5 will be conducting, resulting in no current through the speaker. When driver inputs are pulsed (complementary), almost the full 12 V is switched over the speaker (a little less due to the on-resistance of the push-pull FETs 100 mΩ N-channel and 250 mΩ P-channel).

When designing this siren driver circuit, take the following into account. The BSN20 (X1 and X4) have an input threshold between 0.4 and 1.8 V. The value of the pull-up resistors R1 + R3 and R2 + R4 must be as small as possible (but not less than 280 Ω) to achieve the highest possible switching speed, and to guarantee a voltage level at the gates of X2 and X5 less than 0.8 V. R3 and R4 are optional, but may be necessary to reduce high through-current in the push-pull stages. When using these resistors however, the gate voltage at X3 and X6 will not fully reduce to 0.8 V, which can influence the on-resistance of these FETs and consequently the dissipation when conducting. When using R3 and R4, the values of R1 and R2 need to be adjusted to maintain the 280 Ω.

Concerning the dissipation in the push-pull stage, the on-resistance of the FETs increases by a factor of 1.7 when operating at 150 °C junction temperature. For the P-channel, which dissipates the most, this means that the on-resistance increases to 425 mΩ. If a 4 Ω speaker is used, the maximum current will be 2.6 A at 12 V. If the pulse is symmetrical and the duty cycle is 50%, the dissipation in the P-channel FET will be 1.45 W. Note that the temperature at the soldering point of the drain pins must not exceed 80 °C.

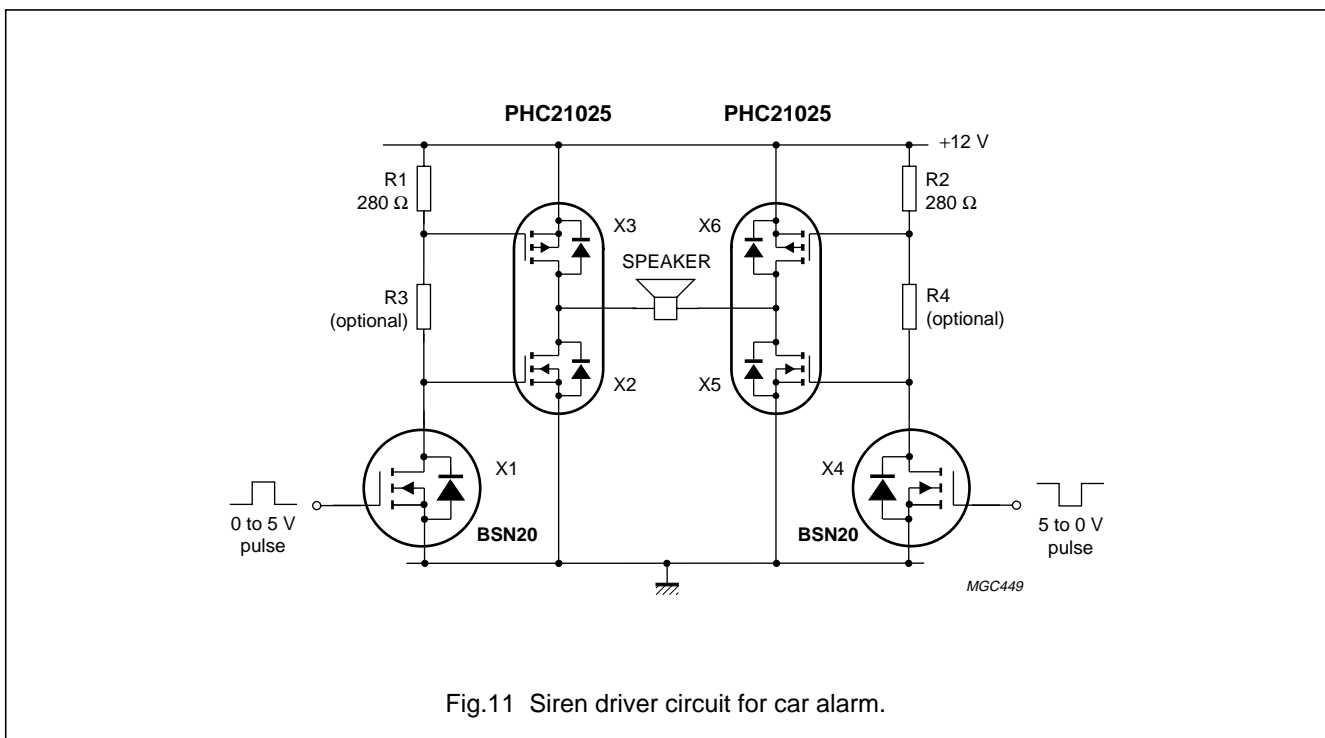


Fig.11 Siren driver circuit for car alarm.

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PRINTED CIRCUIT BOARD HEATSINK AREA FOR SURFACE- MOUNT PACKAGES

When using surface mount components, it is not as easy to dissipate heat in clip-on or bolt-on heatsinks than with through-hole components. With surface mount components, the conductive tracks or pads on the printed-circuit board are often the only means to transfer heat away from the component.

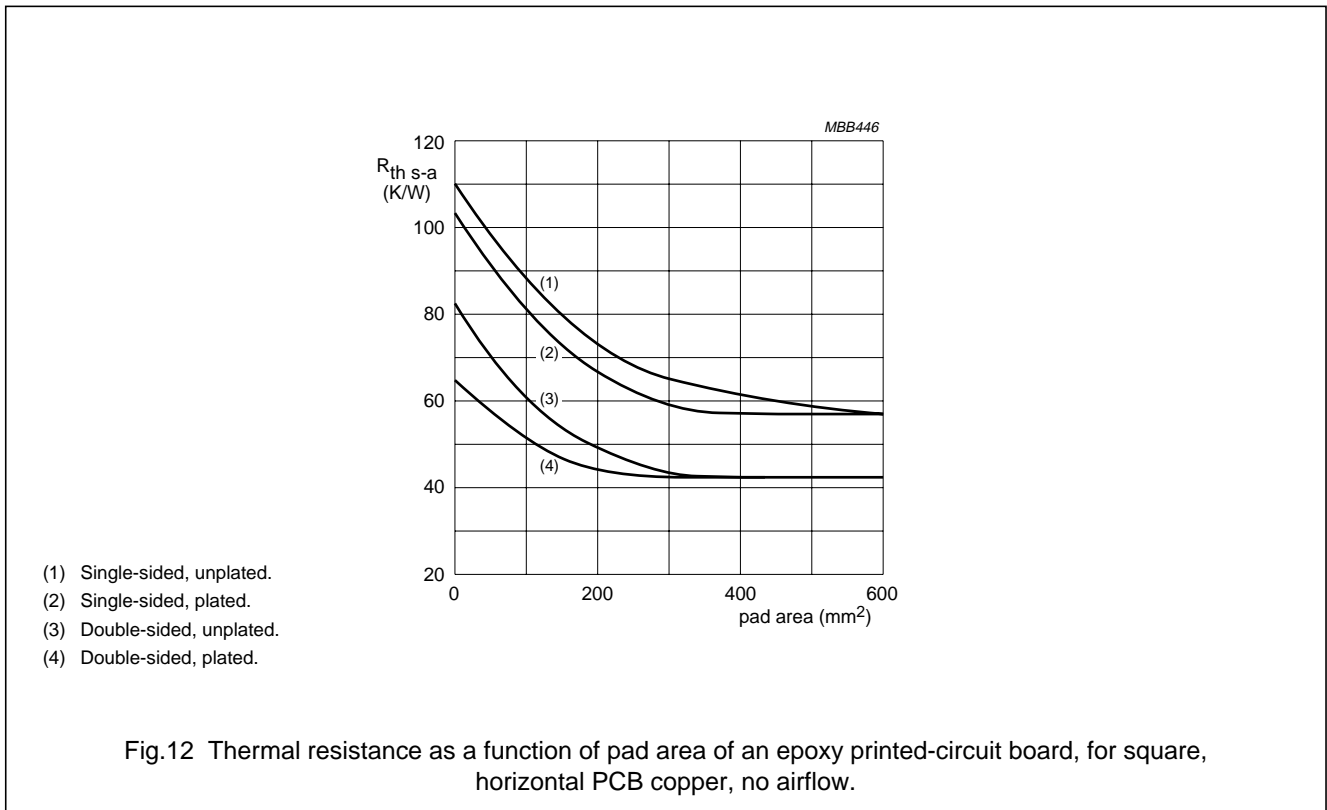
The amount of heat sink area required for the BSP100 type in a SOT223 package can be calculated as follows. This type has been selected as an example for a design that uses a 100 mΩ, N-channel VD-MOS-FET with an I_{DS} of 3 A. The maximum operating junction temperature of this device is 150 °C. At this temperature, the on-resistance of the FET increases with a factor of 1.7 and the power dissipation in continuous use (duty factor 100%) is 1.53 W.

If the ambient temperature is 40 °C, then the total thermal resistance (R_{th}) requirement for FET and PCB is: $(150 - 40)/1.53 = 72$ K/W. The thermal resistance of the FET itself is 10 K/W from junction to the soldering point of the drain tab. Therefore the requirement for R_{th} of the heatsink is $72 - 10 = 62$ K/W.

Figure 12 shows typical thermal resistance from soldering point to ambient as a function of area of an epoxy printed-circuit board. The drain tab of the SOT223 is soldered in the centre of one of the sides (as shown in Fig.13). In this example curve (1) shows a single-sided and unplated copper pad area of 20×20 mm.

A similar calculation can be applied to the SO8 package. Using the PHN210 as an example, we have two 100 mΩ, N-channel VD-MOS FETs in one SO8 package. Taking $I_{DS} = 2$ A per FET and duty factor = 50%, the dissipation per FET is 0.34 W and the total for both FETs is 0.68 W. If the ambient temperature is 60 °C, then the total thermal resistance (R_{th}) requirement for FET and PCB is: $(150 - 60)/0.68 = 132$ K/W. For the SO8 package the R_{th} from junction to the soldering point of the drain tab is 35 K/W, so the requirement for the heat sink thermal resistance is $132 - 35 = 97$ K/W. Referring again to curve (1) in Fig.12, it can be seen that 50 mm² is required.

This example is true for both FETs dissipating equal power. A suggested PCB design is shown in Fig.14. Here the copper is divided into two 3.5×7 mm rectangular portions which gives the required total heatsink area and keeps the drain connections separated.



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