APPLICATION NOTE

- TDA8766G -
10-BIT A/D CONVERTER
DEMONSTRATION BOARD

AN/00014

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1.0	March 1996	Stéphane DESPROGES	AN/96012	First version with "Evaluation Board Documentation" title

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SUMMARY

The **TDA8766** is a 10-bit **A**nalog-to-**D**igital **C**onverter designed for video data digitizing, camera, camcoder, radio communication and other applications. It converts the analog input signal into 10 bits binary digital words at a maximum sampling rate of 20Msps with a power supply from 3 to 5.25V. The reference voltage of the quantization ladder is external.

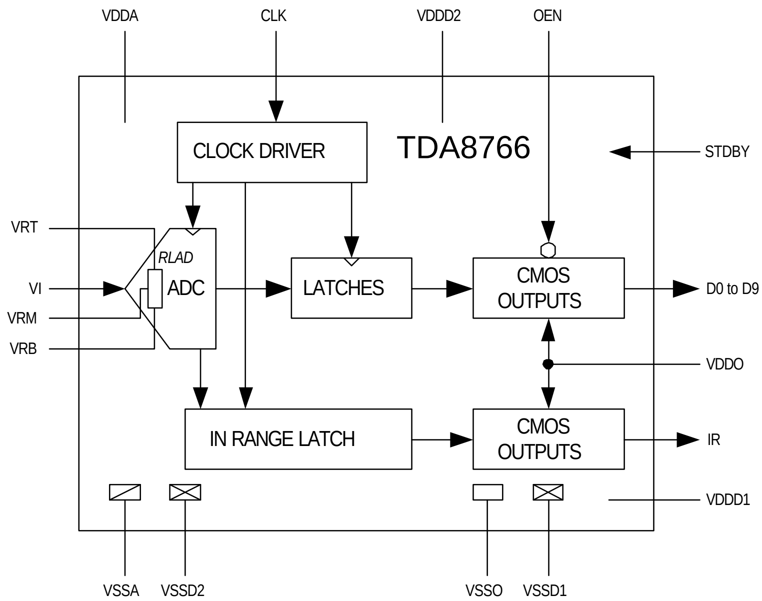
Only one version of this device exist: it is the **TDA8766G**, corresponding to the clock frequency of 20Msps.

This **A**pplication **N**ote describes the design and the realization of the **Demonstration Board** using the **TDA8766G** version (PCB n° 769) with an application environment.

1. MAIN FEATURES OF THE TDA8766G:

The **TDA8766G** is a 10-bit **A**nalog-to-**D**igital **C**onverter. It can convert a typical analog input signal into 10 bits binary digital words at a maximum sampling rate of 20 **M**ega **s**ample **p**er **s**econd with a typical 3.3V power dissipation of 53mW. The **TDA8766G** codes the binary digital words with CMOS digital outputs. The block diagram and the main specifications points of this device are shown on **Figure 1**.

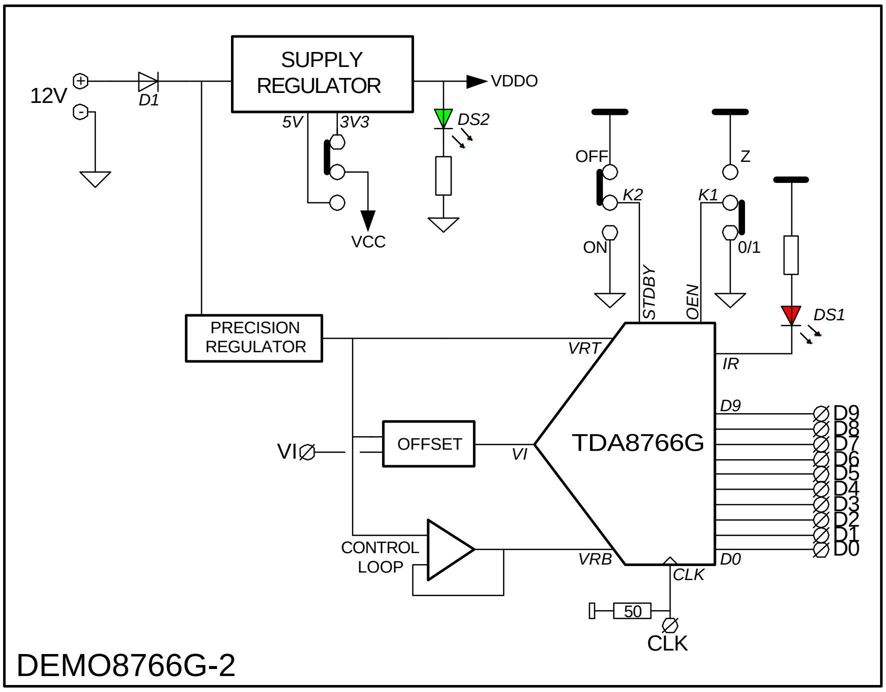
- Clock frequency: 20Msps
- Output voltage: 0V -3V to 5.25V.
- Power dissipation (typical): 53mW (3.3V),
  7.5mW in standby mode.
- Accuracy: 10-bit.
- Supply: 3V to 5.25V.
- Compatibility: input: TTL and CMOS,
  output: TTL and CMOS.



- Figure 1. TDA8766G block diagram -

2. PRINCIPLE AND DESCRIPTION OF THE BOARD:

The principle of the **Demo**nstration **Board** for the **TDA8766G**, which is described in this **A**pplication **N**ote, is shown on **Figure 2**.



- Figure 2. Functional block diagram of Demoboard -

The different blocks of the **Demoboard** are:

- A power **supply regulator** used to supply all the circuitry on the board.
- A voltage **precision regulator** supplying the ADC reference voltage TOP input **VRT** and polarizing the control loop and the input bridge offset.
- A voltage **control loop** circuit making the ADC reference voltage BOTTOM input **VRB** of the quantization ladder, allowing to compensate the different thermal variations of the voltage values.
- A control **offset** bridge polarising the ADC analog voltage input **VI**.

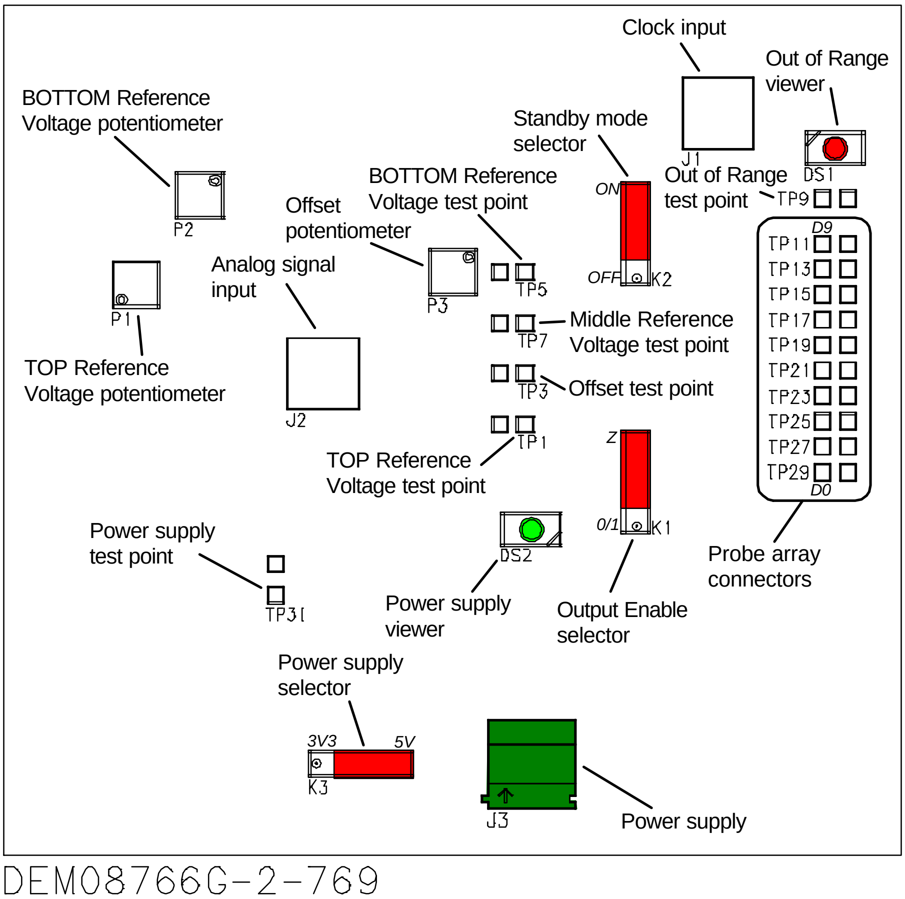
The **Demoboard** works with a single +12V_{DC} external power supply. All circuitry is protected from reverse polarity. The good supply plugging is indicated by the green LED.

The overflow and the underflow of the input analog signal **VI** is indicated by the red LED.

The sample clock signal on the **Demoboard** is external by plugging the square generator in the **CLK** SMA connector. The output impedance of this generator must be 50Ω.

3. OVERVIEW OF THE BOARD:

The whole implantation of the **TDA8766G Demoboard** version is shown on **Figure 3**.



- Figure 3. Overview of Demoboard -

The different connectors, potentiometers, switches, lights and test-points available on the board are:

- **For the general power supply:**

1. A two-points PHOENIX connector **J3** for **$12V_{DC}$** and **GND**.
2. A **PWR** green light **DS2** to indicate the good supply plugging.

- **For the DC voltage adjustment values:**

1. Three chip potentiometers **P1**, **P2** and **P3** to adjust respectively the **VRT** TOP reference voltage, the **VRB** BOTTOM reference voltage and the **OFS** analog input offset of the ADC.
2. Four test-points **TP1**, **TP5**, **TP7** and **TP1** to control respectively the **VRT**, **VRB** and **VRM** reference voltages and **VI+OFS** values.

- **For the evaluation of the TDA8766G:**

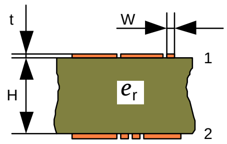
1. A SMA **J2** connector with 50Ω for the analog input signal **VI**.
2. A SMA **J1** connector with 50Ω for the external clock input **CLK**.
3. A switch **K1** to enable the ADC outputs by the input **OEN**.
4. A switch **K2** to stand by the ADC by the input **STDBY**.
5. A **IR** red light **DS1** associated with the **TP9** indicating the out of range of the input analog signal.

- **For the reconstruction of the analog input waveform:**

1. Ten-probe array connectors **TP11**, **TP13**, **TP15**, **TP17**, **TP19**, **TP21**, **TP23**, **TP25**, **TP27** and **TP29** corresponding to the ADC digital output **D9** to **D0** are available to connect the logic analyser which computes the data.

4. PCB DESIGN:

The design is made on a multilayer **P**rinted **C**ircuit **B**oard. The technological concept used to make this PCB is given on **Figure 4**.



- Figure 4. PCB structure -

two physical copper layers are used. Each layer contains the power wires, the signals, the microstrip and the ground planes.

The metallic hole technique is employed to make all the necessary interconnections between the layers. The dielectric substrate used is an Epoxy Glass resin with a relative permittivity (**e_r**) of 4.7 and a copper thickness (**t**) of 35µm (≈1.4mils). The substrate thickness (**H**) is ≈0.8mm (32mils) between the copper layers.

4.1 MICROSTRIP LINES:

To calculate the width (**W**) of these 50Ω matched lines, the Kaup's relation was used:

$$W = \frac{5.98H}{0.8e^{\frac{Zo\sqrt{e_r+1.41}}{87}}} - \frac{t}{0.8},$$

$$\text{(Accurate to within 5\% when } 0.1 < \frac{W}{H} < 3.0 \text{ and } 1 < e_r < 15\text{).}$$

hence:

W = 56.07mils/≈1.4mm,

where:

Zo = 50Ω,
t = 1.4mils/≈35µm,
H = 32mils/≈0.8mm,
e_r = 4.7.

4.2 POWER SUPPLY WIRE:

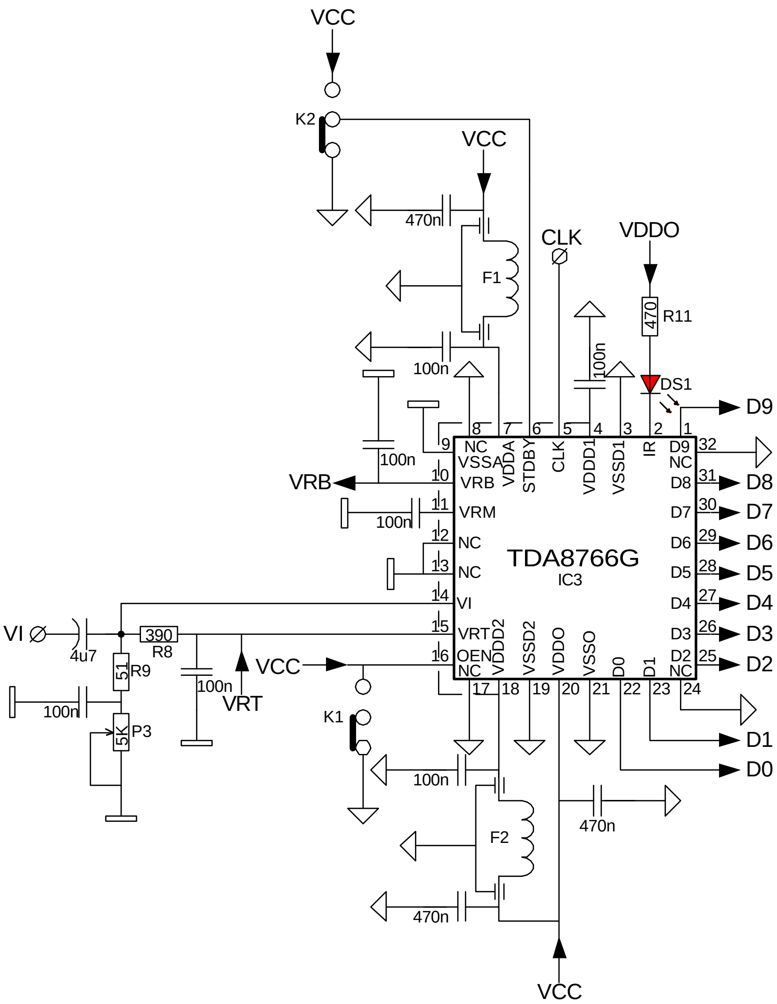
To reduce the voltage fluctuation effects due to switching currents inside the integrated circuits, the power supply wires are designed with a low characteristic impedance of microstrip lines in order to obtain a small equivalent inductance.

4.3 ANALOG AND DIGITAL RETURN GROUND POINT:

To minimise the noise due to capacitive coupling between the analog input and the digital output parts of the ADC, two separate ground planes are designed on all layers and are connected together through an inductor.

5. SPECIAL FEATURES OF THE APPLICATION BOARD:

To obtain optimal performances, the recommended application diagram is given on **Figure 5**.



- Figure 5. TDA8766G application diagram -

5.1 *ADC ANALOG INPUT VI:*

The DC offset voltage is fixed on the board by an intermediate resistor bridge made by the resistors **R8** and **R9** associated with the potentiometer **P3**. The DC offset voltage value is adjusted from the **VRT** reference voltage.
So, the **OFS** typical offset voltage value (which corresponds to code 511/512) is obtained approximately from the relation:

$$OFS = \frac{VRT + VRB - VOST + VOSB}{2},$$

where:

VRT = 3.3V,
VRB = 1.2V,
VOST = 0.135V,
VOSB = 0.135V.

Hence, the typical DC offset level **OFS** corresponding to code 511/512 is:

OFS = 2.25V.

To ensure a sufficient analog input stability, the offset resistor bridge current I_{VI} is fixed at 2.6mA. The value of **P3** is obtained by:

$$R9 + P3 = R8.\left(\frac{OFS}{VRT - OFS}\right) \text{ and } R8 = \frac{VRT - OFS}{I_{VI}},$$

where:

R9 = 51Ω.

The dynamic analog input is connected through a 4.7uF AC coupling to the external generator through a 50Ω microstrip line and a **R9** = 51Ω resistor ending.

A high frequency decoupling of 100nF is added to the potentiometer **P3** so that the decoupling allows to get a good dynamic ground.

The typical peak-to-peak magnitude nominal value $VI_{p.-p}$ of the dynamic input signal is determined from the relation:

$$VI_{p.-p} = VRT - VRB - VOST - VOSB \ ,$$

hence,

$$\mathbf{VI_{p.-p} = 1.83V}.$$

The typical quantum of the **TDA8766G** is:

$$q = \frac{VI_{p.-p}}{2^{10} - 1} \ ,$$

hence,

$$\mathbf{q \approx 1.8mV}.$$

5.2 DATA OUTPUT D0 TO D9:

All data outputs of the **TDA8766G** are CMOS and TTL compatible and they are directly addressed to ten-probe array connectors.

The switch **K1** corresponding to the output enable input **OEN** allows either to enable **0/1** or to put high impedance **Z** state on the data outputs.

The switch **K2** corresponding to the standby input **STDBY** allows to put the **TDA8766G** device in the standby mode.

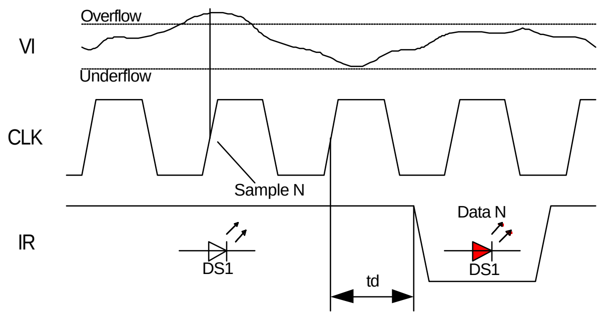
On the **Table 1** is given the correspondence between the different choices.

STDBY	OEN	D9 to D0	IR
0	1	high impedance	
0	0	binary	active
1	X	last logic state	

- Table 1: Selection mode -

5.3 DATA RANGE OUTPUT IR:

The underflow and overflow **IR** output pin is directly connected to the red light LED **DS1**. When the underflow or overflow of the **VI** analog input signal is detected, the red LED is switched on. The functional diagram is shown on **Figure 6**.



- Figure 6. IR voltage waveform -

5.4 ADC ANALOG AND DIGITAL POWER SUPPLIES:

Usually, the power supply form 3V to 5.25V is necessary to supply the TDA8766G, but on the Demoboard, the ADC is evaluated with a 3.3V or 5V power supply (by selector) for the analog, the digital pins and for the output stages.

To ensure a good bypassing at low and high frequencies, the use of several different parallel capacitors is required and SMD bypass π type filters are implanted on the board near the ADC on each power pins.

5.5 REFERENCE VOLTAGES VRB AND VRT:

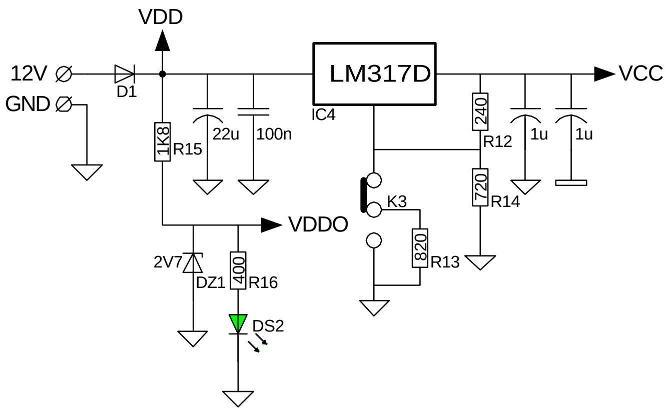
The **TOP Reference Voltage** **VRT** of 3.3V is obtained from a specific IC precision voltage regulator implanted on the board. The regulator output voltage is directly applied on the **VRT** pin of the ADC, a 100nF capacitor placed close to this point constitues an effective decoupling.

The **BOTTOM Reference Voltage** **VRB** of 1.2V is obtained by the control loop from a specific IC low voltage operational amplifier and a transistor. The output voltage of this control loop is directly applied on the **VRB** pin of ADC.

6. ENVIRONMENT CIRCUITS:

6.1 GENERAL POWER SUPPLY:

The electrical diagram is shown on **Figure 7**. Only one IC voltage regulator **IC4** is used directly mounted on the board and it is supplied from an external DC power unit of $12V_{DC}$/50mA. Nevertheless, the external voltage can range from $10V_{DC}$ to $15V_{DC}$.



- Figure 7. Electric diagram of the power supply -

The regulation and the stabilisation of all circuitry com from the **VDD** voltage value obtained after the protection diode **D1**.
The stabilized voltage **VCC** of 3.3V or 5V, depending of the selector **K3** position, are available on the **Demoboard**.

The voltage **VDDO** is used to supply the red light LED **DS1** (underflow/overflow) allowing to have the same brilliancy when the **VCC** change from 3.3 to 5V.

The **VCC** is made from a adjustable regulator IC type LM317D from the relation:

$$VCC = V_{ref}\left(1 + \frac{Z}{R12}\right),$$

where:

V_{ref} = 1.25V (the difference between the output and the adjustment terminal voltages),
R12 = 240Ω.

To obtain **VCC** = 5V, the **Z** must be equal at:

$$Z = R14 = R12\left(\frac{VCC}{V_{ref}} - 1\right),$$

so:

R14 = 720Ω.

To obtain **VCC** = 3.3V, the **Z** must be equal at:

$$Z = \frac{R13.R14}{R13 + R14} = R12\left(\frac{VCC}{V_{ref}} - 1\right),$$

so:

$$R13 = \frac{R12.R14}{\dfrac{R14}{\left(\dfrac{VCC}{V_{ref}} - 1\right)} - R12},$$

hence:

$$R13 \approx 868.2\Omega,$$

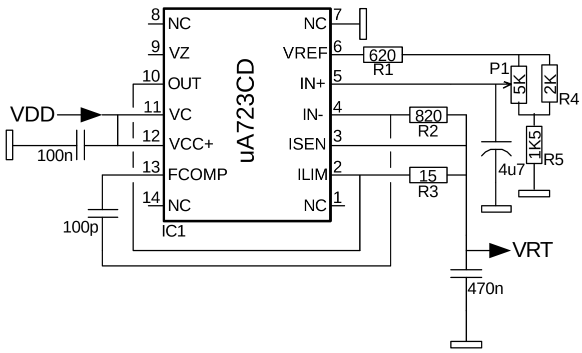
The value chosen is:

R13 = 820Ω.

The BYD17G Silicon diode **D1** ensures the protection of all the circuitry from reverse polarities. The good supply plugging is indicated by a green LED **DS2**.

6.2 TOP REFERENCE VOLATGE REGULATOR:

The precision voltage regulator **IC1 uA723CD** of PHILIPS SEMICONDUCTORS is used and mounted as a positive low-voltage regulator. The electric diagram used is shown on **Figure 8**.

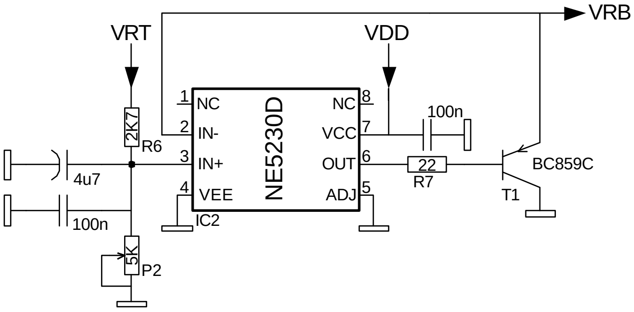


- Figure 8. Electric diagram of the TOP reference voltage -

The voltage level **VDD** obtained on the cathode of the protection diode **D1** is applied on the VCC+ (pin 12) of this device.
The nominal reference level of 3.3V is obtained from the voltage level supplied on the VREF (pin 6) of the **uA723CD**. A bridge resistor **R1**, **R4** and **R5** with a potentiometer **P1** allows to adjust the reference level value on the no-inverting input IN+ (Pin 5) of the IC.
The frequency compensation of the output current amplifier stage is done with an external capacitor of 100pF connected between FCOMP (pin 13) and IN- (pin 4).

6.3 BOTTOM REFERENCE VOLTAGE:

The low voltage operational amplifier **IC2 NE5230D** associated with the transistor PNP **T1 BC859C** of PHILIPS SEMICONDUCTORS is used and mounted as a control loop stage. The electric diagram used is shown on **Figure 9**.



- Figure 9. Electric diagram of the BOTTOM reference voltage -

The **VRB** voltage, controlled by the trimmer potentiometer **P2**, is connected on IN+ (pin 3) of **IC2** and is compared to IN- (pin 2) reference voltage of ADC to compensate the different thermal variations of the voltage values due to the quantization ladder.
The voltage output of the operational amplifier allows to control the conduction of the transistor **T1** which drives the current of the quantization ladder to GND. A resistor **R7** is therefore provided on the board to limit the output current in **IC2**.

6.4 CLOCK JITTER:

The jitter value of the clock signal must be low otherwise some sampling errors can appear. The jitter value can be calculated from the slope of the sinewave input signal. The sinewave input signal is given by:

$$v(t) = \frac{vi_{FS}}{2} . \sin(2.\pi . f_i . t) ,$$

where:

$vi_{FS} = 2^n.q$	: ADC full scale,
n	: ADC bit number,
f_i:	: input signal frequency.

So, the slope of the sinewave is:

$$\Delta v(t) = \Delta t . \frac{\partial v(t)}{\partial t} = \Delta t . \frac{vi_{FS}}{2} .2.\pi . f_i . \cos(2.\pi . f_i . t) .$$

The slope is maximum at t_0=0 (middle of the input full scale):

$$\Delta v(t_0) = \Delta t_0 . vi_{FS} .\pi . f_i ,$$

hence:

$$\Delta t_0 = \frac{\Delta v(t_0)}{2^n.q.\pi . f_i} .$$

For a jitter below the quantum ($\Delta v(t_0)$ = q), it must be inferior at:

$$\mathbf{\Delta t_0 < 86ps},$$

with:

n = 10,
f_i = 3.58MHz.

The variation around the frequency of the sampling clock is given by:

$$\frac{\Delta f_{clk}}{f_{clk}} = \frac{\frac{\Delta t_0 . f_{clk}}{2}}{1 - \left(\frac{\Delta t_0 . f_{clk}}{2}\right)^2} ,$$

hence:

$$\frac{\Delta f_{clk}}{f_{clk}} \langle \pm 400ppm \; .$$

where:

f_{clk} = 20MHz.

7. OPERATING MODE:

An external power unit of 12V/xxmA is required to supply the **Demoboard**. However, the board is able to work between 10V and 15V.

With a power supply of 3.3V, all DC voltage of **P1** (**VRT**), **P2** (**VRB**) and **P3** (**OFS**) are locked in the **S**ystems **& A**pplications **L**aboratories **- C**aen before delivery to be true to the provided product specifications.

So:

VRT = 3.3V,

VRB = 1.2V,

OFS = 2.25V.

But, if the power supply is changed from 3.3 to 5V with **K3** from **3V3** to **5V**, the **VRT**, **VRB** and **OFS** values must be modified by the user to obtain the values above.
The **OFS** value may be modified too to obtain the best full scale of the input analog signal.
To do this, it's better to use the IR viewer to check if the analog input signal is out of range. In this case, the LED **DS1** switches on.

Before putting the board on, please check that **K1** is at **0/1** and **K2** is at **OFF** (referring to the implantation diagram given on **Figure 3**).

7.1 EXTERNAL SINGLE CLOCK OPERATION:

The 50Ω SMA connector J1 is used to connect the 50Ω square clock generator, The required clock levels and time are:

V_{CLK} min = 0.7×VCC,

V_{CLK} max = 0.3×VCC,

t_{rise} max = 10ns.

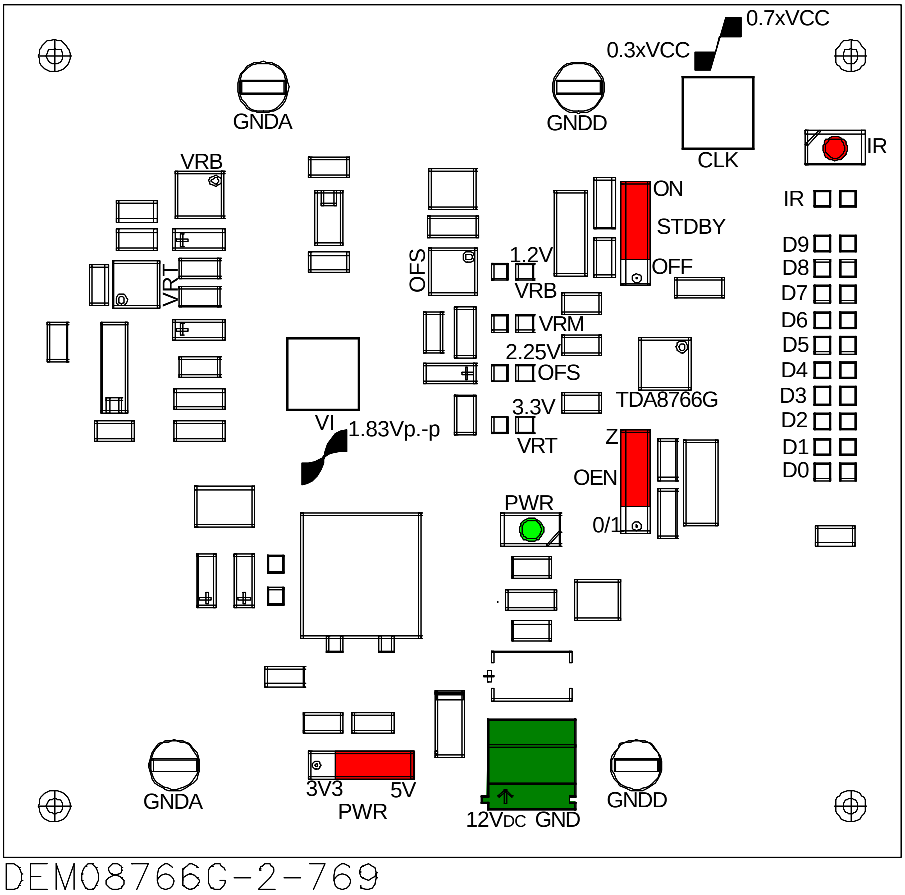
On the **Table 2** is given the values of V_{CLKH} min and V_{CLKH} max according to the power supply values.

POWER SUPPLY:	**3.3V**	**5V**
V_{CLKH} min	2.31	3.5
V_{CLKH} max	0.99	1.5

- Table 2: V_{CLK} values -

7.2 QUICKVIEW OF THE DEMOBOARD:

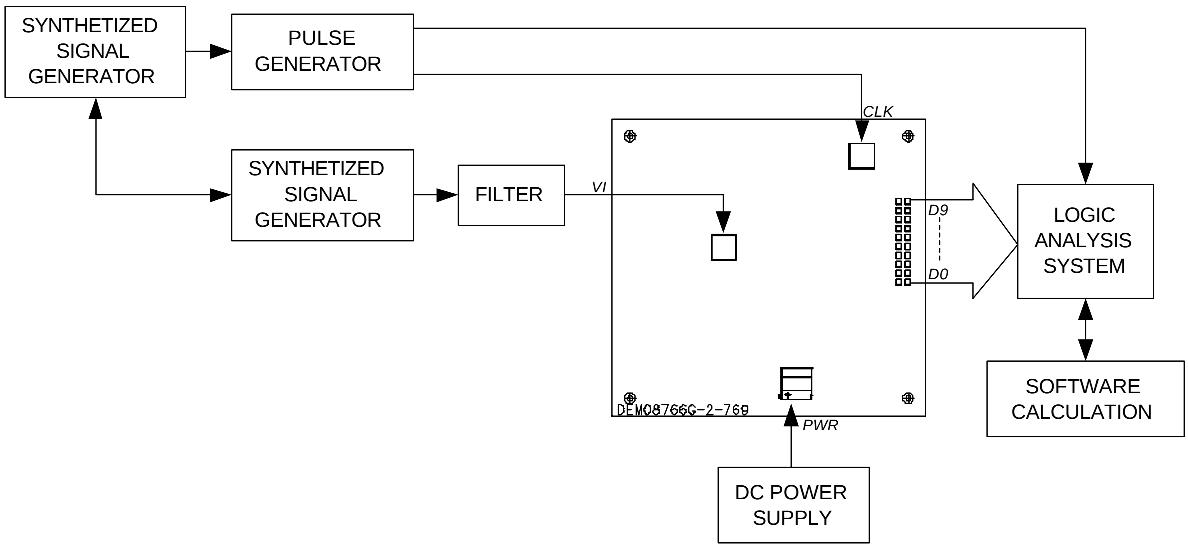
A Quick view of the **TDA8766G Demoboard** with main information is given on **Figure 10**.



- Figure 10. Quickview of the DEMO8766G-2 -

8. PERFORMANCES:

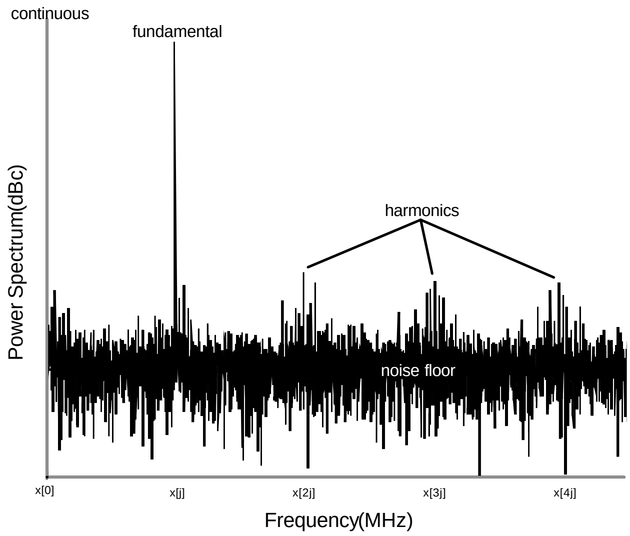
An evaluation of the **TDA8766G** ADC performances were made with the **Demoboard** environment on CAEN's dynamic bench which block diagram is given on **Figure 11**.



- Figure 11. CAEN's dynamic bench block diagram -

8.1 DEFINITION OF THE MEASURING PARAMETERS:

To evaluate the ADC performances on the Demoboard, the CAEN dynamic bench uses the **F**ast **F**ourier **T**ransform for dynamic parameters and the **Histogram** for *static* parameters from the sample signal.



- Figure 12. FFT -

According to the FFT shown on **Figure 12**, the main dynamic parameters are:

- The **T**otal **H**armonic **D**istortion is the ratio between the RMS signal amplitude and the RMS sum of the first five harmonics. From the power spectrum of FFT, the **THD** is calculated from the relation:

$$THD_{dBc} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2}^{6} x^2[i \times j]}}.$$

Where:

$x[j]$: fundamental component corresponding with the j spectrum component,

$x[i \times j]$: component of harmonic i.

- The **S**purious **F**ree **D**ynamic **R**ange is the ratio between the RMS signal amplitude and the RMS value of the highest spectrum component (harmonic or noise). From the FFT, the **SFDR** is calculated from the relation:

$$SFDR_{dB} = 20 \times \log_{10} \frac{x[j]}{MAX(x[i])}.$$

Where:

$x[i]$: spectrum component i with $i \in [2:\frac{N}{2}]$ (N: number of samples) and $i \neq x[j]$.

- The **SI**gnal to **N**oise **A**nd **D**istortion ratio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components. From the FFT, the **SINAD** is calculated from the relation:

$$SINAD_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j}^{\frac{N}{2}} x[i]}}.$$

- The **S**ignal to **N**oise **R**atio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components without harmonic used in the **THD** relation. From the FFT, the **SNR** is calculated from the relation:

$$SNR_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j \times [1:6]}^{\frac{N}{2}} x[i]}}.$$

- The **E**ffective number of bit is calculated by the relation (valid to NYQUIST condition):

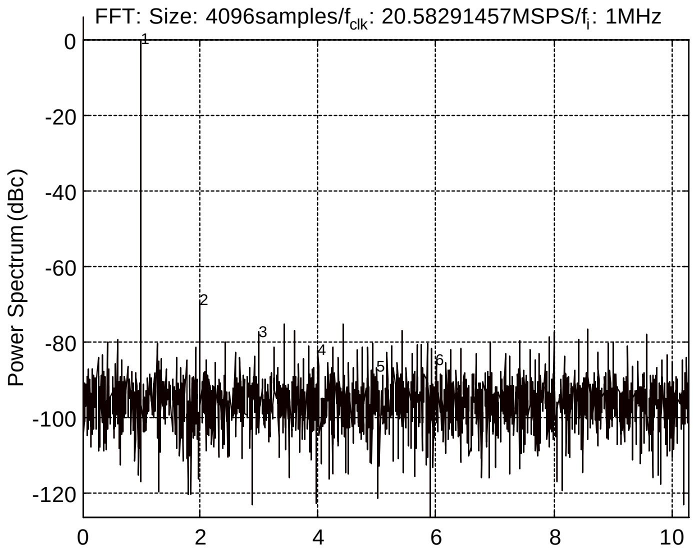
$$E_{BIT} = \frac{SINAD - 10 \times \log_{10} \frac{3}{2}}{20 \times \log 2}.$$

8.2 MEASUREMENT OF THE 20MSPS:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	1MHz.
Waveform:	Sinewave.
Magnitude:	Full Scale (FFT).
Antialiasing Filter:	Yes
Clock frequency:	20Msps.
Output format:	Binary.

The typical results and the corresponding diagrams obtained with these conditions are given on **Figure 13**.



1f_i: 1MHz: 0dBc
2f_i: 2MHz: -69.21dBc
3f_i: 3MHz: -77.53dBc
4f_i: 4MHz: -82.24dBc
5f_i: 5MHz: -86.72dBc
6f_i: 6MHz: -85.02dBc

THD(5H.):68.27dBc
SFDR:-69.21dBc
SINAD:58.37dB(E:9.402bit)
SNR:58.84dB
SFSR:-0.094dB
ENOB:9.418bit

- Figure 15. FFT result of the 20Msps -

9. DEMOBOARD FILES:

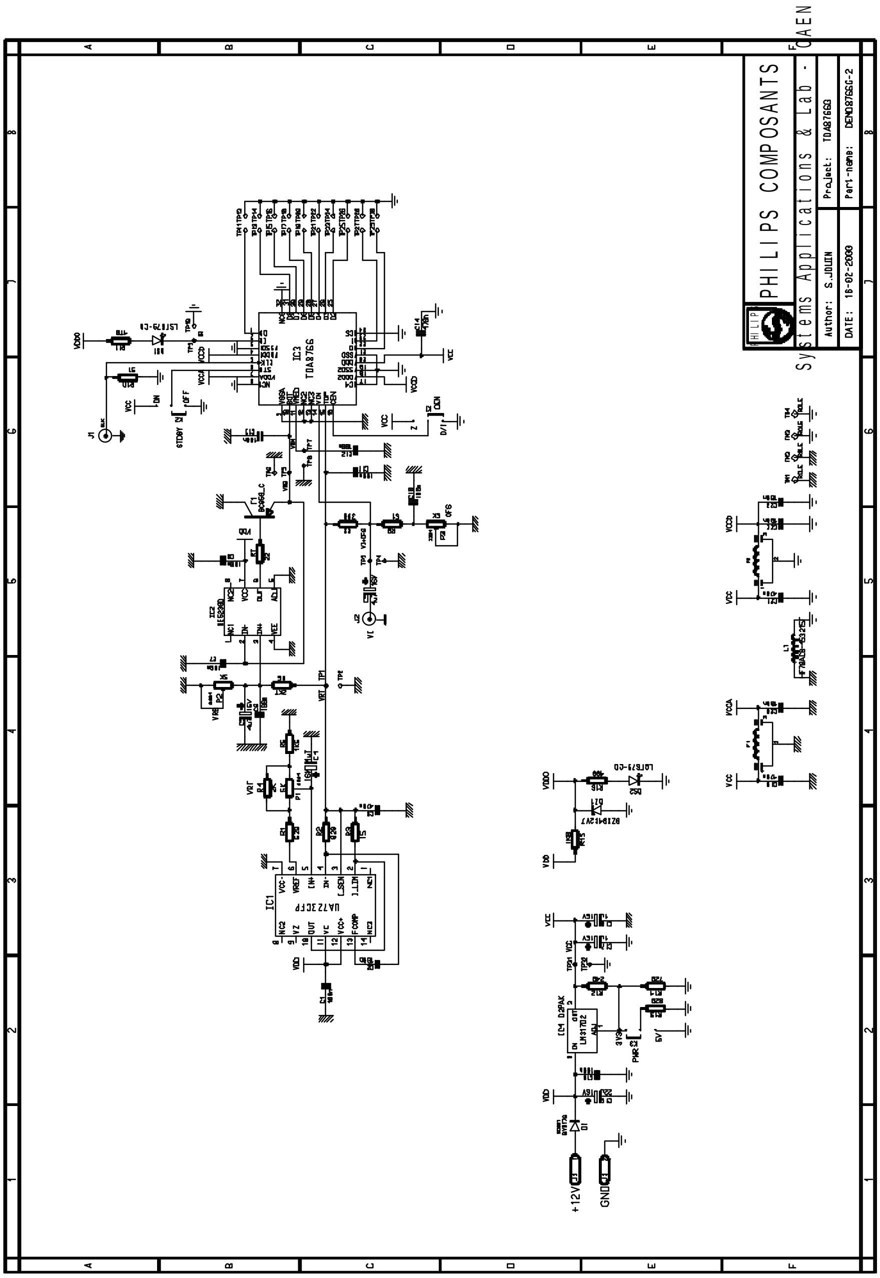
9.1 TDA8766G LQFP32 VERSION:

All documents needed for the realization of this Demoboard are given on **Figures 14 to 18**.

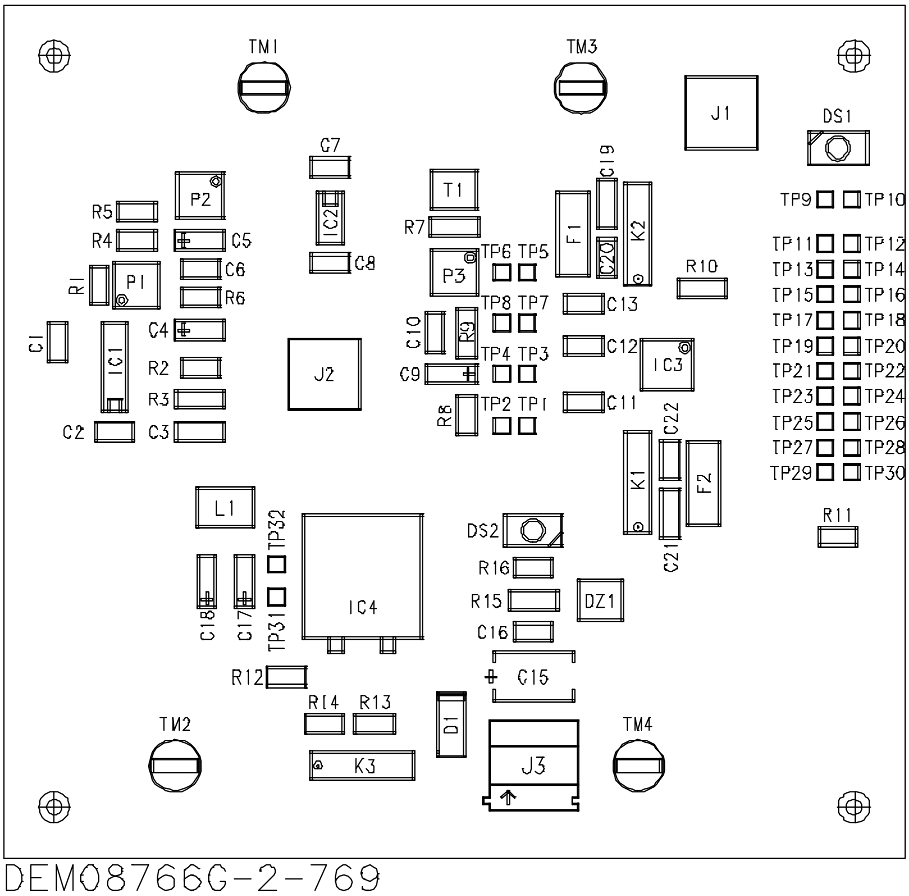
- Electrical diagram.
- Topside component implantation.
- Underside component implantation.
- Topside component layout 1.
- Underside component layout 2.

9.2 COMPONENTS LIST:

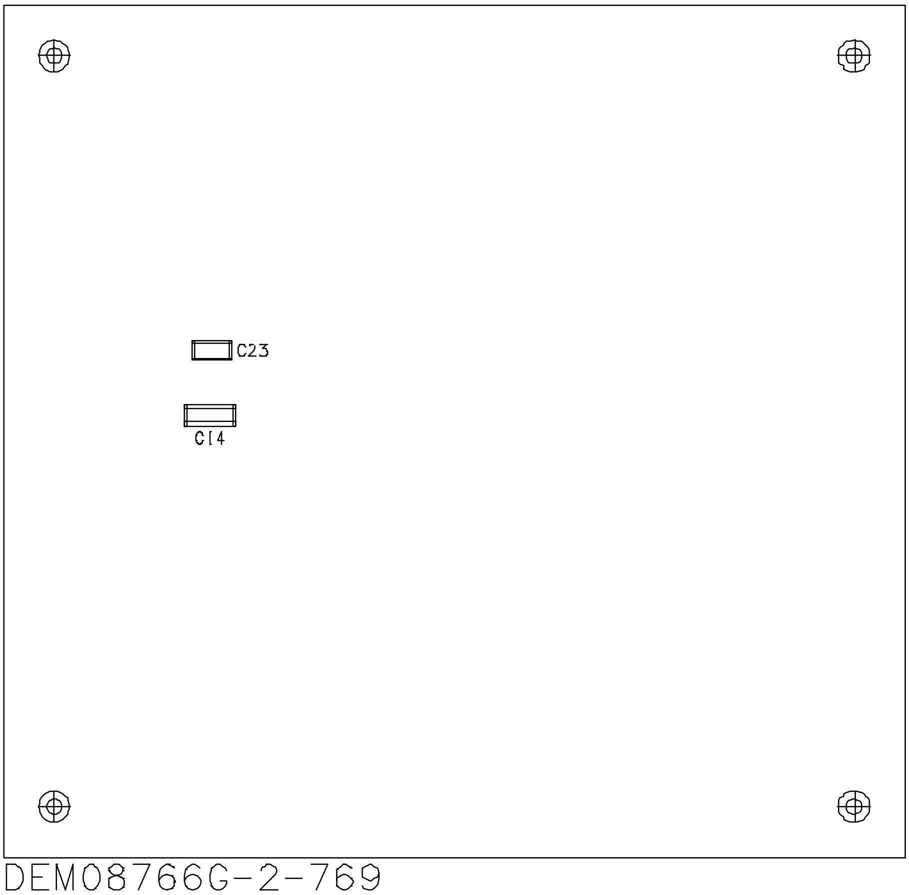
The all version components list with their values and references is given on **Tables 3 to 5**.



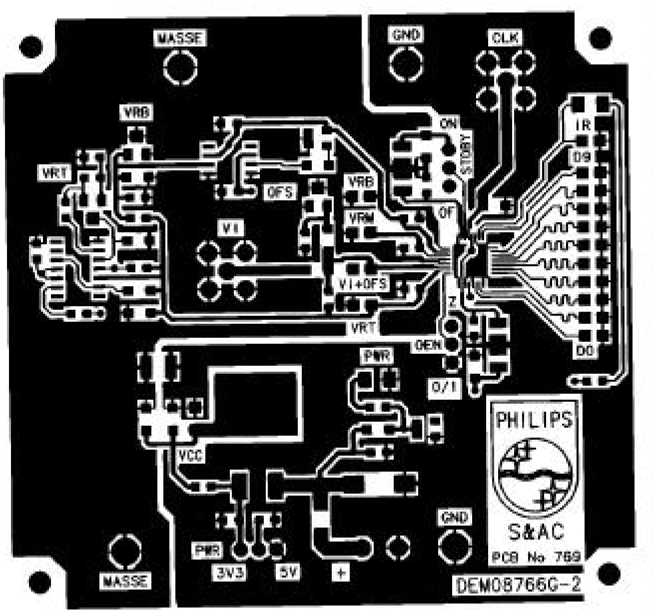
- Figure 14. TDA8766G Demoboard electrical diagram -



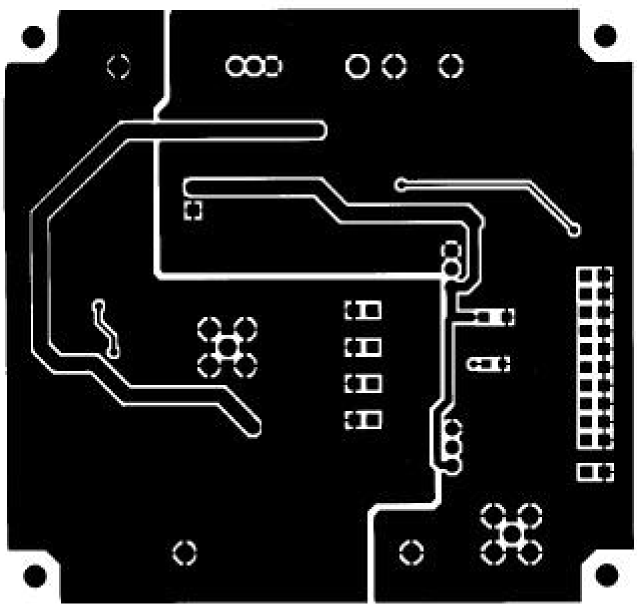
- Figure 15. TDA8766G topside component implantation -



- Figure 16. TDA8766G underside component implantation -



- Figure 17. Topside component layout (layer 1) -



- Figure 18. Underside component (layer 2) -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C1	100nF	CAPACITOR	C0805	PHILIPS
C2	100pF	'	'	'
C3	470nF	'	C1206	'
C4	4.7µF/16V	'	293D/A	SPRAGUE
C5	4.7µF/16V	'	'	‘
C6	100nF	'	C0805	PHILIPS
C7	100nF	'	'	'
C8	100nF	'	'	'
C9	4.7µF/16V	'	293D/A	SPRAGUE
C10	100nF	'	C0805	PHILIPS
C11	100nF	'	'	'
C12	100nF	'	'	'
C13	100nF	'	'	'
C14	470nF	'	C1206	'
C15	22µF/16V	'	293D/D	SPRAGUE
C16	100nF	'	C0805	PHILIPS
C17	1µF/16V	'	293D/A	SPRAGUE
C18	1µF/16V	'	'	'
C19	470nF	'	C1206	PHILIPS
C20	100nF	'	C0805	'
C21	470nF	'	C1206	'
C22	100nF	'	C0805	'
C23	100nF	'	'	'
D1		DIODE	BYD17G	PHILIPS
DS1		RED LED	LST679-CO	SIEMENS
DS2		GREEN LED	LGT679-CO	'
DZ1		DIODE ZENER	BZX84C2V7	PHILIPS
F1	2nF	Π FILTER	4700-003-S	TUSONIX
F2	2nF	'	'	'
IC1		PRECISION VOLTAGE REG	UA723CD	PHILIPS
IC2		LOW VOLTAGE OP. AMPLI.	NE5230D	'
IC3		ADC	TDA8766G	'
IC4		ADJUSTABLE REGULATOR	LM317D	TEXAS INSTRUMENTS
J1	50Ω	CONNECTOR	SMA	RADIALL
J2	50Ω	'	‘	‘

- Table 3. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
J3		CONNECTOR	MKSD	PHOENIX
K2		SWITCH	1C2P	SECME
K4		'	'	'
K5		'	'	'
L1		HF70ACB-453215T	C1812	PHILIPS
P1	5KΩ	POTENTIOMETER	3224W	BOURNS
P2	5KΩ	'	'	'
P3	5KΩ	'	'	'
R1	620Ω	RESISTOR	0805	PHILIPS
R2	820Ω	'	'	'
R3	15Ω	‘	1206	'
R4	2kΩ	‘	0805	‘
R5	1.5kΩ	'	‘	'
R6	2.7kΩ	‘	‘	‘
R7	22Ω	‘	1206	‘
R8	390Ω	‘	0805	‘
R9	51Ω	'	1206	'
R10	51Ω	'	'	'
R11	470Ω	'	0805	'
R12	240Ω	'	'	'
R13	820Ω	'	'	'
R14	720Ω	'	'	'
R15	1.8kΩ	'	1206	'
R16	400Ω	'	0805	'
T1		TRANSISTOR PNP	BC859C	PHILIPS
TM1		MEASUREMENT POINT		COMATEL
TM2		‘		‘
TM3		‘		'
TM4		‘		'
TP1		TEST POINT		COMATEL
TP2		'		'
TP5		'		'

- Table 4. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
TP6		TEST POINT		COMATEL
TP7		'		'
TP8		'		'
TP9		'		'
TP10		'		'
TP11		'		'
TP12		'		'
TP13		'		'
TP14		'		'
TP15		'		'
TP16		'		'
TP17		'		'
TP18		'		'
TP19		'		'
TP20		'		'
TP21		'		'
TP22		'		'
TP23		'		'
TP24		'		'
TP25		'		'
TP26		'		'
TP27		'		'
TP28		'		'
TP29		'		'
TP30		'		'
TP31		'		'
TP32		'		'

- Table 5. List of components -