

**APPLICATION NOTE**

**TDA8050  
QPSK modulator for cable  
uplink transmission.**

**AN96110**

**Abstract**

*The TDA8050 is a QPSK modulator for transmission of information from a home settop box to the headend of a cable system. Burst mode transmission occurs in a small frequency band shared by a number of subscribers each of which transmits in his own time slot.*



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QPSK modulator for cable  
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**Summary**

This report gives the application description of the QPSK transmitter TDA8050.

Further application information is given and also programming sequences for this device are supplied.

Finally an application board, interface board and 3-wire bus software are presented.

# QPSK modulator for cable uplink transmission.

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## 1. INTRODUCTION.

This note gives application information about the QPSK modulator TDA8050. This chip has been designed for modulation of signals to be transmitted by subscribers towards the headend of a cable system. This type of application requires a demodulator which can handle low signal-to-noise ratios (S/N 6dB) and symbol rates up to 1 MSymb/sec at the same time and a modulator delivering 58dBmV typical also for symbol rates up to 1 MSymb/sec. The TDA8050 chip can meet these requirements. The transmitter uses double conversion. Modulation to 140 MHz is followed by down conversion to a range of 5 to 40 MHz.

The transmitter works in burst mode at frequencies from 14 to 26.5 MHz or in an extended range from 5 up to 40 MHz. To demonstrate this and to show some other features of the demodulator chip, a demo board has been developed. Also user interface software running on a PC and a parallel port interface board is available. This board and the measurement methods to evaluate the board are also described in this note.

The TDA8051 is a QPSK demodulator and forms a interaction channel chip-set together with the TDA8050 modulator.

This chip-set TDA8050/TDA8051 is meant to be used in a Settop Box for bidirectional data transmission between this Set Top Box and the Headend. The information can contain control commands, access codes and service information in the downstream (towards the Settop Box) and shopping and bill paying in the upstream (from the Set top Box). Bidirectional communication can be digital voice and network surfing.

The most common modulation technique for digital transmission by a satellite link is Quaternary Phase Shift Keying, QPSK. For cable bidirectional transmission ( interaction channel ) also QPSK modulation is used because it is a cost effective way at the relative low symbol rates compared to the symbol rates necessary for satellite links. The QPSK chip set (TDA8050, TDA8051) has the required functions to modulate and demodulate the QPSK signals. These required functions are:

TDA8050:

- Quaternary Phase Shift Keying burst mode modulation .
- Output buffer with programmable power.
- Quaternary Phase Shift Keying demodulation.
- Phase Locked Loops.
- Symmetrical VCO's with 0-90 degrees signal generation.
- Three wire bus control.

TDA8051:

- AGC detector and amplifier.
- Two matched amplifiers.
- Low noise amplifier .
- Phase Locked Loop.
- Symmetrical VCO with 0-90 degrees signal generation.
- Three wire bus control.

## 2. CABLE UPLINK DESCRIPTION.

In this chapter some elements concerning uplink transmission are described although the standards are not fixed yet.

### 2.1 Modulation.

Differentially encoded burst mode QPSK.

Differential encoding shall generate phase changes from input bits [MSB,LSB] as follows:

**TABLE 1**

Input bits [MSB,LSB]	Phase change (degrees)
00	0
01	-90
10	90
11	180

Symbol rate accuracy: +- 50 ppm

### 2.2 Transmission rate.

256 Kb/s to 2.048 Mb/s.

The upstream data channel is used by all subscriber terminals and controlled by a Protocol for instance Time Division Multiple Access (TDMA). A number of subscribers uses the same RF channel. If the capacity of this channel is exceeded more channels can be used.

### 2.3 Filtering.

$\alpha=0.30$ , square root raised cosine.

### 2.4 Scrambling.

Scrambling begins after the preamble. The scrambler performs a modulo-2 addition of the data with a pseudo-random sequence. A complementary self-synchronising descrambler is used in the headend to recover the data.

### 2.5 RF Parameters.

#### 2.5.1 Frequency range.

Basic 8 - 26.5 MHz, and extended range 5 - 40 MHz at an output level of 33 to 58dBmV.

#### 2.5.2 Channel spacing.

The channel spacing can be for instance 1.5 MHz for 2.048 Mb/s and 187.5 KHz for 256 Kb/s.

**3. FUNCTIONAL DESCRIPTION.**

In this chapter the internal functions of the TDA8050 are discussed.

**3.1 Pinning.****TABLE 2**

<b>Pin</b>	<b>Symbol</b>	<b>Function</b>
1	OUTEN	Output Enable
2	BUF_OUT	Output Buffer balanced Output
3	BUF_OUTC	Output Buffer balanced Output Complement
4	AGND2	Converter Analog Ground
5	I_IN	Balanced Input I
6	I_INC	Balanced Input I Complement
7	Q_IN	Balanced Input Q
8	Q_INC	Balanced Input Q Complement
9	AGND1	Modulator Analog Ground
10	TKa_MOD	Modulator VCO Tank circuit input 2
11	TKb_MOD	Modulator VCO Tank circuit input 1
12	CP_MOD	Modulator Charge Pump output for PLL loop filter
13	DVCC	Digital supply
14	CK	3 wire bus Clock
15	DATA	3 wire bus Data
16	EN	3 wire bus Enable
17	OSC_IN	X-tal oscillator input
18	DGND	Digital Ground
19	CP_CONV	Converter Charge Pump output for PLL loop filter
20	TUNE_CONV	Tuning voltage output for Converter VCO
21	TKb_CONV	Converter VCO Tank circuit input 1
22	TKa_CONV	Converter VCO Tank circuit input 2
23	LOCK	Lock detect signal output
24	IF_FILT	IF balanced output to IF Filter
25	IF_FILTC	IF balanced output to IF Filter Complement
26	AVCC1	Modulator Analog supply
27	RF_OUTC	RF balanced output to RF Filter Complement
28	RF_OUT	RF balanced output to RF Filter
29	AVCC2	Converter Analog supply
30	RF_IN	RF balanced Input to programmable amplifier
31	RF_INC	RF balanced Input to programmable amplifier Complement
32	SW_CAP	Switch capacitor

**3.2 X-tal Oscillator.**

The internal X-tal oscillator is designed to oscillate with an external crystal in series with a small capacitor (27pF typical). This series circuit is to be connected between SW\_CAP (pin32) and preferably Vcc although Vss may be used instead. One of three crystal frequencies may be chosen: 1,2 or 4 MHz. The serie resistance should be less than 100 Ohm, the paralel capacitance less than 10pF. The crystal operates in series resonance mode. The crystal oscillator is used to drive the modulator PLL as well as the convertor PLL.

**3.3 Modulator.**

The modulator consists of two mixers. Each mixer has an symmetrical buffered input called I and Q. Each mixer has also an LO of 140 MHz, one however 90 degrees shifted with respect to the other. These 0 and 90 degrees signals are derived from a Phase Locked Loop stabilized LC oscillator at 280 MHz via a divide by two part. The LC oscillator is Phase Locked to the crystal oscillator. The outputs of the mixers are added to produce the QPSK signal at 140 MHz.

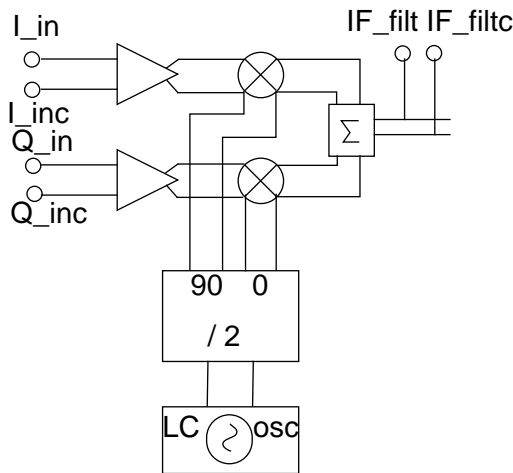


Fig.1 Modulator section.

**3.3.1 Modulator Phase Locked Loop.**

The modulator phase locked loop consists of:

- 1) A fixed main divider of 1120 dividing the 280 MHz oscillator to 250 kHz comparison frequency.
- 2) A programmable reference divider of 4 to 16 dividing the x-tal frequency to 250 KHz.
- 3) A digital phase comparator working at a comparison frequency of 250 kHz.
- 4) A fixed value charge pump of 0.25 mA to drive (via a loop filter) the varicap diodes for controlling the LC oscillator.

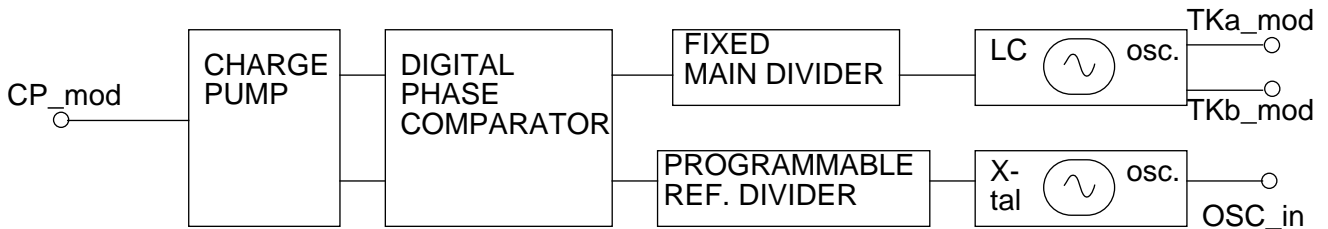


Fig.2 Modulator PLL.

**3.4 IF Filter.**

The QPSK signal is filtered by a 140 MHz LC band pass filter to reduce any unwanted signals in the IF spectrum like baseband signals and 280 MHz LO leakage. This filter should have a -1 dB bandwidth higher than the symbol rate in order not to influence the output flatness.

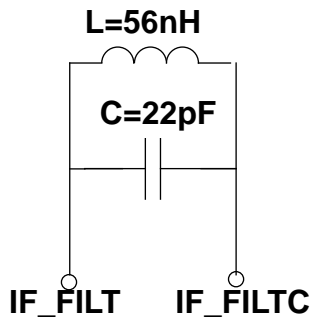


Fig.3 IF Filter Example. (140 MHz)

**3.5 Converter.**

The converter consists of a mixer. The mixer LO is derived from a Phase Locked Loop stabilized LC oscillator which is tunable over a range from 145 to 180 MHz. This mixer produces the difference frequency of 5 to 40 MHz. The LC oscillator is Phase Locked to the crystal oscillator.

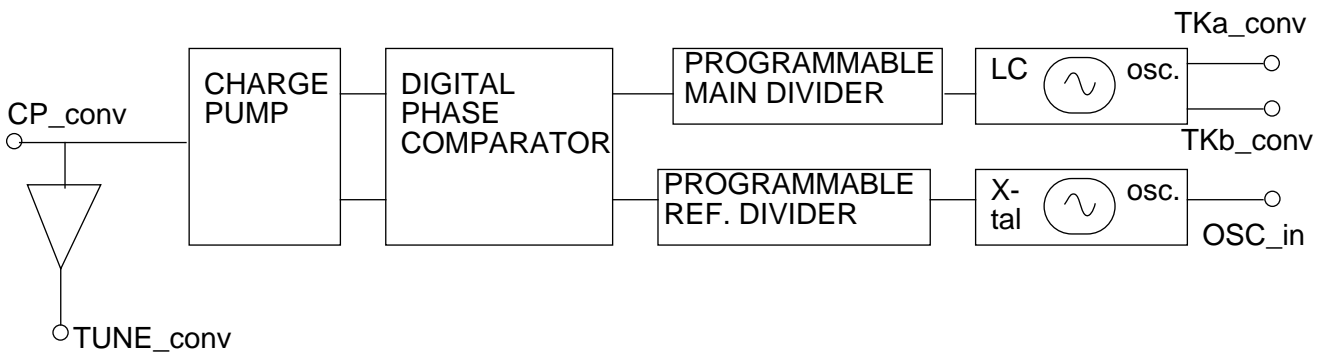


Fig.4 Converter PLL.

### 3.5.1 Converter Phase Locked Loop.

The converter phase locked loop consists of:

- 1) A programmable main divider of 290 to 3600 and a fixed main divider of 4 together dividing the converter oscillator of 145 - 180 MHz to a comparison frequency of 12.5 to 125 kHz.
- 2) A programmable reference divider of 4 to 160 and a fixed divider of 2 together dividing the x-tal frequency to 12.5 to 125 kHz.
- 3) A digital phase comparator working at a comparison frequency of 12.5 to 125 kHz.
- 4) A "smart" charge pump of 1, 0.3, or 0.085 mA. It can be programmed to switch automatically to a lower charge current.
- 5) A tuning amplifier with a maximum output voltage of 9 Volt capable of tuning the oscillator (via a loop filter) over the 145 to 180 MHz range.

### 3.6 RF Filter.

A symmetrical RF filter is to be connected between RF\_out, RF\_outc and RF\_in, RF\_inc with a stopband starting beyond the desired highest baseband frequency.

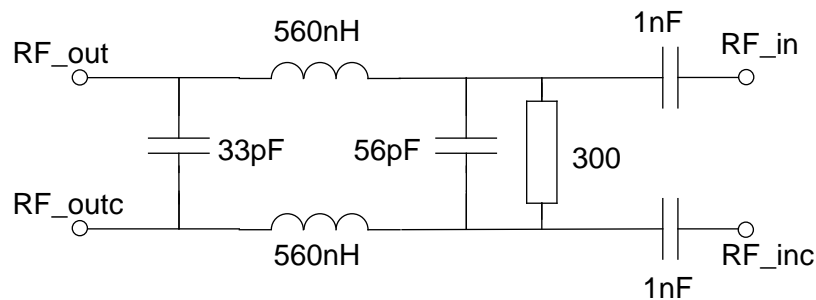


Fig.5 RF Filter example. (26.5 MHz)

### 3.7 Programmable Gain and Output Buffer.

Depending on cable length between settop box and headend an adjustable output power is required to compensate for this variable cable attenuation so the headend will receive all uplink transmissions at the same power level. Therefore a programmable gain amplifier is implemented with a range of 48 dB in 32 steps. This gain amplifier has also an OUTEN (pin 1) by which the output can be switched off for burst mode purposes. An external switch capacitor can be connected to SW\_CAP (pin 32) to adjust the on>off and off>on speed of the amplifier.

The output buffer, which can be shut down by software, is capable of delivering 58 dBmV into a 75 Ohm load via a 300 to 75 Ohm transformer.

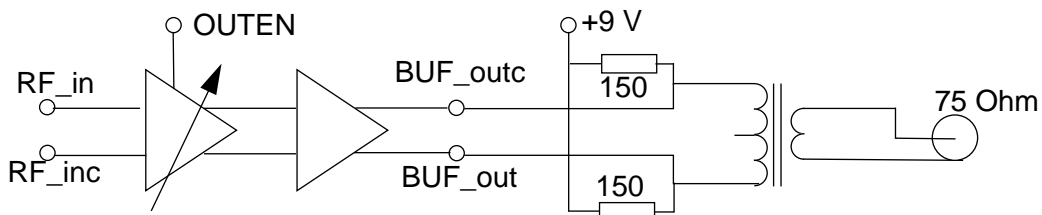


Fig.6 Output Configuration.

### 3.8 3 Wire Bus.

A 3 wire bus is implemented to send programming data to the:

- Programmable modulator reference divider (mp1, mp0).

**TABLE 3**

mp1	mp0	ratio
1	1	4
1	0	8
0	1	16
0	0	forbidden

- Programmable converter reference divider (r7..r0). Ratio from 4 to 160.
- Programmable main divider (p11..p0). Ratio from 290 to 3600.
- Converter charge pump (cr2..cr0).

**TABLE 4**

cr2	cr1	cr0	lock_converter	Charge Pump (mA)
0	0	0	0	1.0
0	0	0	1	0.3
0	0	1	0	0.3
0	0	1	1	0.085
0	1	0	x	0.085
0	1	1	x	0.3
1	0	0	x	1.0
other combinations			x	0.085

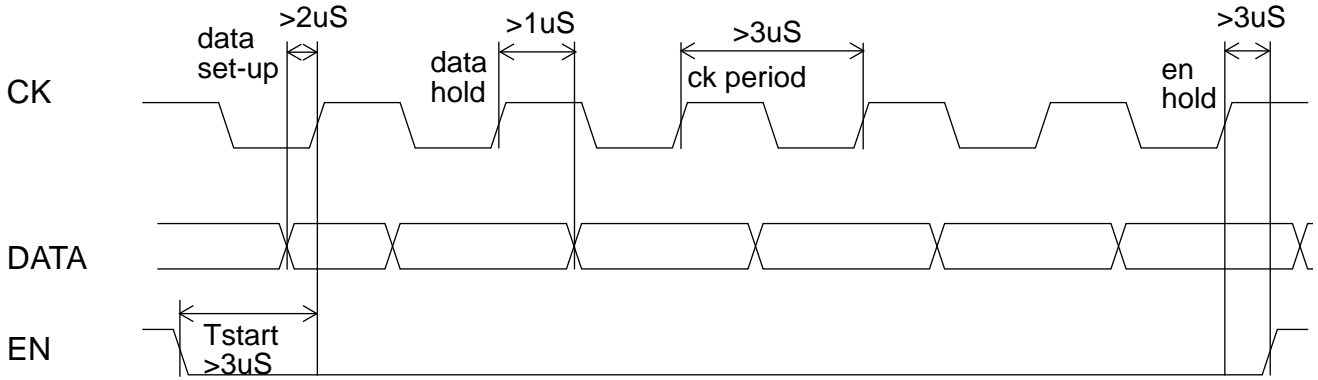
Lock\_converter is an internal signal indicating converter PLL in lock (1 = true).

- Programmable gain amplifier (dac4..dac0). Value from 0 to 31.
- Output buffer enable (oen). Value 1 = enable, 0 = disable.

**TABLE 5 Data format.**

DATA												ADDRESS	
d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	ad1	ad0
first in												last in	
Modulator Reference Divider Ratio				Converter Reference Divider Ratio									
x	x	mp1	mp0	r7	r6	rr5	r4	r3	r2	r1	r0	0	1
Control Register													
x	x	x	oen	cr2	cr1	cr0	dac4	dac3	dac2	dac1	dac0	1	0
Main Divider Ratio													
p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0	1	1

3.8.1 3 Wire Bus Waveforms.



**4. Application information.**

**4.1 Calculating Loop Components.**

The modulator synthesizer PLL as well as the converter synthesizer PLL need a loop filter. This filter must be designed in such a way that these PLL's are stable, the comparison frequency residues are minimal and acquisition time is adequate.

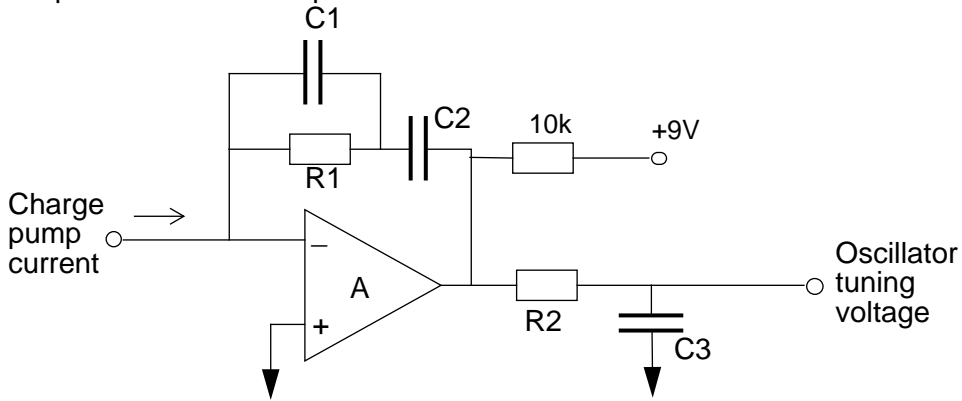


Fig.7 Basic active third order loop filter.

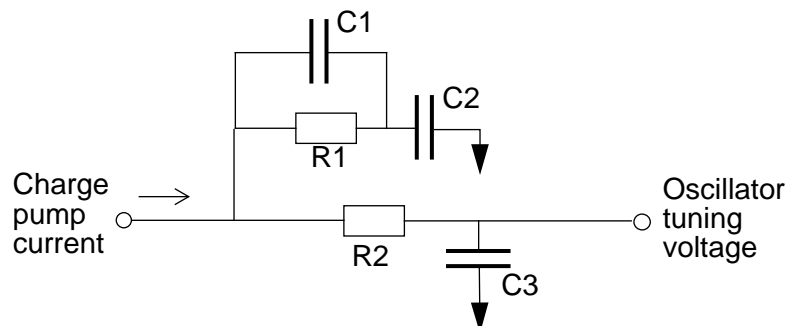


Fig.8 Basic passive third order loop filter.

In the above basic loop filter diagram C2 and R1 are the main loop filter components. C1 is for suppressing comparison frequency residues and is small (1/20) with respect to C2 so it does not influence the loop filter behaviour. R2, C3 is a low pass filter with a corner frequency logarithmically in the centre between the comparison frequency and the loop filter natural frequency.

The main filter components C2 and R1 can be calculated by the design formulae:

$$C2 = \frac{K0 \times Kd}{\omega^2 \times N}$$

$$C1 = \frac{C2}{20}$$

$$R1 = \frac{2\zeta}{\omega \times C2}$$

In which:

Ko: oscillator constant in Mradians per second.

Kd: detector constant in  $\mu\text{A}/\text{radian}$ .

$\zeta$ : damping factor.

N: total main divider ratio (= LO frequency / Comparison frequency)

$\omega$ : natural frequency of the loop in radians per second. ( $f_n$  in Hz/s).

To determine the values for these factors the following considerations have to be taken into account:

For Ko a corner frequency per Volt value is necessary to cover the tuning range (e.g. 0 for the modulator and  $35 \text{ MHz} \times 2\pi$  for the converter for the output range of 5 to 40 MHz). Also an additional range has to be added to compensate for component tolerances.

$$K0 = \frac{2\pi \times \Delta f}{\Delta Vt}$$

$\Delta Vt$  is the tuning voltage which is 5 Volt for the modulator and 9 Volt for the converter.

For Kd holds

$$Kd = \frac{I_{cp}}{2\pi}$$

so for the converter the charge pump current has to be chosen from the given list (see tabel 4).

The damping factor  $\zeta > 0.8$ , usually 1 is a good value. If  $\zeta = 0.8$  the phase margin will be 70 degrees.

The natural frequency depends on the goals to achieve. A high natural frequency suppresses the phase noise of the local oscillator so a high loop bandwidth seems advisable. However the higher the loop bandwidth the more

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difficult it is to filter out the comparison residues.

A good compromise is to choose the loop natural frequency at 1/1000 of the symbol rate for the modulator PLL as its comparison frequency is 250 KHz fixed and a lower natural frequency for the converter PLL as its comparison frequency can be chosen between 12.5 and 125 kHz.

### 4.1.1 Example:

Modulator PLL.

$$K_o = 2\pi * 7 \text{ MHz/V}$$

$$K_d = 250 \text{ mA/rad}$$

$$\omega = 2\pi * 2000 \text{ rad/s}$$

$$\zeta = 1$$

$$N = 1120$$

$$f_n \ll 1/2\pi R_2 C_3 \ll f_{comp}$$

Resulting in  $C_2 = 9.895 \text{ nF}$

$$R_1 = 16 \text{ k}$$

$$C_1 = 470 \text{ pF}$$

$$R_2 = 22 \text{ k}$$

$$C_3 = 330 \text{ pF}$$

## 4.2 Calculating tank circuit components.

The modulator LO as well as the converter LO need an LC tank circuit capable of being locked to the crystal oscillator and being tuned over the desired range.

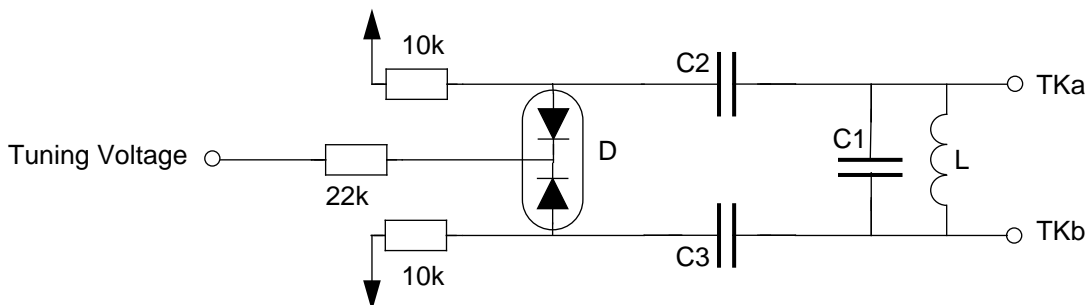


Fig.9 Tunable tank circuit.

The tank circuit components C1 and L can be calculated by the design formula:

$$(2\pi f)^2 LC_{total} = 1$$

$C_{total}$  consists of C1 and the series capacitance of C2, C3 and D.

The double capacitance diode D has to be chosen for its capability to tune the tank circuit over the tuning range and some extra range caused by tank circuit tolerances.

L has a value low enough to obtain a good quality factor for this tank circuit and high enough to be tuned with a normal capacitance diode. 22 nH for the modulator and 56 nH for the converter are typical values.

C2 and C3 are to decouple the tuning voltage from the tank circuit and can be used to lower the tuning range by lowering their value.

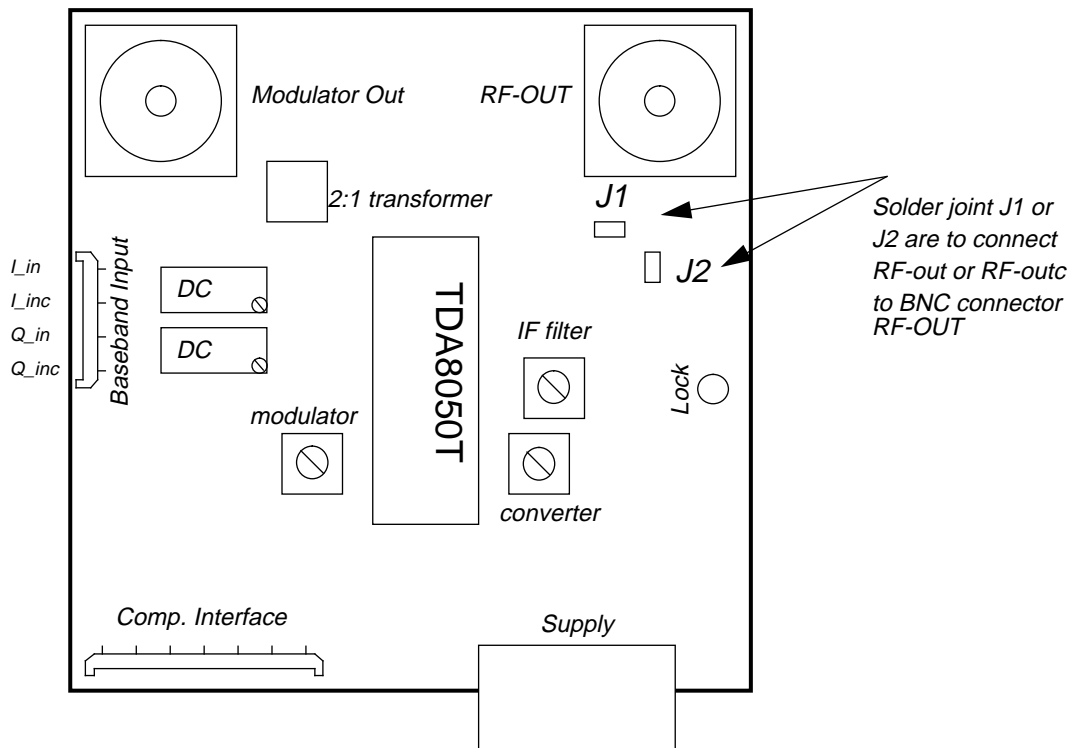
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**5. Hard- and Software.**

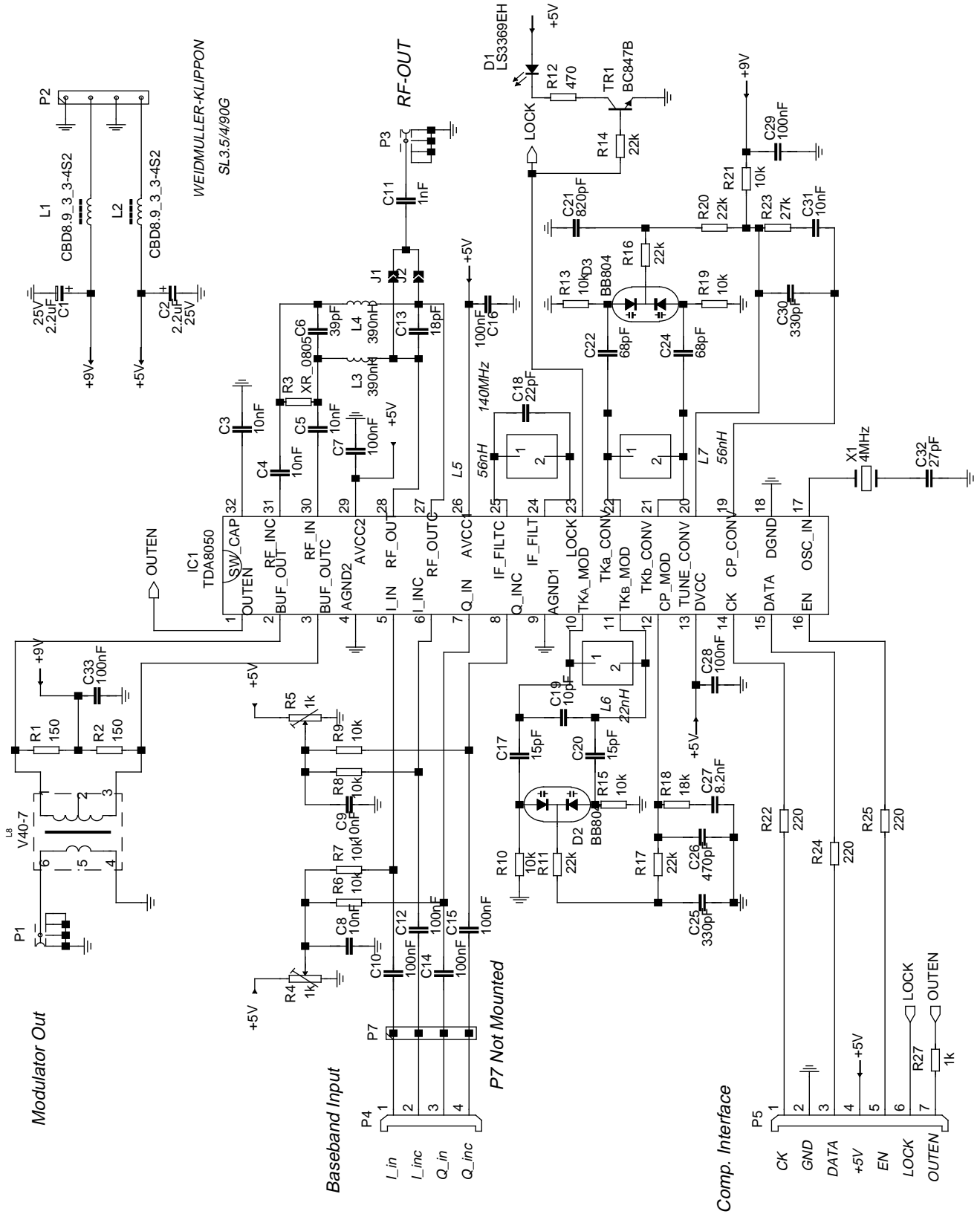
**5.1 Application Board.**

An application board has been made to demonstrate the capabilities of the TDA8050 modulator. The board contains a TDA8050T, the loop filters and tank circuits for both synthesizers, the IF and RF filters, an output transformer to adapt to 75 Ohm, an I and Q input connector with DC balancing potentiometers and a computer interface connector. The board is designed to produce a QPSK modulated signal at an RF frequency programmable from 5 to 40 MHz, although the RF filtering has a corner frequency of 26.5 MHz. All programmable functions can be controlled via the computer interface. Also the hardware output enable (outen) can be switched and the converter synthesizer lock detect is read out on this interface.



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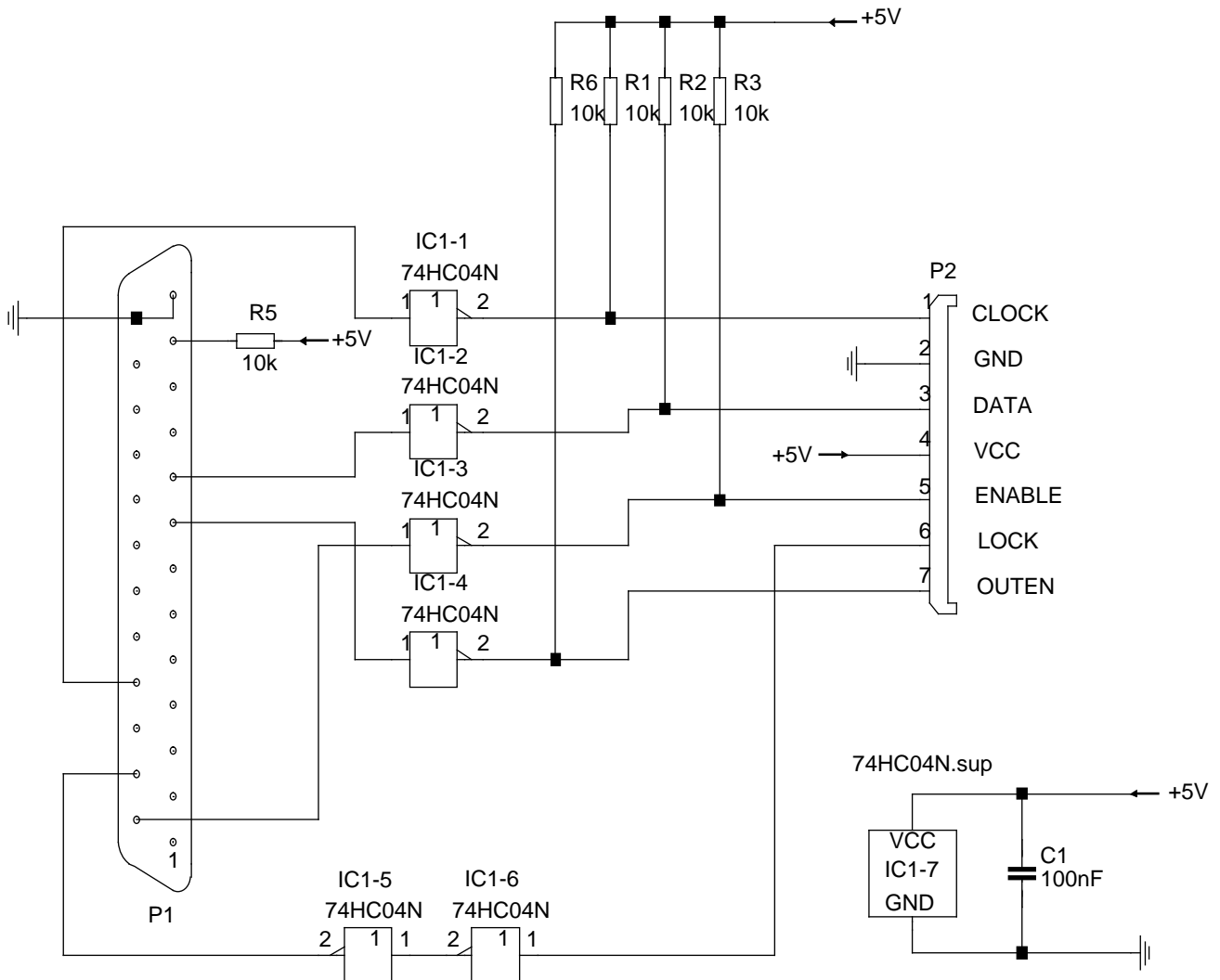


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## 5.2 Computer Interface Board.

A computer interface board has been made to connect the application board to the parallel port of a personal computer. This board allows the transfer of the 3-wire bus signals (clock, data and enable) to the application board. Additionally it transfers the chip's output enable to the board and the converter synthesizer lock detect from the board.



## 5.3 Software.

A 3.5 floppy disc is available containing a Windows based program called DBUI, capable of controlling the application board via the parallel interface board. In this DBUI window all control commands can be given in a user friendly way. Also lock indication is visible.