

# ERRATA SHEET

**Date:** 2004 Aug 31  
**Document Release:** Version 1.1  
**Device Affected:** P89LPC935

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2004 Aug 31

**Identification:**

The typical P89LPC935 devices have the following top-side marking:

P89LPC935x x  
xxxxxxx xx  
xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC935:

Revision Identifier (R)	Comment
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

**Errata Overview - Functional Problems**

Functional Problem	Short Description	fixed in revision	added
CCU.1	CCU in Alternate output mode inverting	none	v1.0
CCU.2	CCU in Alternate output mode halting	none	v1.1
CCU.3	CCU PLL divider	none	v1.1
CCU.4	CCU capture reading ICRxH	none	v1.1
ADC.1	Single Step mode multi channel boundary interrupt	none	v1.0
ADC.2	Timer/Edge with Scan Mode Counter Reset	none	v1.0
EEPROM.1	EEPROM lock-up on power up	none	v1.1

**Errata Overview - AC/DC Deviations**

AC/DC Deviation	Short Description	fixed in revision	added
-	-	-	-

**Errata Notes**

Note	Short Description	added
V <sub>DD</sub> .1	V <sub>DD</sub> Power cycling.	v1.0

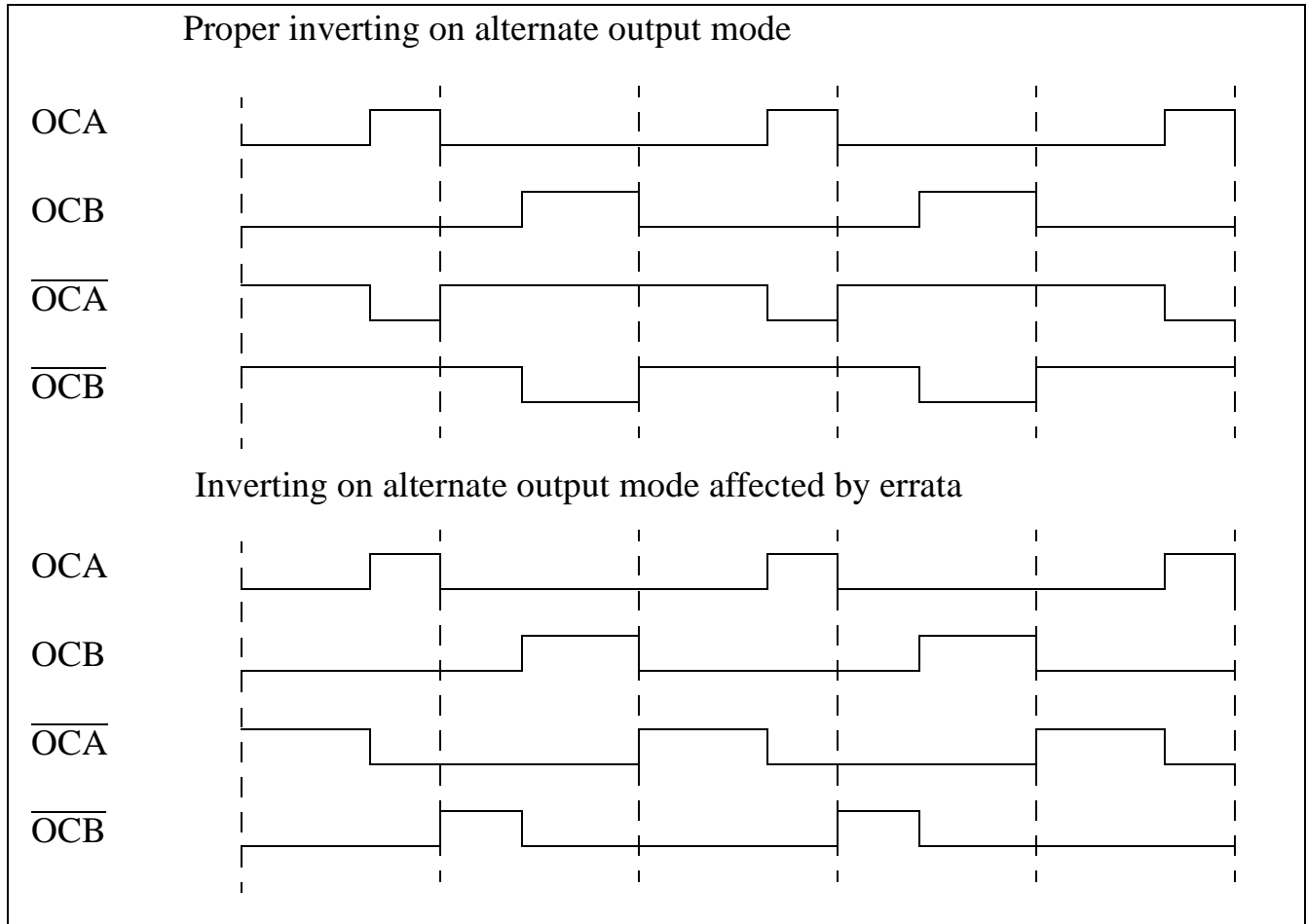
### Functional Deviations of P89LPC935

#### CCU.1: CCU in symmetrical mode when used with CCU prescaler

Introduction: The CCU in the LPC935 is the capture compare unit, which has the option to generate alternate output on 2 PWM signals. All PWM signals can be inverted.

Problem: In the inactive state of the alternate output mode the inverted PWM signal is always low.

Workaround: No known workaround.

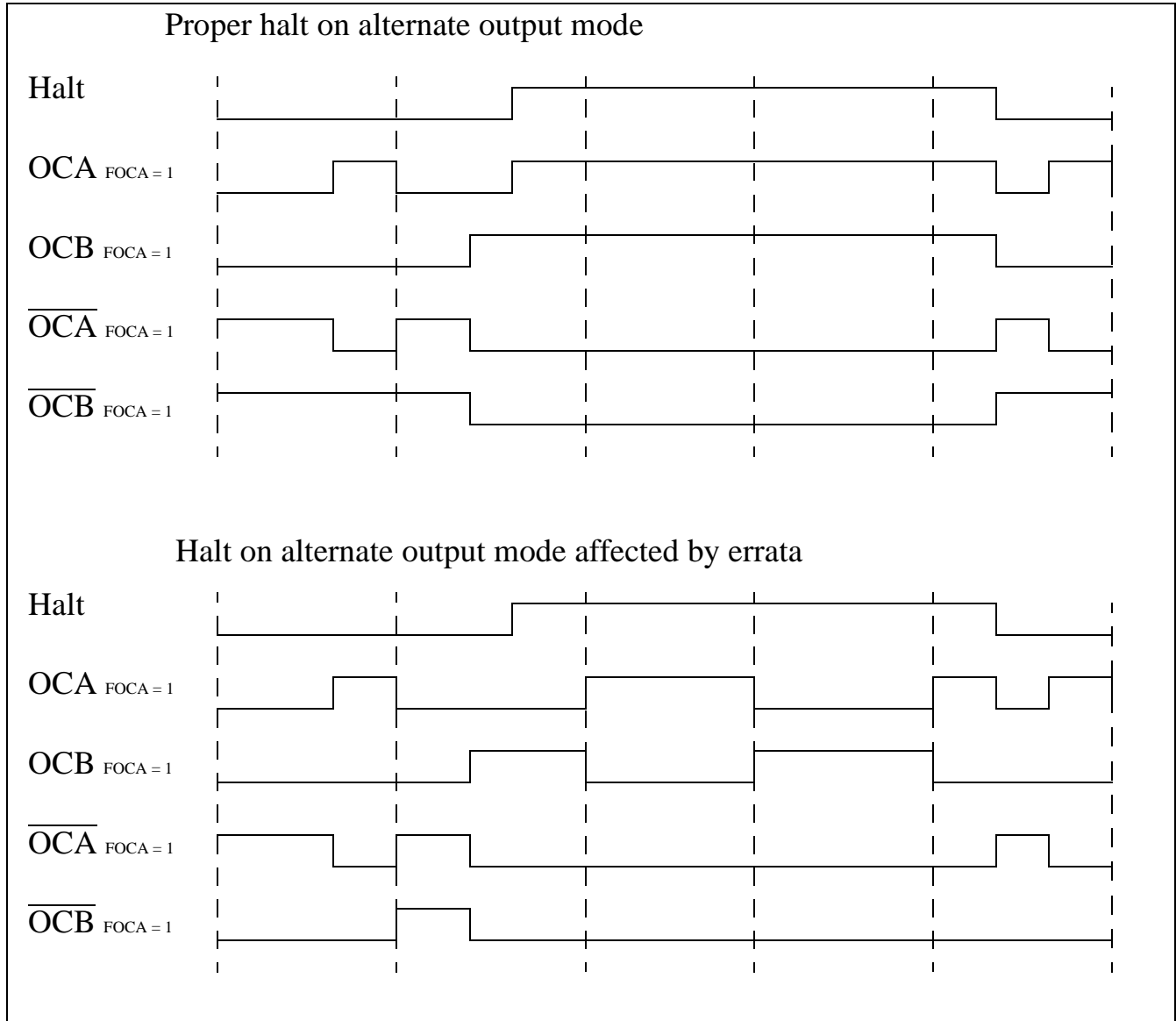


**CCU.2: CCU in Alternate output mode halting**

**Introduction:** The CCU in the LPC935 is the capture compare unit, which has the option to generate alternate output on 2 PWM signals. When a halt condition occurs all the PWM outputs go to the predefined state of FOCx.  
All PWM signals can be inverted.

**Problem:** In the inactive state of the alternate output mode the inverted PWM signal is always low, even during a halt condition.

**Workaround:** No known workaround.



**CCU.3: CCU PLL divider**

**Introduction:** The CCU in the LPC935 is the capture compare unit, which has a PLL to boost the frequency of the CCU block. The PLL has an input range between 0.5 MHz and 1MHz. Different clock dividers such as the DIVM and PLLDIV can be used to get the desired input frequency to the PLL.

**Problem:** When the PLLDIV is selected to divide by 0, the PLL circuit does not lock and output the correct frequency.

**Workaround:** Use a different combination of DIVM and PLLDIV where PLLDIV is not 0.

**CCU.4: CCU capture reading ICRxH**

**Introduction:** The CCU in the LPC935 is the capture compare unit, which has the option to capture external signals on the ICA and ICB channels. The capture event is read out in 2 registers the capture low register ICRxL and ICRxH.

**Problem:** When reading out ICRxH the data will not be correct, the data in ICRxH will be updated after ICRxH is read.

**Workaround:** Read ICRxH twice, the second read of the ICRxH will have the correct data.

**ADC.1: Single Step mode multi channel boundary interrupt**

**Introduction:** The ADC on the LPC935 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

**Problem:** When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. This applies to both ADC0 and ADC1 on the LPC935.

**Workarounds:**

- 1) Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
- 2) Use the default boundary channel, not clear BNDI bit until all channels are converted.

**ADC.2: Timer/Edge trigger with scan mode**

**Introduction:**

The ADC on the LPC935 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Timer / Edge trigger mode where the ADC will generate an ADC start condition on the timer or edge on a pin. Scan mode is an ADC feature where the ADC will scan through all selected channels on an ADC start condition.

**Problem:** When the ADC is in Timer or Edge mode, with scan mode, and more than 1 channel is selected, and the repeat conversion on timer or edge is selected, the channel counter increments to last selected channel on first conversion, but on all subsequent conversion triggers the counter is not reset, so only the last channel is converted over and over again. This applies to both ADC0 and ADC1 on the LPC935.

**Workarounds:**

- 1) To reset the counter that sticks on the last channel the ADC can be disabled and enabled again.
- 2) Switch from ADC mode to DAC mode and back.

**EEPROM.1: EEPROM lock-up on power up**

**Introduction:** The LPC935 has onboard data EEPROM, which allows to store non volatile data bytes on the LPC935 that will hold their value when the power is not applied to the LPC935.

**Problem:** With a slow rising VDD slower than 10ms there is a chance that the EEPROM circuitry will lock up, and incorrect data will be read out.

The EEPROM itself still has the correct data.

**Workaround:** The data EEPROM can be unlocked by a dummy write cycle. The following function shows a dummy write cycle.

```
void dummywrite(void)
{
    DEECON &= 0x0E;           // EEPROM write mode
    DEEDAT = 0x5A;           // dummy data
    DEEADR = 0x00;           // dummy write address 0x000
    while(!(DEECON&0x80))    // wait till interrupt flag is set
    {
    }
}
```

## **Electrical and Timing Specification Deviations of P89LPC935**

**No known errata**

## Errata Notes

### **V<sub>DD</sub>.1: V<sub>DD</sub> Power cycling**

To generate a proper Power-On-Reset (POR), V<sub>DD</sub> must have dropped below 0.2V before being powered back up. Power-cycling without V<sub>DD</sub> having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V<sub>POR</sub> specification in LPC935 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V<sub>DD</sub> must fall below V<sub>POR</sub>.