

# Circuit Sensitivity Analysis in Terms of Process Parameters

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*A new methodology for sensitivity analysis at circuit level in terms of process parameters is presented. Response functions for long-channel MOSFETs are found from process and device simulations. Responses for a device with arbitrary dimensions are subsequently calculated using the MOS MODEL 9 scaling rules.*

## INTRODUCTION

A realistic sensitivity analysis at circuit level in terms of process parameters would necessitate many full 3D process and device simulations, because devices with different geometries ( $W/L$ ) are used. This is far outside the scope of present days simulation packages. In this paper, we describe a new methodology for analyzing the spreads at circuit level by simulating the response surfaces of long-channel transistor only. For the extrapolation of the results of the long-channel devices to devices with arbitrary dimensions, we use the scaling rules of MOS MODEL 9[1]. This allows a quasi-3D analysis without the need to actually perform process and device simulations in three dimensions. The method is verified on a large database of a CMOS process containing the parameter sets of MOSFETs and applied at circuit level by modeling the gate delay of a ring oscillator.

## EXPERIMENTAL

The characteristics of MOSFETs in a CMOS production line were monitored over a long period of time. The database contains more than 11.000 fully characterized sets of MOSFETs. Each set consists of  $n$  and  $p$ -channel devices with various channel lengths. The MM9 parameters of each MOSFET were determined with direct parameter extraction. The 4 most important parameters and the correlations between  $V_t$ 's and gain factors were used for statistical analysis. All transistor parameters are subjected to short-term variations (within one batch) and long-term variations (from batch to batch). In this paper, we analyze the short-term variations. For the analysis at circuit level we have looked at a 21-stage ring oscillator followed by a frequency divider. The ring oscillator was designed with six different geometries for the  $n$  and  $p$ -channel MOSFETs.

## LONG-CHANNEL DEVICES

The basic simulation chain for the determination of the long-channel compact model parameters is depicted in figure 1 [2].

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The NORMAN/DEBORA package[3] is used for the modeling of the response surfaces. The 2D doping profile is constructed using SUPREM3 for the channel and SUPREM4 for the S/D area. For long-channel MOSFETs, fluctuations in the S/D profile are not important for the electrical performance and 1D process simulations for the channel profile are sufficient to examine the fluctuations in the transistor parameters. The  $IV$  characteristics are simulated with MINIMOS4, and the compact model parameters are finally extracted using MOS MODEL 9 (fig. 2).

In total 16 process parameters were varied in the simulations. Included were the temperatures of all furnace anneals, the energies and doses of the implantations and the layer thicknesses. The spreads in the lithography ( $\delta W$  and  $\delta L$  variations) were taken into account, but not used as fitting parameters, because these variations are exactly known from independent calibrations. The problem we face is to find a unique description of the statistics in terms of the process parameters. It is extremely important to take the correlations between the transistor parameters explicitly into account in order to obtain the correct spreads in the process parameters [2]. We are able to identify the five main process parameters responsible for the spreads in the transistor parameters. This is in accordance with principal components analysis, which shows that we have a 5 dimensional parameter space. Table 1 and 2 show the measured and simulated spreads and the correlation coefficients for the long-channel devices using our 'fingerprinting' technique (fig. 4).

## SHORT-CHANNEL DEVICES

The compact MOS model MOS MODEL 9 contains analytical formulas describing the model parameters as a function of the geometry. These formulas are used to calculate the short-channel parameters from the long-channel parameters (table 3). In addition, we can also use these scaling rules to calculate the spread in the short-channel devices.

This is illustrated in figure 5 where we discuss the spread in the short-channel gain factor  $\beta$ . The spread in the gain factor consists of an intrinsic spread  $\sigma(\beta_{\text{long}})$  of a large device and a contribution due to the lithography spread  $\sigma(\text{litho})$ . The  $\sigma(\text{litho})$  has not been fitted, but is taken directly from the database. The spread  $\sigma(\beta_{\text{long}})$  is found from the analysis of the long-channel devices as discussed above. The MM9 scaling rule translates  $\sigma(\beta_{\text{long}})$  and  $\sigma(\text{litho})$  to the final spread  $\sigma(\beta_{\text{short}})$ . Width variations can be accounted for by making use of the scaling rules in the  $W$  direction. Figure 6 illus-

trates our methodology for the threshold voltage  $V_t$ . Notice that it is possible to include the reverse short-channel effect (RSCE), because the  $V_t$  scaling rule of MOS MODEL 9 accounts for  $V_t$  roll-up. The geometry variations of the other transistor parameters are treated in a similar way.

This procedure enables us to find the response surfaces for transistor parameters of a short-channel or narrow-width device in terms of the process parameters without the need to perform 3D numerical simulations.

Table 4 shows the spreads of the short-channel devices. From this table we can conclude that our method can accurately predict the behaviour and spreads of the short-channel devices. Figure 7 depicts the experimental plot of  $I_{sat,n}$  versus  $I_{sat,p}$ . A good agreement with the experiments is observed (see also tables 3 and 4).

### CIRCUIT ANALYSIS

The experimental database as well as the simulations have been described in terms of compact model parameters (figure 2). This allows us to use our results directly into the circuit simulations to obtain response functions at circuit level in terms of the process parameters. The simulation chain is depicted in figure 8. All the simulations – from process simulations to the circuit simulations – are done automatically.

As an example, we have performed a sensitivity analysis of a 21-stage ring oscillator. The experimental spread in the gate delay was obtained from a database containing 2000 characterized ring oscillators. Long-channel MOSFETs are simulated with process and device simulations, and the MOS MODEL 9 scaling rules are subsequently used to translate these long-channel transistor parameters into the parameters of the short-channel and narrow-width devices used in the layout of the ring oscillator. The ring oscillator is a good measure of the intrinsic device performance and can thus be used to test our methodology. We have used the process parameter spreads obtained from the analysis of the long-channel devices to predict the spread in the gate delay. An excellent agreement is observed with the experiments as shown in figure 9.

### CONCLUSIONS

We introduced a new method to describe circuit performance in terms of the process parameters. It is extremely computational efficient because we extract the long-channel transistor parameters from simple process and device simulations and use the scaling rules of MOS MODEL 9 to obtain the response surfaces for devices with arbitrary dimensions. Simple 1D process simulations can thus be used to predict the behaviour of a circuit. The method has been verified on a large industrial database.

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### References

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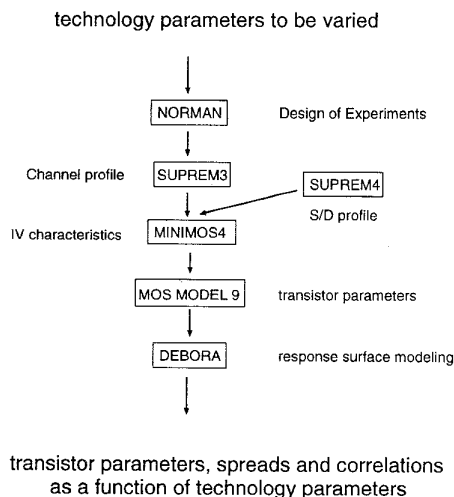


Figure 1: Simulation chain to obtain the spreads in the transistor parameters and the correlation coefficients of the long-channel MOSFETs.

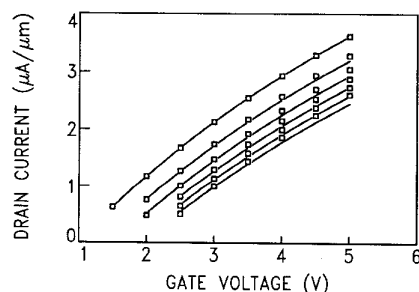


Figure 2: The database as well as the simulations are characterized in terms of MM9 parameters. This allows us to use the response functions for the transistor parameters directly in the circuit simulations. Plot shows the MM9 fit to the characteristics simulated for a long-channel nMOSFET.

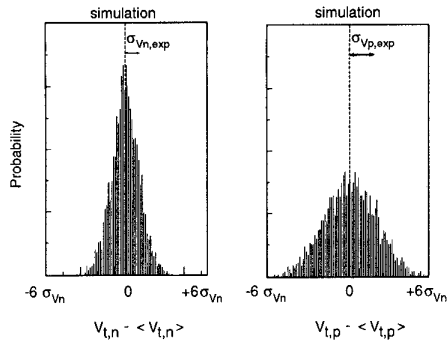


Figure 3: Simulated distributions for long-channel  $V_{t,n}$  and  $V_{t,p}$ . These are simulation results. The experimental spreads are indicated in the figure. Good agreement between simulations and experiment is obtained.

parameter	n MOSFET $\sigma_{SIM}/\sigma_{EXP}$	p MOSFET $\sigma_{SIM}/\sigma_{EXP}$
$\beta$	0.99	1.02
$V_t$	1.19	0.93
K	0.79	1.10
KO	0.97	0.92

Table 1. Ratio of simulated and experimental spread for different long-channel transistor parameters. The parameters included are the gain factors  $\beta$ , the threshold voltages  $V_t$ , and the body factors K and KO (see also fig. 3).

SIMULATED				
	$V_{t,n}$	$V_{t,p}$	$\beta_n$	$\beta_p$
$V_{t,n}$	-	-0.40	-0.54	0.03
$V_{t,p}$		-	0.16	-0.55
$\beta_n$			-	0.61
$\beta_p$				-

EXPERIMENTAL				
	$V_{t,n}$	$V_{t,p}$	$\beta_n$	$\beta_p$
$V_{t,n}$	-	-0.52	-0.44	-0.19
$V_{t,p}$		-	0.03	-0.63
$\beta_n$			-	0.56
$\beta_p$				-

Table 2. Experimental and simulated correlations coefficients between the gain factors and the threshold voltages of the long-channel MOSFETs. The spreads in the process parameters have been fitted to obtain the right correlations and the spreads of the transistor parameters.

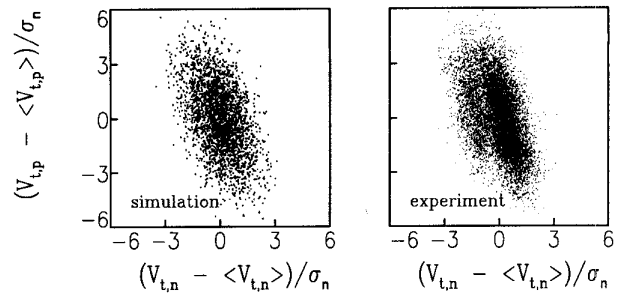


Figure 4: Simulated and experimental spread in long-channel  $V_{t,n}$  and  $V_{t,p}$ . Good agreement exists between the experiments and the simulations. These plots are the 'fingerprints' of the process. A plot like this can easily be generated from the response surfaces.

parameter	n MOSFET $P_{CAL}/P_{EXP}$	p MOSFET $P_{CAL}/P_{EXP}$
$\beta$	1.000	1.001
$V_t$	1.022	0.991
K	1.002	1.001
KO	1.015	0.980
Isat	1.011	1.001

Table 3. Ratio of calculated and experimental transistor parameters for the short-channel devices. These values have been calculated from the simulated long-channel parameters using the MM9 scaling rules. Isat is not a model parameter, but has been included because of its importance to circuit designers.

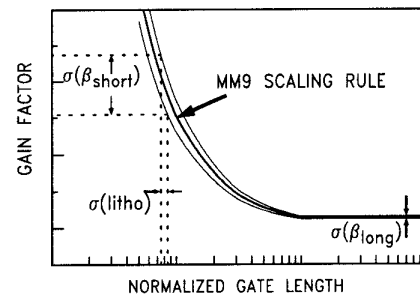


Figure 5: Modeling of the short-channel gain factor. The numerical analysis yields the spread in the long-channel gain factor. The thick line indicates the scaling rule of MOS MODEL 9 for the gain factor. The spread in the short-channel gain factor can be calculated using the long-channel parameter spread in combination with the observed litho spread.

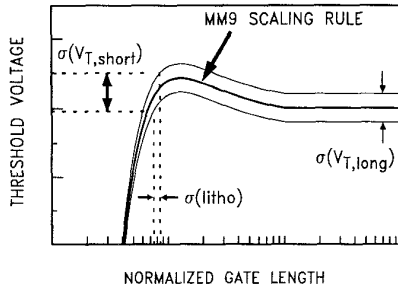


Figure 6: Same figure for the threshold voltage. The MM9 scaling rule for  $V_t$  takes account of the RSCE. This allows us to predict the spread in the short-channel  $V_t$  from the analysis of the long-channel devices.

parameter	n MOSFET	p MOSFET
	$\sigma_{CAL}/\sigma_{EXP}$	$\sigma_{CAL}/\sigma_{EXP}$
$\beta$	0.95	0.73
$V_t$	1.31	1.09
K	0.69	0.73
KO	0.72	0.75
Isat	1.19	0.82

Table 4. Ratio of calculated and experimental spread for different short-channel transistor parameters. These spreads have been calculated from the long-channel parameter spreads using the scaling rules of MOS MODEL 9.

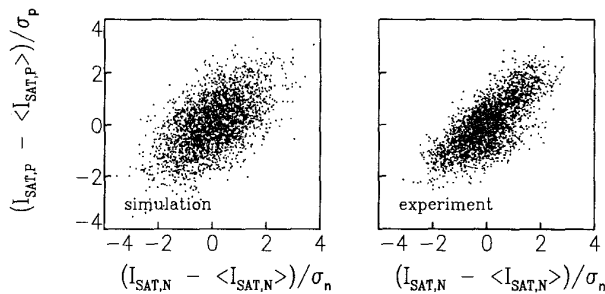


Figure 7: Plot of  $I_{sat}(n)$  versus  $I_{sat}(p)$  of the short-channel devices. Note that the correlation between these two important parameters is correctly predicted from the long-channel sensitivity analysis.

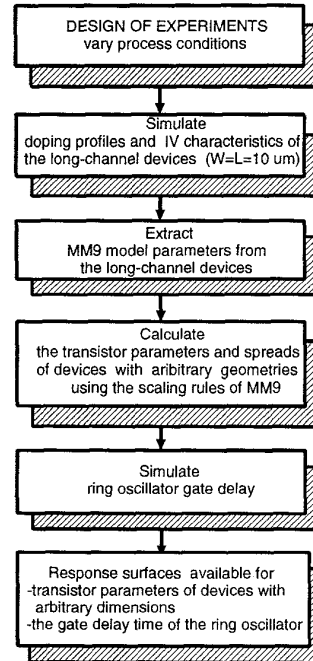


Figure 8: Simulation chain to obtain the spreads in the transistor parameters and the gate delay of the ring oscillator.

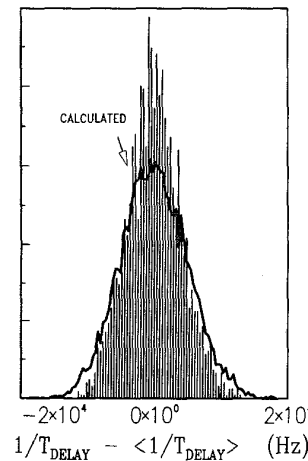


Figure 9: Histogram showing the measured gate delay distribution of a ring oscillator followed by a frequency divider. The solid line has been calculated using the results of the long-channel sensitivity analysis.