

A Large Signal Non-Quasi-Static MOS Model for RF Circuit Simulation

A.J. Scholten, L.F. Tiemeijer, P.W.H. de Vreede and D.B.M. Klaassen

Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands
Phone: +31-40-2742723; Fax: +31-40-2743390; E-mail: andries.scholten@philips.com

Abstract

A large-signal non-quasi-static (NQS) model for RF CMOS circuit simulation is presented that can be built from channel segments described by conventional QS models like BSIM3 or MOS Model 9. This large-signal NQS model is shown to give a very accurate prediction of the high-frequency behaviour of the intrinsic transconductance, the power gain and input resistance.

Introduction

With the scaling towards minimum gate lengths of 0.18 μm and below the use of CMOS has become a serious option in several wireless RF applications previously considered to be the exclusive domain of bipolar and III-V technologies [1, 2]. To facilitate RF CMOS circuit design, RF modelling tools should give an accurate description of quantities like power gain, input impedance and the phase delay between drain current and gate voltage. To achieve this, not only parasitic resistances [3, 4], but also effects of finite channel transit times [3, 5] have to be taken

into account. These so-called non-quasi-static (NQS) effects are included in various small-signal models (see e.g. [6]), which are, however, not suited for large-signal, transient and harmonic-balance simulations. In a large-signal NQS extension of the compact MOS model BSIM3 two Elmore resistors are placed in series with the source-gate and drain-gate capacitances [7]. This approach is computationally efficient, but retains only the lowest pole of the original RC network. Moreover, for the Elmore constant a compromising value between the linear and saturation region has been chosen, which has its impact on the prediction of the input impedance. In **this paper** we *i*) investigate the method of building a large-signal NQS model by breaking down the MOSFET into N equal channel segments in series, *ii*) solve the problems with short-channel effects associated with it [7], *iii*) investigate the optimum choice of N by comparison with high-frequency measurements, and *iv*) assess the computational efficiency.

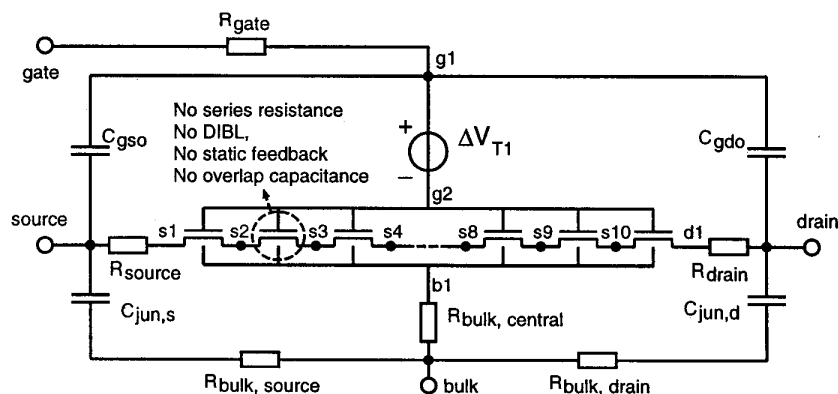


Figure 1: Equivalent circuit of the large-signal NQS model with 10 channel segments. Each segment is modelled by MOS Model 9. The parameters of all channel segments are identical. The source and drain series resistances have been removed from the mobility reduction parameters and are taken into account externally. The drain-induced barrier-lowering (DIBL), static feedback and the overlap capacitances are put equal to zero in each channel segment. DIBL and static feedback are accounted for by an external voltage source at the gate, $\Delta V_{T1} = -\gamma_0 \frac{V_{GTx}^2}{V_{GTx}^2 + V_{GT1}^2} V_{d1s1} - \gamma_1 \frac{V_{GT1}^2}{V_{GTx}^2 + V_{GT1}^2} V_{d1s1}^{nos}$ (see [8]). Also the overlap capacitances are taken into account externally. Note that also parasitic gate and bulk resistances have been added [4].

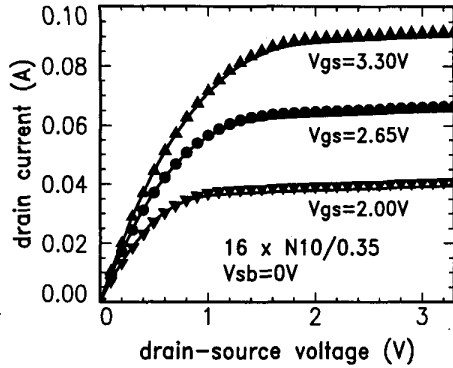


Figure 2: Saturation region of a $0.35 \mu\text{m}$ NMOS device; symbols represent normal MM9 simulations, lines represent the large-signal NQS model with 10 channel segments.

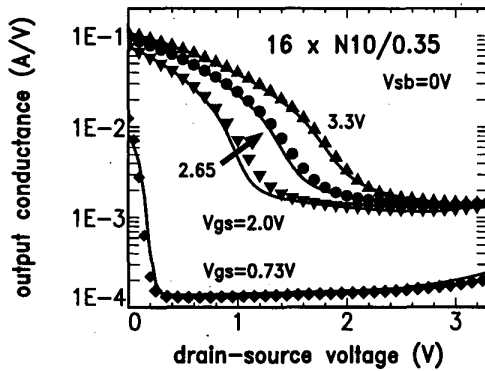


Figure 3: Output conductance of a $0.35 \mu\text{m}$ NMOS device; symbols represent normal MM9 simulations, lines represent the large-signal NQS model with 10 channel segments.

Equivalent circuit of large-signal NQS model and parameter extraction

The equivalent circuit of our large-signal NQS model is given in fig. 1. Each channel segment is modelled by MOS Model 9 (MM9) [8]. Drain-induced barrier-lowering and static feedback are modelled by an external voltage source. This procedure can be applied to any compact MOS model (e.g. BSIM3), which incorporates both effects in an effective gate voltage. No additional parameters have been introduced. All parameters have identical values for each channel segment and are extracted from DC measurements following the same procedure as for the QS model. Using this procedure currents in all operating regions and output conductance are described as accurately as with the QS model (see figs. 2 and 3).

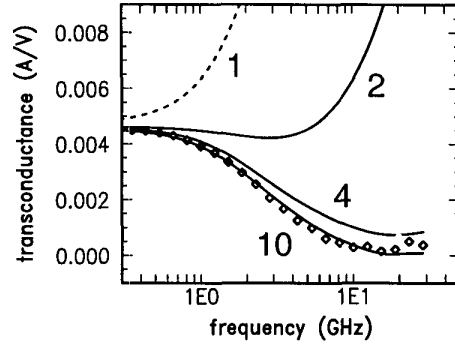


Figure 4: Intrinsic transconductance, $|Y_{dg} - Y_{gd}|$, versus frequency for a $16 \times 10/4$ NMOS device ($V_{DS}=3.3\text{V}$; $V_{GS}=1.5\text{V}$). Symbols represent measurements; lines represent simulations with the QS model (dashed line) and large-signal NQS model (solid lines). The number of channel segments is indicated.

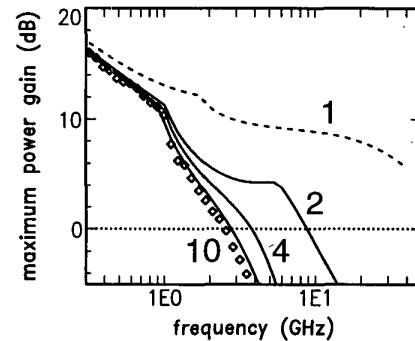


Figure 5: Maximum power gain, G_{msg} and G_{max} , versus frequency for a $16 \times 10/4$ NMOS device ($V_{DS}=3.3\text{V}$; $V_{GS}=1.5\text{V}$). Symbols represent measurements; lines represent simulations with the QS model (dashed line) and large-signal NQS model (solid lines). The number of channel segments is indicated.

High-frequency verification

High-frequency measurements on a number of devices from a $0.35 \mu\text{m}$ CMOS technology have been performed using well-known procedures (see e.g. [4]). As benchmarks for the high-frequency behaviour of the large-signal NQS model intrinsic transconductance, maximum power gain and input resistance are used. From figs. 4 to 6 it can be seen that for $N = 4$ already a reasonable agreement between measurements and simulations is obtained, while for $N = 10$ the agreement is perfect. The cut-off frequency, f_T , for this device with a gate length of $4 \mu\text{m}$,

7.3.2

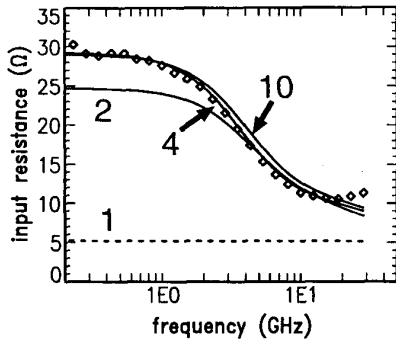


Figure 6: Input resistance, $\text{Re}(Y_{gg}^{-1})$, versus frequency for a $16 \times 10/4$ NMOS device ($V_{DS}=3.3\text{V}$; $V_{GS}=1.5\text{V}$). Symbols represent measurements; lines represent simulations with the QS model (dashed line) and large-signal NQS model (solid lines). The number of channel segments is indicated.

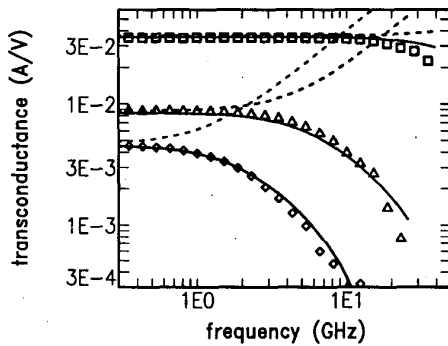


Figure 7: Intrinsic transconductance, $|Y_{dg} - Y_{gd}|$, versus frequency for a $16 \times 10/4$ (diamonds), a $16 \times 10/2$ (triangles) and a $16 \times 10/0.35$ (squares) NMOS device ($V_{DS}=3.3\text{V}$; $V_{GS}=1.5\text{V}$). Dashed line: MM9; solid line: large-signal NQS model with 10 channel segments.

is 360 MHz ($V_{DS}=3.3\text{V}$; $V_{GS}=1.5\text{V}$). Consequently, it can be concluded that an accurate description has been obtained up to frequencies well above $10 \times f_T$. As a next step we compared simulations using the large-signal NQS model with $N = 10$ with measurements for a number of channel lengths (see figs. 7 to 9). Accurate predictions of intrinsic transconductance, power gain and input resistance have been obtained, which are a large improvement over the QS results.

Parameter scaling and short-channel effects

To use this approach in a circuit simulator, it is important that the parameters of the channel segments follow the scaling

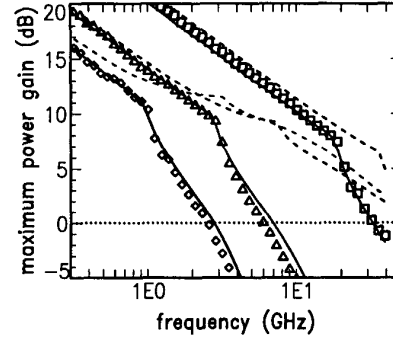


Figure 8: Maximum power gain, G_{msg} and G_{max} , versus frequency for a $16 \times 10/4$ (diamonds), a $16 \times 10/2$ (triangles) and a $16 \times 10/0.35$ (squares) NMOS device ($V_{DS}=3.3\text{V}$; $V_{GS}=1.5\text{V}$). Dashed line: QS model; solid line: large-signal NQS model with 10 channel segments.

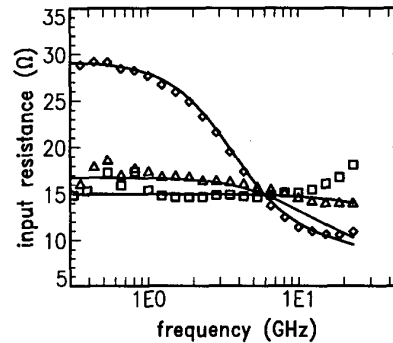


Figure 9: Input resistance, $\text{Re}(Y_{gg}^{-1})$, versus frequency for a $16 \times 10/4$ (diamonds), a $16 \times 10/2$ (triangles) and a $16 \times 10/1$ (squares) NMOS device ($V_{DS}=3.3\text{V}$; $V_{GS}=1.5\text{V}$). Solid line: large-signal NQS model with 10 channel segments.

rules of the QS model, that is used to describe the individual segments. From fig. 10 it can be seen that the MM9 scaling rules give a good description, even though the segment length at the minimum gate length is only 25 nm. Consequently it can be concluded that any problems with artificial short-channel effects (see [7]) are adequately solved.

Computational efficiency

In order to investigate the computational efficiency of the NQS model, transient simulations for a mixer based on a 6-transistor Gilbert cell, designed in $0.25 \mu\text{m}$ CMOS technology, have been performed for a varying number of channel segments, N . The computation time has been found to increase less than proportional with N (slope ≈ 0.8). Pushing the input frequen-

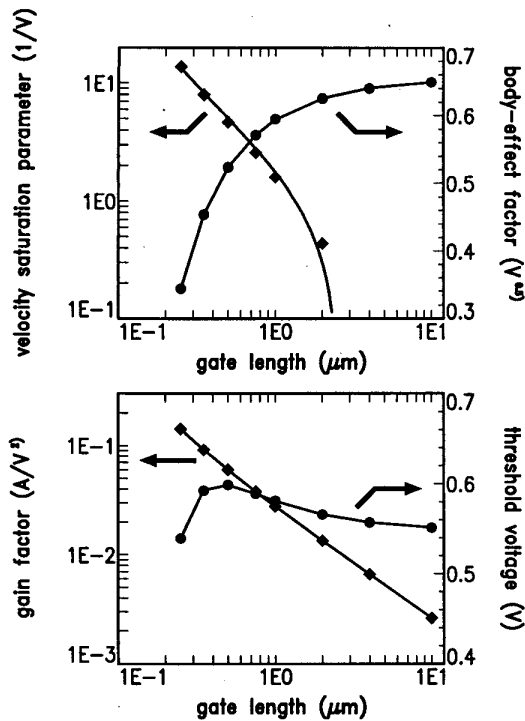


Figure 10: Threshold voltage, gain factor, body-effect factor and velocity saturation parameter of the individual channel segments for a $0.25 \mu\text{m}$ CMOS technology as a function of the gate length. Symbols represent the miniset parameters and lines represent the MM9 scaling rules. Note that 10 channel segments have been used for each gate length.

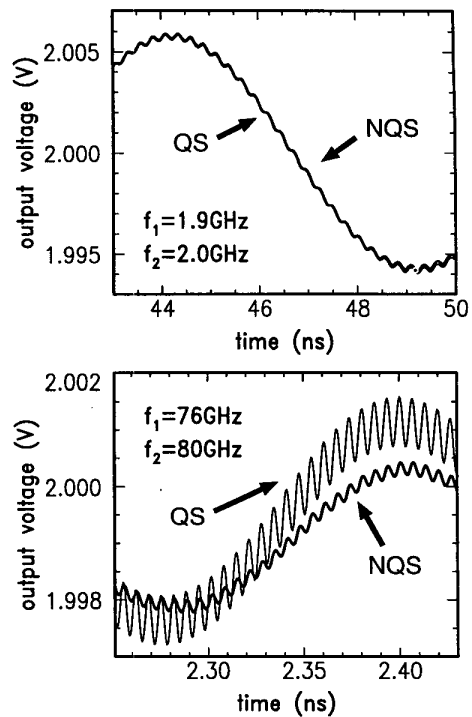


Figure 11: Output of a mixer based on a 6-transistor Gilbert cell, at low (top) and high (bottom) frequency simulated with both the QS and NQS models. Whereas at low frequency both models give identical results, at high frequency the NQS model yields smaller amplitudes for the output signal at both the difference and sum frequencies of the input frequencies.

cies to values far above the cut-off frequency of the $0.25 \mu\text{m}$ MOSFETs yields differences in the signal amplitude at the difference frequency of the input frequencies (see fig. 11). Note that the difference between the QS and NQS models is even larger at the sum frequency, which is due to the wrong frequency dependence of the transconductance in the QS model (see fig. 7).

Conclusions

In this paper a large-signal NQS model for RF CMOS circuit simulation has been presented that gives a very accurate prediction of the high-frequency behaviour of the intrinsic transconductance, the power gain and input resistance. This NQS model can be built from channel segments described by conventional QS models like BSIM3 or MM9, without introducing artificial short-channel effects. Keeping in mind that in RF circuits only a limited number of transistors are crucial for the high-frequency performance, the trade-off between this high accuracy and the computational penalty is very positive.

References

- 1) P. Baltus, Tech. Dig. VLSI Symp., pp. 9-13, Taiwan (1997).
- 2) H.S. Momose et al., Tech. Dig. IEDM-96, pp. 105-108 (1996).
- 3) W. Liu et al., Tech. Dig. IEDM-97, pp. 309-312 (1997).
- 4) L.F. Tiemeijer and D.B.M. Klaassen, Tech. Dig. ESSDERC-98, pp. 480-483 (1998).
- 5) L.F. Tiemeijer et al., Tech. Dig. ESSDERC-99, pp. 652-655 (1999).
- 6) T. Smedes and F.M. Klaassen, Solid-State Electr., Vol. 38, pp. 121-130 (1995).
- 7) M. Chan et al., IEEE Trans. Electron Dev., Vol. 45, pp. 834-841 (1998).
- 8) MOS Model 9 documentation and source code: http://www.semiconductors.philips.com/Philips_Models/