

# **ERRATA SHEET**

**Date:** 2003 Aug 01  
**Document Release:** Version 1.0  
**Device Affected:** P89LPC912

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2003 Aug 01



**Identification:**

The typical P89LPC912 devices have the following top-side marking:

P89LPC912x x  
xxxxxxx xx  
xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC912:

Revision Identifier (R)	Comment
'_'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

**Errata Overview - Functional Problems**

Functional Problem	Short Description	fixed in revision	added
I/O.1	Port Configuration	none	v1.0
I/O.2	Port 2.4 can draw additional power	none	v1.0
ICP.1	ICP Global Erase	none	v1.0

**Errata Overview - AC/DC Deviations**

AC/DC Deviation	Short Description	fixed in revision	added
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## Functional Deviations of P89LPC912

### I/O.1: Port Configuration

**Introduction:** The I/O ports of the LPC912 can be configured to 4 different modes by writing to the PxM1 and PxM2 registers. The default mode after Reset is "Input Only".

**Problem:** Coming out of Reset, the LPC912 port registers should be initialized as follows. Without executing this sequence, the LPC912 could consume additional power.

**Workaround:** Initialize the LPC912 ports in two steps:

Step 1: Configure all port registers with this initialization.

```
P0M1 = 0x00;           // set P0 to quasi-bidirectional
P1M1 = 0x00;           // set P1 to quasi-bidirectional
P2M1 = 0x00;           // set P2 to quasi-bidirectional
P3M1 = 0x00;           // set P3 to quasi-bidirectional
```

Step 2: Configure the port pins on the LPC912 to their required mode using only AND and OR operations. Make sure to modify only the port pins available on the LPC912.

### I/O.2: Port 2.4 can draw additional power

**Introduction:** Port 2.4 is a general purpose I/O pin.

**Problem:** P2.4 always has an active internal pull-up, which will draw additional power when the port is written low.

**Workaround:** No known workaround.

### ICP.1: ICP Global Erase

**Introduction:** The LPC912 can be programmed using ICP (In Circuit Programming). One of the ICP functions is the Erase Global command, which will erase the entire chip including the security bytes and configuration information.

**Problem:** When giving the Erase Global command through the ICP interface the LPC912 will not clear the busy flag and stay busy forever.

**Workaround:** The workaround can be done in 4 steps:

Step 1: Shift out the WR\_FMCON command followed by the Erase Global opcode.

Step 2: Wait 5ms.

Step 3: Do 8 dummy reads with the RD\_FMDATA\_I command.

Step 4: Read FMCON until the busy flag gets cleared.

Please also see figure 1 on the following page.

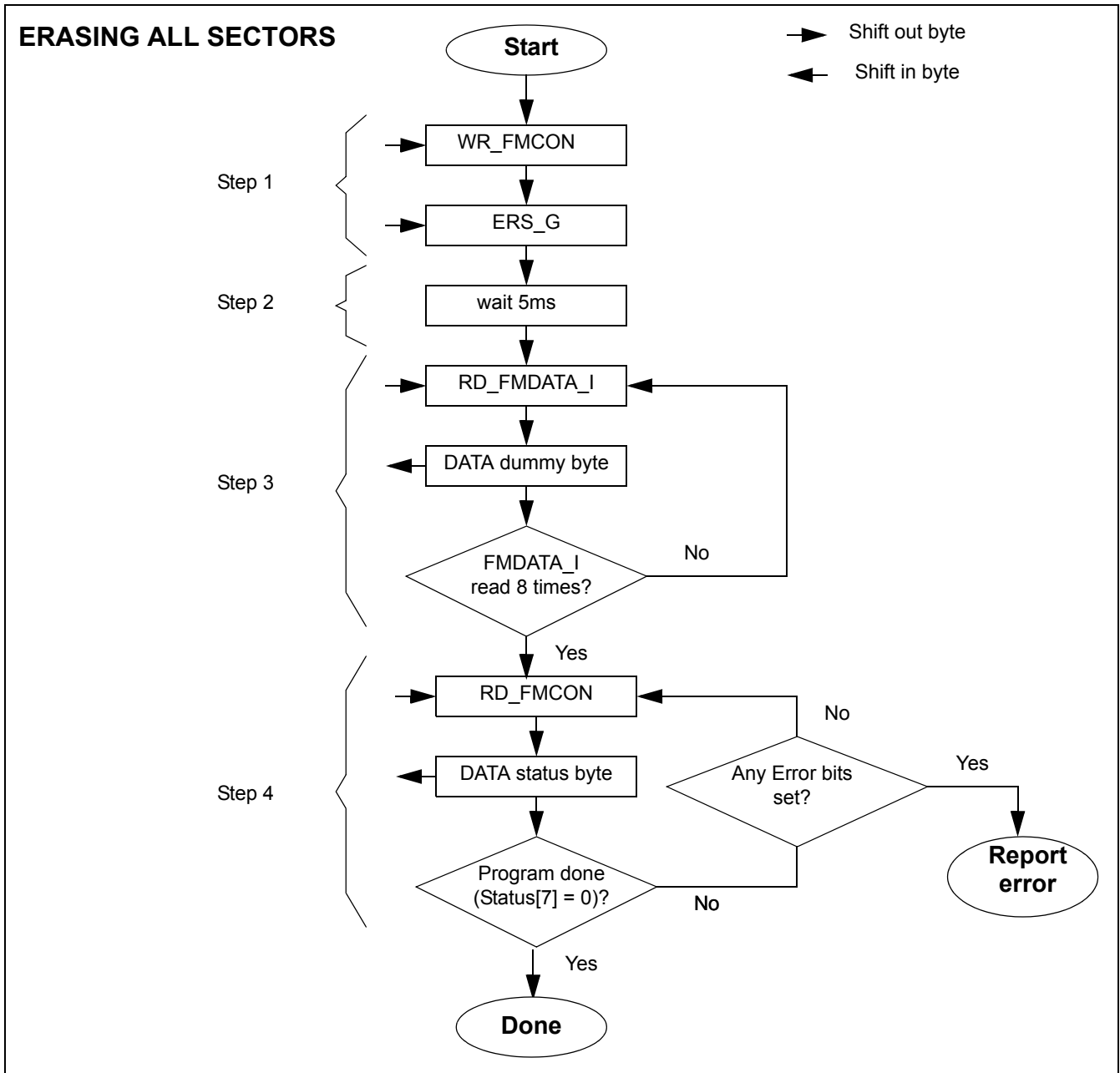


Figure 1: Flowchart ICP Global Erase

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## **Electrical and Timing Specification Deviations of P89LPC912**

No known erratas.