

## Fail-Safe System Basis Chips UJA106x

# Taking the complexity out of automotive networking

Comfort, convenience and safety are driving factors in today's automotive market. This means more electronics and more complex automotive networks in every car model. Further complicating designs, each individual electronic control unit (ECU) and / or node within a network has its own unique requirements. Until now, manufacturers have been faced with a multitude of solutions based on proprietary variants with resulting high development and implementation costs.

### The SBC family

- ▶ UJA1061 – ISO 11898-3 compliant Fault-Tolerant CAN and LIN2.0 compliant SBC
- ▶ UJA1065 – ISO 11898-2 compliant High-Speed CAN and LIN2.0 compliant SBC
- ▶ UJA1066 – ISO 11898-2 compliant High-Speed CAN SBC
- ▶ UJA1069 – LIN2.0 compliant SBC

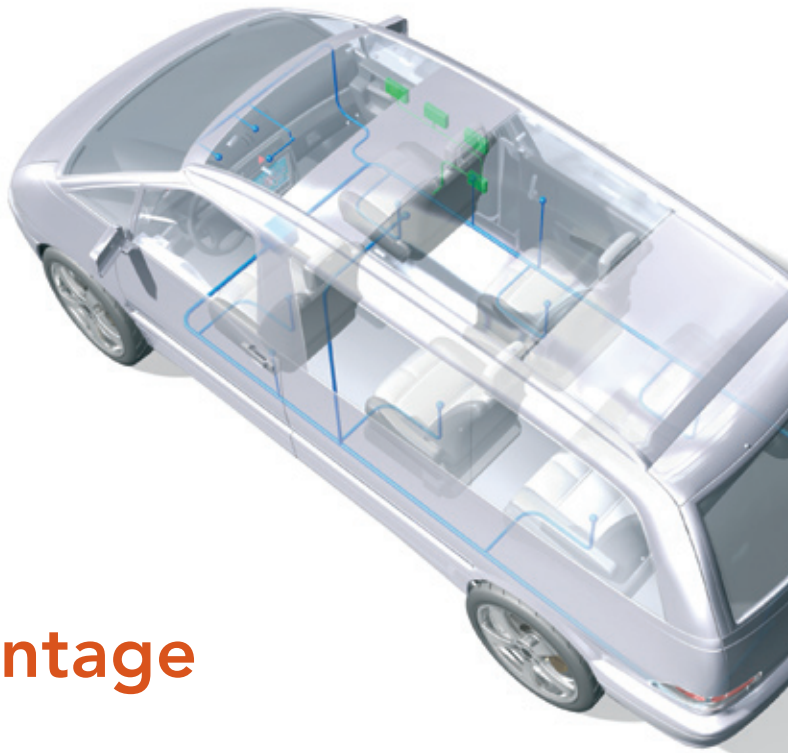
### Key features

- ▶ Family of SBCs compliant with LIN 2.0 and / or ISO11898 CAN
- ▶ Excellent EMC performance
- ▶ Low sleep current – typically 50  $\mu$ A
- ▶  $\pm$ 8 kV ESD protection and excellent robustness
- ▶ Support for 12 and 24 V systems
- ▶ Small-footprint HTSSOP32 package with low thermal resistance

### Key benefits

- ▶ Quick and easy development of robust, fail-safe ECUs
- ▶ Lower development risk and costs for both vehicle manufacturers and module makers
- ▶ Easy to switch between different physical layers (e.g. FT-CAN and HS-CAN)
- ▶ Support for a wide range of microcontrollers (3.0, 3.3 and 5.0 V), maximizing flexibility and reducing costs
- ▶ Flexible network design due to partial networking capability
- ▶ Reduced ECU size

NXP makes it easy and more cost-effective for car manufacturers to design and build today's complex networks. As a leader in automotive network solutions, we have used our experience to intelligently integrate the common functionality required for an ECU into a single, compact chip. More importantly, we have taken a platform approach that maximizes hardware and software re-use across a complete family of Fail-Safe System Basis Chips (SBCs). It is this platform approach that ensures we help you develop lower-cost CAN / LIN networks.

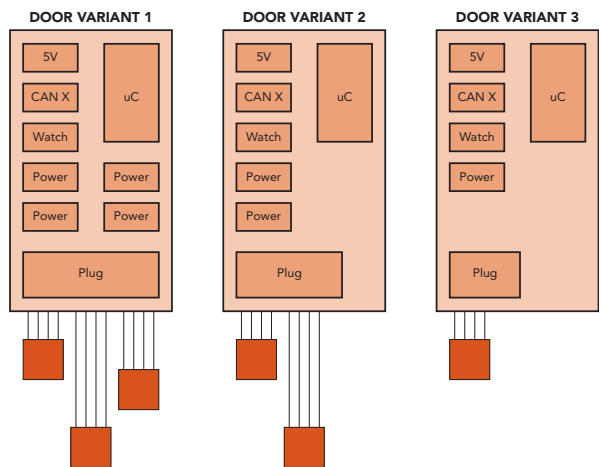


Our Fail-Safe SBCs are highly integrated System-on-Chip (SoC) solutions for automotive network systems, addressing the trend for increased network complexity and functionality. Offering the most extensive feature list in the industry, they greatly simplify design and implementation of ECUs, especially for applications operating under 'ignition-off' conditions. These Fail-Safe SBCs combine LIN and /or CAN transceivers, two LDO voltage regulators, an SPI, a watchdog and many diagnostics features on a single chip. And thanks to NXP' third-generation Silicon-on-Insulator (SOI) process, they deliver outstanding EMC performance.

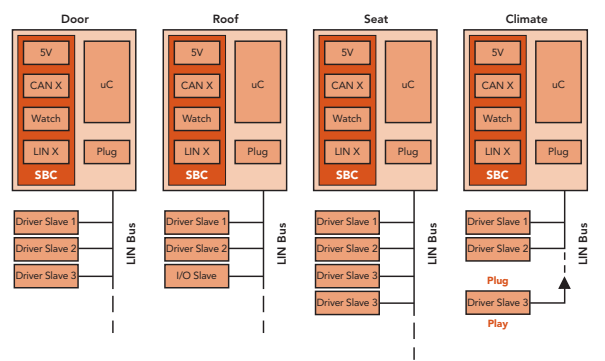
# NXP's platform advantage

What is the platform advantage? By ensuring an integrated and standardized approach to ECU design, our family of Fail-Safe SBCs greatly simplifies implementation of complex CAN / LIN networks. In fact, once you have developed one implementation it is easy to develop others for any car model. With a range of fully interchangeable products covering High-Speed CAN, Fault-Tolerant CAN and LIN protocols, all that is needed to switch between physical layers is to just swap from one SBC to another. The rest of the PCB and even your software can remain the same. And by using the same pinning and software interface, with a high level of re-use, time-to-market is also significantly reduced.

To achieve this standardized family, NXP has taken a mechatronic approach to ECU design that delivers a number of inherent advantages. Distributing power onto the actual node eliminates the need for large power connectors on the ECU. This helps simplify the overall design of the ECU and also reduces ECU size and cost. Additionally, specific customer or application features can simply be plugged into the LIN network without having to go through an expensive redesign of the ECU.



Non-standardized approach



Standardized, mechatronic approach using NXP's Fail-Safe SBC family

It is not just ease of design-in where our Fail-Safe SBCs excel. They also incorporate critical fail-safe and diagnostic functions – a feature set unique to NXP. A fully integrated fail-safe system controller ensures any conceivable local ECU failure stays local, while an extensive set of SPI readable diagnostic features provides detection, detailed reporting and rigorous error handling on CAN and LIN bus failures.

## Safe under all conditions

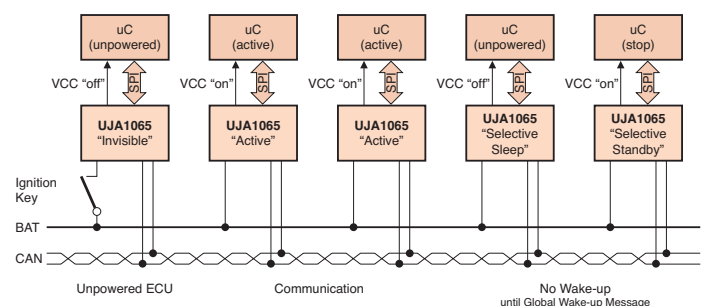
The extensive set on-chip of SPI readable diagnostics features allows rigorous error handling. Detection and detailed error reporting on CAN and LIN bus failures (e.g. shorts to GND/BAT, open bus wires etc.) ensure any failure can be easily handled, while TxD dominant and RxD recessive clamping as well as RxD to TxD short detection prevent bus deadlocks.

A host of features to ensure robust system operation are available including, ECU two-level ground-shift detection, over-temperature warning, ECU battery monitoring (for example to detect chattering battery contact or to save data before microcontroller power down) and signaling of potential RAM-retention errors due to low microcontroller  $V_{CC}$ . Other features include guaranteed ramp down of the microcontroller voltage in case of a soft restart, detection of cyclic ECU problems and Global Enable pin to control safety critical hardware.

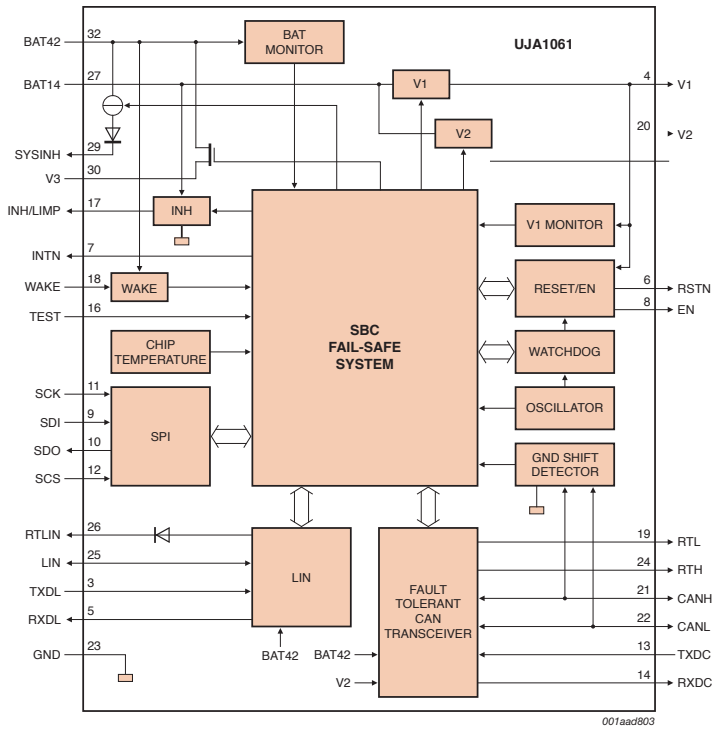
If a failure condition occurs the SBC will detect, report and ultimately switch to a low-power fail-safe mode, reducing power consumption and interference with the rest of the network. This is an important factor with the increasing number of bus nodes in today's cars. At the same time,

alternative application hardware can be activated to enable a 'limp home' capability. The result – no more drained batteries for parked cars, or potentially dangerous network deadlocks.

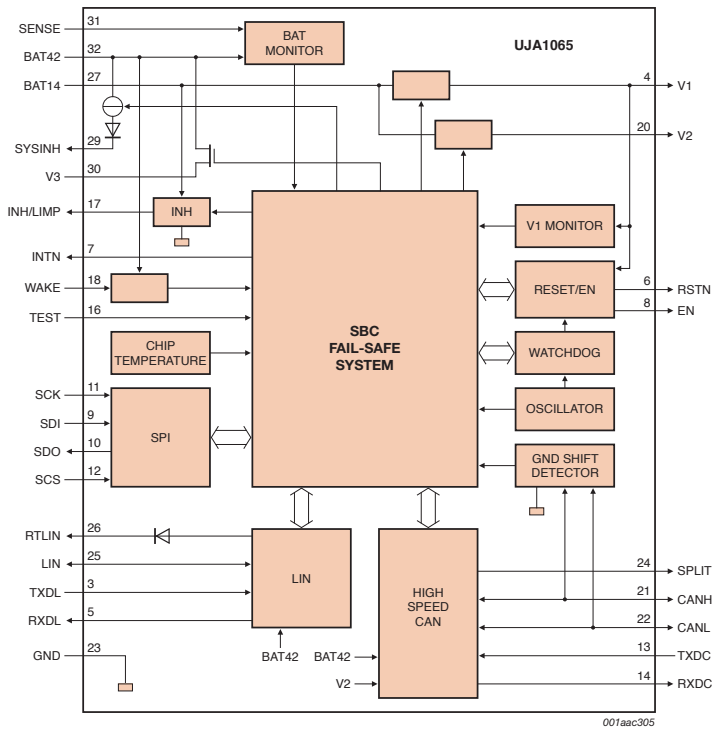
Our Fail-Safe SBC family also incorporates a selective sleep mode offering a versatile way to create partial networks. This function allows traffic to continue between nodes that must remain active, for instance central locking, without disturbing the rest of the network when the ignition is switched off. All that is required to re-activate nodes in Selective Sleep is a simple 'wake-up' message. This further reduces overall power consumption, especially under 'ignition-off' conditions. What's more, integrating Selective Sleep into existing networks is simplicity itself. Just add an NXP Fail-Safe SBC where you need partial networking capability and the rest of the network can stay the same.



Selective sleep mode



Block diagram UJA1061



Block diagram UJA1065