



# NXP 208-MHz, 32-bit ARM926EJ-S processor LPC32x0

## ARM9 MCUs with up to 256-KB SRAM, Ethernet, USB, and LCD controller

These advanced microcontrollers use a powerful ARM926EJ-S core, a VFP coprocessor, an internal bus matrix, and a large set of standard peripherals to achieve outstanding performance.

### Key features

- ▶ 208-MHz, 32-bit ARM9EJ-S with Embedded Trace Module (ETM)
- ▶ Vector Floating Point coprocessor
- ▶ 90-nm technology for operation down to 0.9 V in low-power mode
- ▶ Up to 256 KB of internal SRAM and 32 KB I-cache/32 KB D-cache
- ▶ External memory controller for DDR and SDR SDRAM, SRAM, and Flash
- ▶ Selectable boot-up from NAND Flash, SPI memory, UART, or static memory
- ▶ 10/100 Ethernet MAC with dedicated DMA controller (LPC3240 & LPC3250 only)
- ▶ USB OTG with full-speed host and device capabilities
- ▶ 24-bit LCD controller with dedicated DMA controller supports STN and TFT panels (LPC3230 & LPC3250 only)
- ▶ Three-channel, 10-bit A/D converter with touch-screen interface
- ▶ Comprehensive set of serial interfaces (two I<sup>2</sup>S, two SPI, two SSP, two I<sup>2</sup>C-bus, and seven UARTs)
- ▶ SD memory-card interface
- ▶ Six 32-bit timers, Watchdog timer, 11 PWM channels, and real-time clock with separate clock and power domain
- ▶ 8-channel, general-purpose DMA controller
- ▶ Keyboard-scan interface for 8 x 8 keys and up to 87 GPIO
- ▶ JTAG interface with emulation trace buffer
- ▶ Core voltage = 1.2 V, I/O = 1.8, 2.8, and 3.0 V
- ▶ TFBGA296 package (15 x 15 x 0.8 mm)

### Applications

- ▶ Consumer
- ▶ Medical
- ▶ Industrial
- ▶ Automotive
- ▶ Network control
- ▶ Communication

Built around a 90-nm, 208-MHz ARM926EJ-S CPU core and a Vector Floating Point (VFP) coprocessor, the NXP LPC32x0 family is designed for applications that require high performance, high integration, and low power consumption.

The VFP coprocessor increases the speed of typical calculations by a factor of four to five in scalar mode, and much more in optimized vector mode. Advanced process technology optimizes each microcontroller's intrinsic power, and software-controlled features provide best-in-class power management. Each LPC32x0 microcontroller has up to 256 KB of internal SRAM, and an external memory controller that supports DDR and SDR SDRAM, SRAM, Flash, and static devices. The external-memory controller can boot-up from NAND Flash, SPI memory, UART, or SRAM. On the LPC3230 and the LPC3250, there is also



a flexible LCD controller that supports STN and TFT panels, and offers a dedicated DMA controller and programmable display resolution up to 1024 x 768 and up to 16 M colors.

Multiple interfaces for serial communications increase design flexibility, provide larger buffer size, and deliver higher processing power. The LPC3240 and LPC3250 microcontrollers have a 10/100 Ethernet MAC with a dedicated DMA controller. Every LPC32x0 microcontroller also has a USB interface that supports device, host, and On-The-Go (OTG) operation. There are four standard 16C550 UARTs (one supports IrDA), three high-speed (up to 921,600 bps) UARTs, two Fast I<sup>2</sup>C-bus (400 Mbps) interfaces with slave, single, and multi-master support, two SPI/SSP ports, and a function for automatic keyboard scanning that supports 8 x 8 keys. There are also two I<sup>2</sup>S interfaces, each with separate input and output channels. Each channel can be operated independently on three pins, or, with only four pins, the input and output of one I<sup>2</sup>S interface can be used.

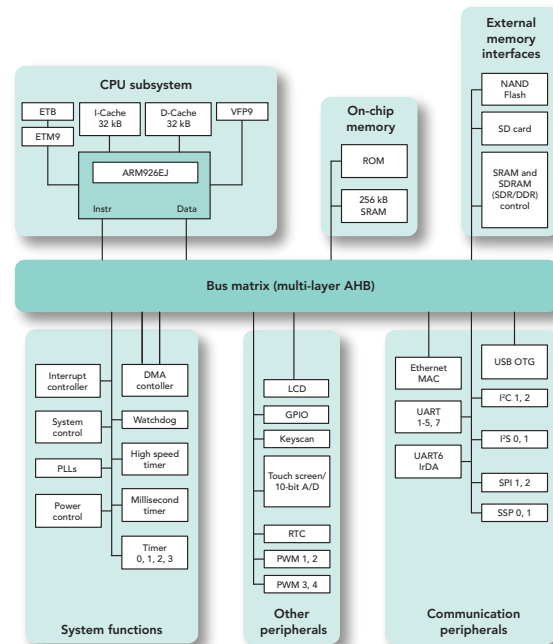
Each LPC32x0 microcontroller has a 10-bit, 400-kHz A/D converter with three channels and a touchscreen interface, five 32-bit timers with capture/compare channels, a 32-bit timer driven by the real-time clock, eleven PWM channels, and a Watchdog timer. There is also a real-time clock with a separate clock and power domain, a dedicated 32-kHz oscillator, a Secure Digital (SD) interface, and an integrated interrupt controller that supports up to 73 interrupt sources.

Data movement is managed by an eight-channel, general-purpose DMA controller that can be used with SD ports, UARTs, I<sup>2</sup>S ports, SPI interfaces, or memory-to-memory transfers.

A seven-layer, 32-bit, 104-MHz AHB matrix provides a separate bus for each of the seven AHB masters (D-cache, I-cache, two DMA, Ethernet MAC, USB controller, and LCD controller). This eliminates arbitration delays, except when two masters attempt to access the same slave at the same time.

### Selection guide for LPC32x0 family

Type	SRAM (KB)	A/D converter (channel x bit)	10/100 Ethernet	LCD controller	USB host, device, OTG	Serial interfaces				Temperature range (°C)	Package
						I <sup>2</sup> C-bus	SPI/SSP	I <sup>2</sup> S	UART		
LPC3220	128	3 x 10	0	0	1	2	2	2	7	-40 to +85	TFBGA296
LPC3230	256	3 x 10	0	1	1	2	2	2	7	-40 to +85	TFBGA296
LPC3240	256	3 x 10	1	0	1	2	2	2	7	-40 to +85	TFBGA296
LPC3250	256	3 x 10	1	1	1	2	2	2	7	-40 to +85	TFBGA296



LPC3250 block diagram

An on-chip PLL lets the CPU operate up to its maximum rate without a high-frequency crystal. A second PLL enables operation from the 32-kHz real-time clock instead of the external crystal.

The core voltage supports 1.2 V, while the I/O ports support 1.8, 2.8, and 3.0 V. The operating temperature range -40 to +85 °C. In ultra-low power mode, the core operates down to 0.9 V.

For debugging, LPC32x0 microcontrollers use a JTAG interface with a 2K x 24-bit emulation trace buffer and supports real-time emulation.

### Third-Party Development Tools

Through third-party suppliers, we offer a range of development and evaluation tools for our microcontrollers. For the most current listing, please visit [www.nxp.com/microcontrollers](http://www.nxp.com/microcontrollers).