

## *Self Qualification Results*

*Matte Sn + postbake leadfree solution for*

*Products with Copper based lead-frames*

- *HSOP20 packages with glue die-attach, assembled in Philips Semiconductors Kaohsiung.*

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## 1. Introduction

The intention of the change to Pb-free packages from Philips has been announced in the Advance CPCN for Pb-free, issued in May 2003, CPCN # 200305025.

The final CPCN will be issued in different phases, each phase showing qualification results of a certain group of packages.

This self qualification report presents an overview of the qualification data completed to release a group of packages to be assembled in matte Sn + postbake solution.

This report covers the results of :

- HSOP20 packages (glue die-attach versions) assembled in Philips Semiconductors Kaohsiung.

In order to validate assembly quality and reliability, a self-qualification program has been performed. The results of this qualification demonstrate that Philips Semiconductors can achieve distinctive assembly quality with equal or better product quality and reliability when compared to the lead-tin plated versions of these products.

With the introduction of matte Sn as Pb-free solution, the Bill of Materials (BoM) of the mentioned packages is fully compliant to the RoHS legislation requirements.

## 2. Assembly Facilities

### *PSK*

Philips Semiconductors Kaohsiung is the first organization set up in the Republic of China by Philips Electronics in 1966. In 1969 the IC assembly started in the Nantze Export Processing Zone ("Nantze EPZ") in Kaohsiung, Taiwan. At present the floor space is 49,000 square meters and the total number of employees is 2700.

Package family portfolio and test capabilities of PSK consists of DIP, SILP, SO, VSO, HSOP, QFP and BGA.

PSK has received Ford TQE (Total Quality Excellence) award, ISO9002, ISO900 and ISO140001 certification. In 1997 PSK received QS-9000 certification and the Japan Quality Medal.

In June 2003, PSK was ISO/TS 16949 2002 certified.

### 3. Material Selection background matte Sn + postbake

Main characteristics :

- material availability is good
- closest to SnPb in cost and process
- good solderability with SnPb and Pb free solders
- good solderjoint reliability
- “whisker free” process available (see section 5.3)

A comparison of the available post-plating finishes is showed in below table 1 :

**Table 1 : Comparison Post-Plating Materials (source: E3)**

Aspect	Sn Bright	Sn Matte	Sn Matte Baked	SnBi Bi<4%	SnCu	SnAg	SnPb
(1) Solder Wettability	+	+	+	+	+/-	+	++
(2) Adhesion to lead-frame	+	+	+	+	+	+	+
(3) Resistance to Leadbending	-	+	+	+/-			++
(4) Soldered joint Reliability	(+)	+	+	+	+	+	+
(5) Corrosion Resistance	+	+	+	+		+	+
(6) Whisker resistance	-	+/-	++	+	-		++
(7) Migration resistance	+	+	+				+
(8) Cost	+	+	+ / ++	-	-	--	++
(9) Mass Productivity	++	++	++	+	+	-	++
(10) Compatibility	+	+	+	+	(+)	(+)	+
(11) Eco Impact	++	++	++	+/-	+/-	--	-

### 4. Constructional Details of Test vehicles

Lot	PSK-01	PSK-02
Assy Site	PSK	PSK
Package / Pin	HSOP20	HSOP24
Outline	SOT418-2	SOT566-2
Moulding compound	6210SR	6210SR
Die-Attach Adhesive	PbAg2.5Sn2.0	PbAg2.5Sn2.0
Chip Coat	Yes	Yes
LF-mat/ pitch/ E or P	CuFe2P/1.27/P	CuFe2P/1.27/P
Die Pad Size (mm)	5.60x7.00	5.60x7.00
Die Size (mm)	4.82x5.98	4.29x5.15
Vehicle name	TDA8586TH/N1	TDA8920TH/N1

Note: test vehicles in PbAg2.5Sn2.0 PAS die-attach, will be used to release matte Sn of EP121-7 packages.

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## 5. Reliability Test Program

An extensive qualification program has been executed to demonstrate that PSK can assemble HSOP20 matte Sn packages with a high quality and reliability.

### 5.1 Reliability Test Descriptions

In this section the reliability tests are described in detail. These tests are stated in Philips Semiconductors' General Quality Specification (SNW-FQ-611) and the Plastic Package Qualification Guideline (SNW-FA-04-07).

#### *Pcon – Preconditioning*

SMD Qualification samples for PPOT and HAST undergo SMD reflow preconditioning before reliability test is performed. This preconditioning is performed in accordance with IPC/JEDEC J-STD-020B specification, as described in Philips Semiconductors specification SNW-FQ-225A. SMD packages are preconditioned to the appropriate MSL level. Peak temperature applied is 240-245°C.

#### *PPOT – Pressure Pot Test*

Pressure Pot Test – autoclave (121°C, 100%R.H., 96 hrs release time point), unbiased with Pcon. This test is particularly suitable to evaluate the moisture resistance of the package.

### 5.2 Construction Analysis Tests Descriptions

In addition to the reliability evaluation, qualification lots will be subjected to Construction Analysis tests which are relevant for the plating change per below test methods :

- Visual/Mechanical Inspection (V/M) SNW-FQ-612B
- Lead Finish Inspection (LFNH) Local document
- Solderability Inspection (SOLD) SNW-FQ-221

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### 5.3 Whisker Testing

#### 5.3.1 Whisker Mechanism

In order to understand the impacts of matte Sn plating, Philips is performing an extensive whisker research program. Topics of interest are a.o. :

- definition what is a whisker, understand the growing-mechanism
- plating characteristics such as layer thickness, grain size, crystal orientation
- leadframe base material impact
- counter measures for whisker growth
- recommendations for process control and process/product release tests.
- cooperate within E3 to have consensus within Europe's large players

The E3 presentation on the Pb-free CPCN website is showing the results and conclusions of the whisker research activities by the E3. The website address is :

[http://www.semiconductors.philips.com/acrobat/other/green\\_roadmap/e3\\_presentation.pdf](http://www.semiconductors.philips.com/acrobat/other/green_roadmap/e3_presentation.pdf)

#### 5.3.2 Whisker Tests Description

The following whisker tests have been performed on the test vehicles.

Despite huge amount of research, an acceleration test is not available at this moment. Philips ( and the E3) do consider the 2 years ambient test as best suitable.

However, based on industry and customer demanding, test B and test C per below were performed as a reference.

##### **Test A**

Storage at ambient (18°C -25 °C / 30-70% RH).

Inspect after 0, 4, 12 and 26 wks. Keep parts and do extended readpoints after 52 , 78 and 104 weeks.

Sample size : 10 post-baked samples

Accept when after 26 weeks not any whisker longer than 15 µm is found

##### **Test B**

TMCL 500 cycles -35°C/ 125 °C, minimum dwell time 7 minutes

Sample size : 10 post-baked samples.

Accept when no whiskers above 40 µm are found.

##### **Test C**

Storage at 55 °C and 85% RH.

Inspect after 8 weeks and after 26 weeks.

Sample size : 10 post-baked samples.

Accept when after 8 weeks no whiskers above 20 µm are found.

Accept when after 26 weeks no whiskers above 40 µm are found.

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#### 5.4 Summary of Solder Joint Reliability Tests for leadfree, leadframe based packages.

##### Variants included in the Investigation

- SMD packages with gull wing and J –leads (SO.....,VSO, QFP.....,PLCC.....)
- Lead frame material : Copper-alloy (mainly) and FeNi42 .
- Terminal finish : Matte Tin 100 , NiPdAu (only for Copper alloy)
- 2 layer FR4 board, (CE 5004)
- Reflow soldering : SnPb36Ag2 and SnAg 3.8Cu0.7
- Wave soldering with SnPb38Bi2 and SnAg3.8Cu0.7
- Temperature Cycling -40°C/125°C according to IEC60068-2-14.
- Electrical test (Daisy Chain) at around 2k intervals and visual inspection.

##### Conclusions

- No rejects up to 2000 cycles for all combinations.
- Mean time to failure over 6600 cycles except for FeNi based VSO56 and HTQFP100.
- Reflow solder : No significant difference in failure times/fracture modes between SnPb paste and SnAgCu paste.
- Wave solder : No significant difference in failure times/fracture modes between SnPb solder and SnAgCu solder.
- High profile packages / lead forms show less degradation due to a better compliancy.

##### Remarks

- All package variants applied with Pb and Pb-free soldering process
- Weibull graphs are shown in the E3 presentation which can be found on the Pb-free CPCN website : [http://www.semiconductors.philips.com/acrobat/other/green\\_roadmap/e3\\_presentation.pdf](http://www.semiconductors.philips.com/acrobat/other/green_roadmap/e3_presentation.pdf)

## 6. Self-qualification results matte Sn packages

**Table 2 : Reliability Tests matte Sn**

Package	Lot No.	Device	MSL/ temp.	PPOT		
				pcon	96 hrs	192 hrs
HSOP20	PSK-01	TDA8586TH/N1	3/245	L3	0/231	0/231
HSOP24	PSK-02	TDA8920TH/N1	3/245	L3	0/77	0/77

Reliability qualification requirements time points are shown in **bold**, additional points are for engineering evaluation.

**Table 3: Construction Analysis tests matte Sn**

Package	Lot No.	Device	Construction Analysis Tests					
			V/M	LFNH	SOLD-A <sup>(1)</sup>	SOLD-B <sup>(1)</sup>	SOLD-C <sup>(1)</sup>	SOLD-D <sup>(1)</sup>
HSOP20	PSK-01	TDA8586TH/N1	0/15	0/9	0/11	0/11	0/11	0/11
HSOP24	PSK-02	TDA8920TH/N1	0/15	0/9	0/11	0/11	0/11	0/11

(1) conditions for solderability testing :

A : SnPb solder after 8h steam age, 5 sec, 215 °C

B : SnPb solder after 16h dry-bake, 5 sec, 215 °C

C : SAC solder after 8h steam age, 3 sec, 245 °C

D : SAC solder after 16h dry-bake, 3 sec, 245 °C

RMA is the standard flux.

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**Table 4:** *Whisker Tests Results matte Sn*

Package	Lot No.	Device	Whisker Test Results				
			Whisker Test A		Whisker Test B	Whisker Test C	
			Readpoint in wks from assy	longest whisker in $\mu\text{m}$	longest whisker in $\mu\text{m}$ After TMCL 500x	Readpoint in wks from assy	longest whisker in $\mu\text{m}$
HSOP20	PSK-01	TDA8586TH/N1	26	0	7	26	5

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## 7. Conclusion

An extensive qualification program has been executed to demonstrate that PSK can assemble HSOP20 packages in matte Sn + postbake solution at a high quality and reliability level.

With the positive completion of the Qualification tests, the Assembly and Test Organization Philips Semiconductors announces the release of matte Sn + postbake for use in above mentioned packages via final CPCN 20030525F supplement 5.

## 8. Implementation

Deliveries will start from January 2005 onwards.

## 9. Document Revision Sheet

R E V I S I O N   S H E E T			
DATE yyyy/mm/dd	REV	DESCRIPTION	AUTHOR
2004-10-19	01	Self Qualification Results phase 6 for Lead (Pb) free lead-finish of leadframe-based IC packages. HSOP20 at PSK.	Rob de Heus