

Self Qualification Results

Matte Sn + postbake leadfree solution for

*QFP + SQFP
LQFP + HLQFP
TQFP + HTQFP*

Products with Copper based lead-frames

assembled in

*Philips Semiconductors Calamba (PSC)
Philips Semiconductors Kaohsiung (PSK)
Subcontractor Amkor (Korea + Philippines)
Subcontractor ASE Kaohsiung*

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Assembly & Test Organization Philips Semiconductors	Self Qualification Results: Matte Sn + postbake for QFP's in PSC, PSK, Amkor and ASE.	Document Number RNR-83-03/RdH/RdH-2045
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1. Introduction

The intention of the change to Pb-free packages from Philips has been announced in the Advanced CPCN for Pb-free, issued in May 2003, CPCN # 200305025.

The final CPCN will be issued in 5 different phases, each phase showing qualification results of a certain group of packages.

Notification of the 1st phase, covering SO14/16/20 packages in NiPdAu, was issued on 05 November 2003.

This self qualification report presents an overview of the qualification data completed to release a group of packages to be assembled in matte Sn + postbake solution.

This report covers the results of (S)QFP, (H)LQFP, (H)TQFP packages assembled in matte Sn on Copper based leadframes in assembly factories of PSC (Philips Semiconductors Calamba), PSK (Philips Semiconductors Kaohsiung), Amkor Korea, Amkor Philippines and ASE Kaohsiung.

The updated qualification plans for the other packages can be found in the updated Self Qualification plan, document number RNR-83-03/RdH/RdH-2057, report database # 030924, can be downloaded from the Philips Pb-free CPCN website : http://www.semiconductors.philips.com/green_roadmap/ .

In order to validate assembly quality and reliability, a self-qualification program has been performed for matte Sn in (S)QFP, (H)LQFP, (H)TQFP family from above mentioned assembly centres.

The results of this qualification demonstrate that Philips Semiconductors can achieve distinctive assembly quality with equal or better product quality and reliability when compared to the lead-tin plated versions of these products.

With the introduction of matte Sn as Pb-free solution, the Bill of Materials (BoM) of the mentioned packages is fully compliant to the RoHS legislation requirements.

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2. Assembly Facilities

PSC

Philips Semiconductors Calamba is a new, state-of-art facility for the assembly and testing of IC's located at the Light Industry and Science Park II in Calamba. The plant occupies an area of 85,000 square meters of land. Construction of the first phase with a floor area of 17,900 square meters was completed in 1998, while the second phase is already in construction.

Package family portfolio and test capabilities of PSC consists of SSOP/TSSOP, QFP, HVQFN and LF/TFBGA.

Philips Semiconductors Calamba successfully passed certification to the QS9000 standard, while ISO 14001 certification was achieved in March 2000.

PSK

Philips Semiconductors Kaohsiung is the first organization set up in the Republic of China by Philips Electronics in 1966. In 1969 the IC assembly started in the Nantze Export Processing Zone ("Nantze EPZ") in Kaohsiung, Taiwan. At present the floor space is 49,000 square meters and the total number of employees is 2700.

Package family portfolio and test capabilities of PSK consists of DIP, SILP, SO, VSO, SSOP, QFP and BGA.

PSK has received Ford TQE (Total Quality Excellence) award, ISO9002, ISO900 and ISO140001 certification. In 1997 PSK received QS-9000 certification and the Japan Quality Medal.

In June 2003, PSK was ISO/TS 16949 2002 certified.

AMKOR

AMKOR is one of Philips preferred subcontractors and is established in 1968. Amkor has grown to be a world-class leader in integrated circuit (IC) packaging, assembly and test services. AMKOR has assembly factories in Korea (ATK), Taiwan (ATT), China (ATC) and the Philippines (ATP).

Package family portfolio of AMKOR consists of amongst others DIP, SO, SSOP, PLCC, QFP, (LF)BGA and CSP. AMKOR is certified SAC level 1.

ASE

Advanced Semiconductor Engineering, Inc. (ASE Inc.) is the largest independent IC packaging company in Taiwan. The Company was founded in 1984. Commercial production began at the packaging facility located in the Nantze Export Processing Zone ("Nantze EPZ") in Kaohsiung, Taiwan in July 1984.

Package family portfolio of ASE consists of amongst others DIP, SO, SSOP, PLCC, CSP, QFP and (LF)BGA. ASE is certified SAC level 1.

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3. Material Selection background matte Sn + postbake

Main characteristics :

- material availability is good
- closest to SnPb in cost and process
- good solderability with SnPb and Pb free solders
- good solderjoint reliability
- “whisker free” process available (see section 5.3)

A comparison of the available post-plating finishes is showed in below table 1 :

Table 1 : *Comparison Post-Plating Materials (source: E3)*

Aspect	Sn Bright	Sn Matte	Sn Matte Baked	SnBi Bi<4%	SnCu	SnAg	SnPb
(1) Solder Wettability	+	+	+	+	+/-	+	++
(2) Adhesion to lead-frame	+	+	+	+	+	+	+
(3) Resistance to Leadbending	-	+	+	+/-			++
(4) Soldered joint Reliability	(+)	+	+	+	+	+	+
(5) Corrosion Resistance	+	+	+	+		+	+
(6) Whisker resistance	-	+/-	++	+	-		++
(7) Migration resistance	+	+	+				+
(8) Cost	+	+	+ / ++	-	-	--	++
(9) Mass Productivity	++	++	++	+	+	-	++
(10) Compatibility	+	+	+	+	(+)	(+)	+
(11) Eco Impact	++	++	++	+/-	+/-	--	-

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4. Constructional Details of Test vehicles

Lot	PSC-04	PSC-05	PSC-06	PSC-08
Assy Site	PSC	PSC	PSC	PSC
Package / Pin	LQFP32	LQFP80	QFP64	LQFP64
Outline	SOT401-1	SOT315-1	SOT393-1	SOT314-2
Moulding compound	G700	G700	MP8000	G700
Die-Attach Adhesive	QMI-519	QMI-519	8390P	QMI-519
LF-mat/ pitch/ E or P	CuNi3/0.5/E	CuNi3/0.5/P	CuNi3/0.8/P	CuNi3/0.8/P
Die Pad Size (mm)	2.45x2.45	9.60x9.60	5.60x5.60	4.60x4.60
Die Size (mm)	2.10x2.10	6.01x7.55	2.53x2.58	
Vehicle name	TZA3031AHL/C4	TEA6849H/V1/M5	SAA7325H/T/M2B	ISP1160BD

Lot	PSK-01	PSK-02	PSK-03	PSK-05
Assy Site	PSK	PSK	PSK	PSK
Package / Pin	HTQFP100	LQFP100	LQFP208	QFP100
Outline	SOT638-1	SOT407-1	SOT459-1	SOT317-2
Moulding compound	7351U	7351U	7351U	MP8000
Die-Attach Adhesive	8390P	8390P	8390P	8390P
LF-mat/ pitch/ E or P	CuCr/0.5/U	CuNi3/0.5/P	CuNi3/0.5/E	CuNi3/0.65/P
Die Pad Size (mm)	6.60x6.60	5.60x5.60	8.00x8.00	8.00x8.00
Die Size (mm)	4.56x4.56	3.95x4.05	6.769 x 6.756	5.36x5.54
Vehicle name	PNX8510C	PCF2113DH/F2	SAA7810HL/M3B	TDA8044AH/C2

PSC = Philips Semiconductors Calamba factory
PSK = Philips Semiconductors Kaohsiung factory

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Lot	ATK-02	ATK-03
Assy Site	ATK	ATK
Package / Pin	SQFP208	HLQFP176
Outline	SOT316-1	SOT766-1
Moulding compound	MP8000	EME G700
Die-Attach Adhesive	8361J	3230
LF-mat/ pitch/ E or P	CuNi3/0.5/E	CuCr/0.5/E
Die Pad Size (mm)	9.50x9.50	6.00x6.00
Die Size (mm)	8.038x8.728	4.40x3.96
Vehicle name	SAA7219HS/C3	TDA8751HV/C1

Lot	ATP-03
Assy Site	ATP
Package / Pin	QFP160
Outline	SOT322-2
Moulding compound	MP8000
Die-Attach Adhesive	8361J
LF-mat/ pitch/ E or P	CuNi3/0.65/E
Die Pad Size (mm)	7.00x7.00
Die Size (mm)	5.96x5.44
Vehicle name	SAA4993H/V1

Lot	ASE-03	ASE-04
Assy Site	ASE	ASE
Package / Pin	LQFP128	QFP160
Outline	SOT420-1	SOT322-2
Moulding compound	G700	MP8000
Die-Attach Adhesive	8340	8361J
LF-mat/ pitch/ E or P	CuNi3/0.4/P	CuNi3/0.65/U
Die Pad Size (mm)	6.50x6.50	6.99x6.99
Die Size (mm)	5.30x5.50	5.67x5.73
Vehicle name	ISP1561	SAA6713H/V1

ATK = Amkor Korea factory
ATP = Amkor Philippines factory
ASE = ASE Kaohsiung factory

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5. Reliability Test Program

An extensive qualification program has been executed to demonstrate that PSC, PSK, Amkor and ASE can assemble matte Sn packages with a high quality and reliability.

5.1 Reliability Test Descriptions

In this section the reliability tests are described in detail. These tests are stated in Philips Semiconductors' General Quality Specification (SNW-FQ-611) and the Plastic Package Qualification Guideline (SNW-FA-04-07). AEC_Q100 is used as a guideline for specific automotive products.

Pcon – Preconditioning

SMD Qualification samples for PPOT, HAST/THBS and TMCL undergo SMD reflow preconditioning before reliability test is performed. This preconditioning is performed in accordance with the latest revision of the IPC/JEDEC JSTD-020B specification, as described in Philips Semiconductors specification SNW-FQ-225A. SMD Packages are preconditioned to the appropriate MSL level. Peak temperature applied is 245°C for large bodies and 260°C for small bodies.

PPOT – Pressure Pot Test

Pressure Pot Test – autoclave (121°C, 100%R.H., 96 hrs release time point), unbiased with Pcon. This test is particularly suitable to evaluate the moisture resistance of the package.

HAST – Highly Accelerated Stress Test

Highly Accelerated Stress Test (130°C/85% R.H., 96 hrs release time point), with electrical bias and Pcon. This test stresses both the electrical endurance of the design/process, as well as the resistance to moisture of the package.

5.2 Construction Analysis Tests Descriptions

In addition to the reliability evaluation, qualification lots will be subjected to Construction Analysis tests which are relevant for the plating change per below test methods :

- Visual/Mechanical Inspection (V/M) SNW-FQ-612B
- Lead Finish Inspection (LFNH) Local document
- Solderability Inspection (SOLD) SNW-FQ-221

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5.3 Whisker Testing

5.3.1 Whisker Mechanism

In order to understand the impacts of matte Sn plating, Philips is performing an extensive whisker research program. Topics of interest are a.o. :

- definition what is a whisker, understand the growing-mechanism
- plating characteristics such as layer thickness, grain size, crystal orientation
- leadframe base material impact
- counter measures for whisker growth
- recommendations for process control and process/product release tests.
- cooperate within E3 to have consensus within Europe's large players

The E3 presentation on the Pb-free CPCN website is showing the results and conclusions of the whisker research activities by the E3. The website address is :

http://www.semiconductors.philips.com/green_roadmap/

5.3.2 Whisker Tests Description

The following whisker tests have been performed on the test vehicles.

Despite huge amount of research, an acceleration test is not available at this moment. Philips (and the E3) do consider the 2 years ambient test as best suitable.

However, based on industry and customer demanding, test B and test C per below were performed as a reference.

Test A

Storage at ambient (18°C -25 °C / 30-70% RH).

Inspect after 0, 4, 12 and 26 wks. Keep parts and do extended readpoints after 52 , 78 and 104 weeks.

Sample size : 10 post-baked samples

Accept when after 26 weeks not any whisker longer than 15 µm is found

Test B

TMCL 500 cycles -35°C/ 125 °C, minimum dwell time 7 minutes

(this test for Copper-based leadframes only)

Sample size : 10 post-baked samples.

Accept when no whiskers above 40 µm are found.

Test C

Storage at 55 °C and 85% RH.

Inspect after 8 weeks and after 26 weeks.

Sample size : 10 post-baked samples.

Accept when after 8 weeks no whiskers above 20 µm are found.

Accept when after 26 weeks no whiskers above 40 µm are found.

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5.4 Summary of Solder Joint Reliability Tests for leadfree, leadframe based packages.

5.4.1 Variants included in the Investigation

- SMD packages with gull wing and J –leads (SO.....,VSO, QFP.....,PLCC.....)
- Lead frame material : Copper-alloy (mainly) and FeNi42 .
- Terminal finish : Matte Tin 100 , NiPdAu (only for Copper alloy)

- 2 layer FR4 board, (CE 5004)
- Reflow soldering : SnPb36Ag2 and SnAg 3.8Cu0.7
- Wave soldering with SnPb38Bi2 and SnAg3.8Cu0.7

- Temperature Cycling -40°C/125°C according to IEC60068-2-14.
- Electrical test (Daisy Chain) at around 2k intervals and visual inspection

5.4.2 Conclusions

- No rejects up to 2000 cycles for all combinations.
- Mean time to failure over 6600 cycles except for FeNi based VSO56 and HTQFP100.
- Reflow solder : No significant difference in failure times/fracture modes between SnPb paste and SnAgCu paste .
- Wave solder : No significant difference in failure times/fracture modes between SnPb solder and SnAgCu solder.
- High profile packages / lead forms show less degradation due to a better compliancy.

5.4.3 Remarks

- All package variants applied with Pb and Pb-free soldering process
- Weibull graphs are shown in the E3 presentation which can be found on the Pb-free CPCN website : http://www.semiconductors.philips.com/green_roadmap/.

6. Self-qualification results matte Sn packages

Table 2 : Reliability Tests matte Sn

Package	Lot	Device	MSL/ temp.	PPOT			HAST		
	No.			pcon	96 hrs	192 hrs	Pcon	96 hrs	192 hrs
QFP64	PSC-06	SAA7325H/T/M2B	2/245	0/77	0/71	0/71	0/45	0/44	-
QFP100	PSK-05	TDA8044AH/C2	3/245	0/77	0/77	-	-	-	-
QFP160	ATP-03	SAA4993H/V1	3/245	0/77	0/77	-	-	-	-
QFP160	ASE-04	SAA6713H/V1	3/245	0/77	0/76	-	-	-	-
SQFP208	ATK-02	SAA7219HS/C3	3/245	0/77	0/77	-	-	-	-
LQFP32	PSC-04	TZA3031AHL/C4	1/260	0/77	0/76	0/76	0/36	0/36	-
LQFP80	PSC-05	TEA6849H/V1/M5	2/260	0/77	0/77	0/77	0/45	0/45	-
LQFP100	PSK-02	PCF2113DH/F2	2/260	0/77	0/77	-	0/45	0/45	-
LQFP128	ASE-03	ISP1561	2/260	0/77	0/77	-	0/45	0/45	-
HLQFP176	ATK-03	TDA8751HV/C1	-	-	-	-	-	-	-
HTQFP100	PSK-01	PNX8510C	1/260	0/77	0/77	-	-	-	-
LQFP208	PSK-03	SAA7810HL/M3B	3/245	0/77	0/77	-	-	-	-

Reliability qualification requirements time points are shown in **bold**, additional points are for engineering evaluation.

Table 3: Construction Analysis tests matte Sn

Package	Lot No.	Device	Construction Analysis Tests					
			V/M	LFNH	SOLD-A ⁽¹⁾	SOLD-B ⁽¹⁾	SOLD-C ⁽¹⁾	SOLD-D ⁽¹⁾
QFP64	PSC-06	SAA7325H/T/M2B	0/15	0/9	0/11 ⁽³⁾	0/11 ⁽³⁾	0/11	0/11
QFP100	PSK-05	TDA8044AH/C2	0/15	0/9	0/11	0/11	0/11	0/11
QFP160	ATP-03	SAA4993H/V1	0/15	0/9	0/11	0/11	0/11	0/11
QFP160	ASE-04	SAA6713H/V1	0/15	0/9	0/11	0/11	0/11	0/11
SQFP208	ATK-02	SAA7219HS/C3	0/15	0/9	0/11 ⁽³⁾	0/11 ⁽³⁾	0/11	0/11
LQFP32	PSC-04	TZA3031AHL/C4	0/15	0/9	0/11 ⁽³⁾	0/11 ⁽³⁾	0/11	0/11
LQFP64	PSC-08	ISP1160BD	0/15	0/9	0/11 ⁽³⁾	0/11 ⁽³⁾	0/11	0/11
LQFP80	PSC-05	TEA6849H/V1/M5	0/15	0/9	0/11 ⁽³⁾	0/11 ⁽³⁾	0/11	0/11
LQFP100	PSK-02	PCF2113DH/F2	0/15	0/9	0/11	0/11	0/11	0/11
LQFP128	ASE-03	ISP1561	0/15	0/9	0/11	0/11	0/11	0/11
HLQFP176	ATK-03	TDA8751HV/C1	0/15	0/9	0/11 ⁽²⁾	0/11 ⁽²⁾	0/11 ⁽²⁾	0/11 ⁽²⁾
HTQFP100	PSK-01	PNX8510C	0/15	0/9	0/11	0/11	0/11	0/11
LQFP208	PSK-03	SAA7810HL/M3B	0/15	0/9	0/11	0/11	0/11	0/11

(1) conditions for solderability testing :

A : SnPb solder after 8h steam age, 5 sec, 215 °C

B : SnPb solder after 16h dry-bake, 5 sec, 215 °C

C : SAC solder after 8h steam age, 3 sec, 245 °C

D : SAC solder after 16h dry-bake, 3 sec, 245 °C

RMA is the standard flux.

(2) : R-flux was used in stead of RMA flux.

(3) : 3 sec dipping used in stead of 5 sec.

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Table 4: Whisker Tests Results matte Sn

Package	Lot No.	Device	Whisker Test Results				
			Whisker Test A ⁽¹⁾		Whisker Test B	Whisker Test C ⁽¹⁾	
			Readpoint in wks from assy	Result	Result After TMCL 500x	Readpoint in wks from assy	Result
QFP64	PSC-06	SAA7325H/T/M2B	20wks	Pass	Pass	16wks	Pass
QFP100	PSK-05	TDA8044AH/C2	26wks	Pass	Pass	26 wks	Pass
QFP160	ATP -03	SAA4993H/V1	20wks	Pass	Pass	16 wks	Pass
QFP160	ASE-04	SAA6713H/V1	18wks	Pass	Pass	18wks	Pass
SQFP208	ATK -02	SAA7219HS/C3	18wks	Pass	Pass	18wks	Pass
LQFP32	PSC-04	TZA3031AHL/C4	4wks	Pass	Pass	8wks	Pass
LQFP64	PSC-08	ISP1160BD	12wks	Pass	Pass	8wks	Pass
LQFP80	PSC-05	TEA6849H/V1/M5	20wks	Pass	Pass	16wks	Pass
LQFP100	PSK-02	PCF2113DH/F2	26wks	Pass	Pass	26 wks	Pass
LQFP128	ASE-03	ISP1561	18wks	Pass	Pass	18wks	Pass
HTQFP100	PSK-01	PNX8510C	26wks	Pass	Pass	26 wks	Pass
LQFP208	PSK-03	SAA7810HL/M3B	26wks	Pass	Pass	26 wks	Pass

(1) : these are interim readpoints after x weeks from plating date, 26 wks readpoints will be available before mass-production starts.

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7. Conclusion

An extensive qualification program has been executed to demonstrate that PSC, PSK, Amkor and ASE can assemble (S)QFP, (H)LQFP and (H)TQFP packages in matte Sn + postbake solution at a high quality and reliability level.

With the positive completion of the Qualification tests, the Assembly and Test Organization Philips Semiconductors announces the release of matte Sn + postbake for use in (S)QFP, (H)LQFP and (H)TQFP products assembled in PSC, PSK, Amkor and ASE, via final CPCN 20030525F phase 2.

8. Implementation

Deliveries will start from February 2004 onwards.

9. Document Revision Sheet

R E V I S I O N S H E E T			
DATE yyyy/mm/dd	REV	DESCRIPTION	AUTHOR
2003-12-08	01	Self Qualification Results phase 2 for Lead (Pb) free lead-finish of leadframe-based IC packages.	Rob de Heus
2003-12-16	02	Minor update	Rob de Heus