

MF0 IC U10 01

MF0 IC U11 01

Bumped sawn wafer on UV-tape

Rev. 3.2 — 16 March 2007
102132

Product data sheet
PUBLIC

1. General description

1.1 Scope

The MF0 IC U10 01 and the MF0 IC U11 01 are contactless Smart Card ICs designed for card IC coils following the mifare card IC coil design guide and are qualified to work properly in NXP' reader environment, which is built according to NXP' specification.

This specification describes electrical, physical and dimensional properties of wafers.

2. Features

3. Applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Ordering Code
MF0ICU1001W/V1D			9352 774 63005
MF0ICU1101W/V1D			9352 774 72005

5. Mechanical specification

5.1 Wafer

- Diameter: 200mm
- Thickness: $150\mu\text{m} \pm 15\mu\text{m}$
- PGDW: 62861
- PCM location: reticle area

5.2 Wafer backside

- Material: Si
- Treatment: ground and stress relieve
- Roughness: R_a max. 0.5 μm
 R_t max. 5 μm

5.3 Chip dimensions

- Chip size: 0.69 x 0.69 mm
- Scribe line: 66.4 / 86.4 μm
- Pad size:
 - LA, LB 104 x 104 μm
 - TEST, VSS¹ 74 x 74 μm

5.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride(on top)
- Thickness: 500 nm / 600 nm

5.5 Au bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
 - within a die: $\pm 2 \mu\text{m}$
 - within a wafer: $\pm 3 \mu\text{m}$
 - wafer to wafer: $\pm 4 \mu\text{m}$
- Bump flatness: $\pm 1.5 \mu\text{m}$
- Bump size:
 - LA, LB, VSS 90 x 90 μm
 - TESTIO 60 x 60 μm
- Bump size variation: $\pm 5 \mu\text{m}$
- Under bump metallization: sputtered TiW

Remark: Substrate is connected to VSS.

1.Pads VSS and TESTIO are disconnected when wafer is sawn.

5.6 Fail die identification

All fail dies are inked according to electrical test results.

Electronic wafer mapping (IBIS format) covers the electrical test results and additionally the results of mechanical/visual inspection.

6. Chip orientation and bondpad locations

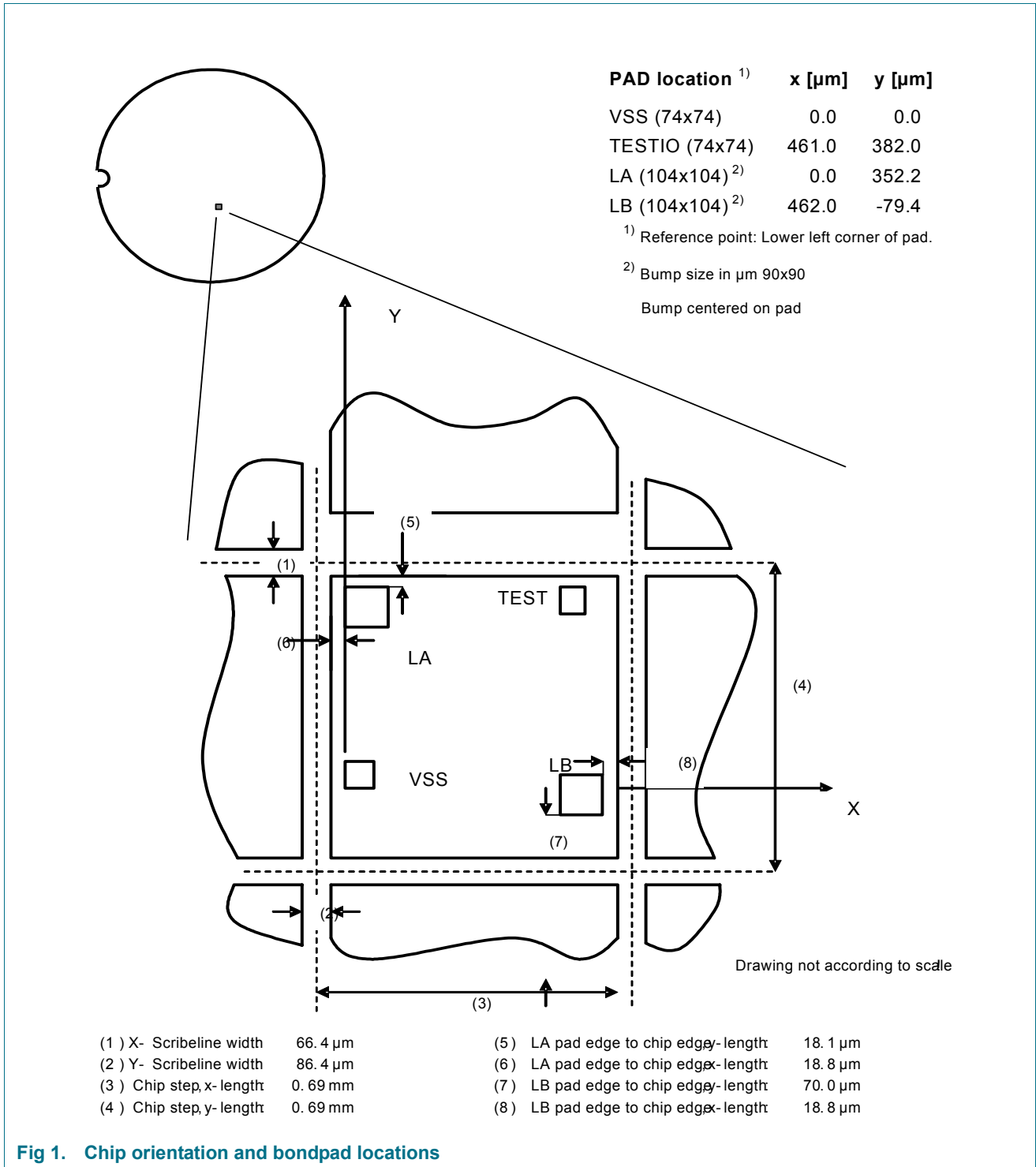


Fig 1. Chip orientation and bondpad locations

7. Limiting values

Table 2. Limiting values^{[1][2][3][4]}

In accordance with the Absolute Maximum Rating System(IEC 134)

Symbol	Parameter	Min	Max	Unit
I_{IN}	Input current	-	30	mA
T_{STOR}	Storage temperature	-55	125	°C
T_{OP}	Operating temperature	-25	70	°C
V_{ESD}	Electrostatic discharge voltage LA-LB ^[4]	2		kV
I_{LU}	Latchup current	±100		mA

- [1] Stresses above one or more of the limiting values may cause permanent damage to the device
- [2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the Characteristics section of the specification is not implied
- [3] Exposure to limiting values for extended periods may affect device reliability
- [4] MIL Standard 883-C method 3015; Human body model: C = 100 pF, R = 1.5 kΩ

8. Characteristics

8.1 Electrical Characteristics MF0 IC U10 01

Table 3. Characteristics MF0 IC U10 01^{[1][2][3]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{IN}	Input Frequency		-	13.56	-	MHz
C_{IN}	Input capacitance (LCR meter HP4258)	22°C, Cp-D, 13.56 MHz, 2V	14.85	17.0	20.13	pF
t_W	EEPROM write time		-	3.8	-	ms
t_{RET}	EEPROM data retention		5	-	-	years
N_{WE}	EEPROM write endurance		10000	-	-	cycles

- [1] Stresses above one or more of the limiting values may cause permanent damage to the device
- [2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the Characteristics section of the specification is not implied
- [3] Exposure to limiting values for extended periods may affect device reliability

8.2 Electrical Characteristics MF0 IC U11 01

Table 4. Characteristics MF0 IC U11 01^{[1][2][3]}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{IN}	Input Frequency		-	13.56	-	MHz
C_{IN}	Input capacitance (LCR meter HP4258)	22°C, Cp-D, 13.56 MHz, 2V	42.5	50	57.5	pF
t_W	EEPROM write time		-	3.8	-	ms
t_{RET}	EEPROM data retention		5	-	-	years
N_{WE}	EEPROM write endurance		10000	-	-	cycles

[1] Stresses above one or more of the limiting values may cause permanent damage to the device

[2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the Characteristics section of the specification is not implied

[3] Exposure to limiting values for extended periods may affect device reliability

9. Support information

For additional information, please visit: <http://www.nxp.com>

10. References

- [Data sheet "general specification for unsawn 8" wafer on UV-tape"](#)
- [Data sheet "au bumps layout rules and specification"](#)
- [Data sheet "Contactless single-trip ticket IC MF0 IC U1 functional specification"](#)
- [Application note "mifare card IC coil design guide"](#)
- [Data sheet "specification of the IBIS wafer map"](#)

11. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
102130	August 2006	Initial version		
102131	February 2007	Product data sheet		3.0
102132	16 March 2007	Product data sheet	treatment information	3.1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. 			

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Fig 1. Chip orientation and bondpad locations⁴

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