

DATA SHEET

ADDENDUM

SL2 ICS11

I•CODE UID

Smart Label IC

Bumped Wafer Specification

Product Specification
Revision 3.0

2004 January 30
089030

Bumped Wafer Specification**SL2 ICS11****CONTENTS**

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Bumped Wafer Specification

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1 SCOPE

This specification describes electrical, physical and dimensional properties of Au-bumped, sawn wafers on FFC of I•CODE UID Smart Label IC.

2 REFERENCE DOCUMENTS

2.1 Philips Documents

- Data Sheet 'General Specification for 8" Wafer'
- Data Sheet 'General Quality Specification'
- Data Sheet 'I•CODE UID Smart Label IC, Functional Specification'
- Data Sheet 'Specification of the IBIS Wafermap'
- Application Note 'Coil Design Guide'

3 MECHANICAL SPECIFICATION

3.1 Wafer

- Diameter: 200 mm (8")
- Thickness: 150 μm \pm 15 μm

3.2 Wafer Backside

- Material: Si
- Treatment: ground and stress release
- Roughness: R_a max. 0.5 μm ,
 R_t max. 5 μm

3.3 Chip Dimensions

- Chip size: x = 760 μm , y = 560 μm
- Scribe line: x-line: 60 μm
y-line: 80 μm

3.4 Passivation on Front

- Type: Sandwich structure
- Material: PSG/Nitride (on top)
- Thickness: 500 nm/600 nm

3.5 Au Bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
 - within a die: $\pm 2 \mu\text{m}$
 - within a wafer: $\pm 3 \mu\text{m}$
 - wafer to wafer: $\pm 4 \mu\text{m}$
- Bump flatness: $\pm 1.5 \mu\text{m}$
- Bump size:
 - LA, LB 90 x 90 μm
 - TestIO/Vss⁽¹⁾ 60 x 60 μm
- Bump size variation: $\pm 5 \mu\text{m}$
- Under bump metallisation: sputtered TiW

(1) TestIO and Vss are floating after sawing.

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4 FAIL DIE IDENTIFICATION

Every die is electrically tested according to data sheet. Identification of chips with electrical parameters not conform with the data sheet is done by inking and wafer mapping (all dies at wafer periphery are identified as 'FAIL').

The ink information refers to unsawn wafers. At sawn wafers (on FFC) additional ICs are marked as 'FAIL' in the wafer map if damaged during the sawing process. These ICs will not be inked.

4.1 Wafer Mapping

Wafer mapping for failed die information is available on Floppy-Disk.

Format: IBIS format

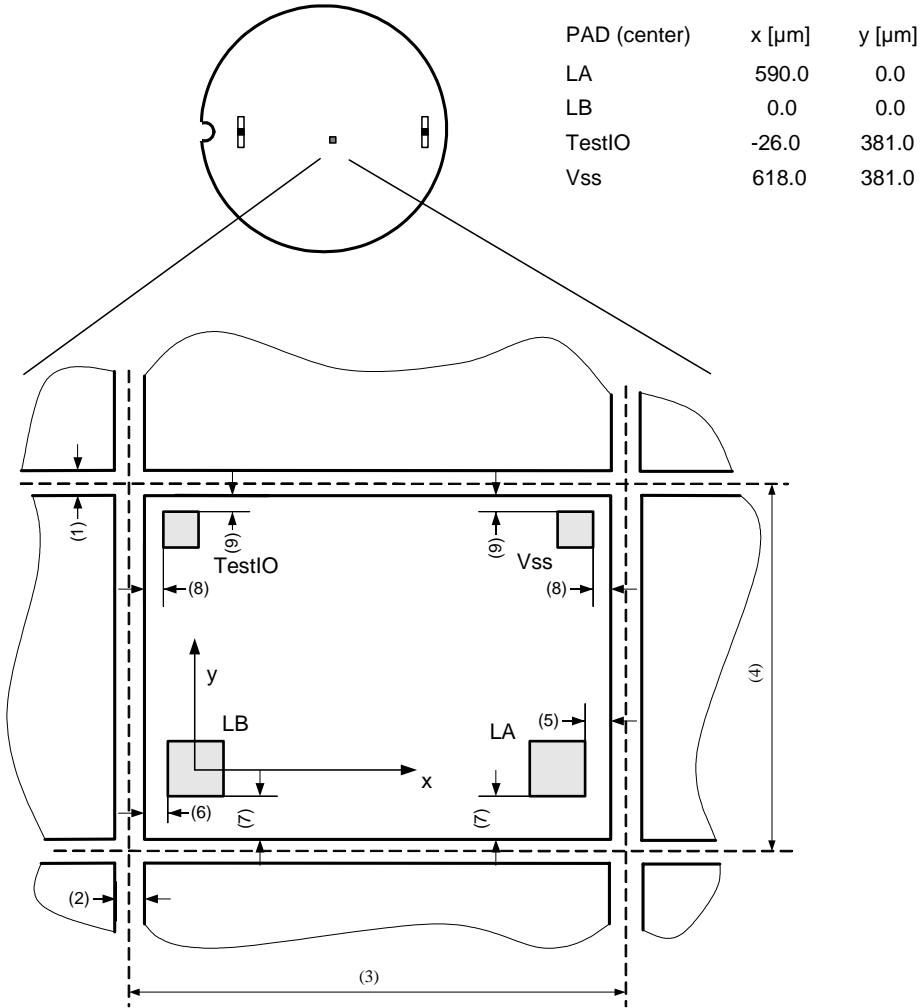
5 ORDERING INFORMATION

TYPE NAME	DESCRIPTION	ORDERING CODE
SL2 ICS11 01DW/V4	Bumped die on sawn wafer	9352 751 57005

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6 CHIP ORIENTATION AND BONDPAD LOCATIONS



- | | | | |
|--|-------------------|---|------------------|
| (1) x-Scribeline width: | 60 μm | (6) LB bump edge to chip edge, x-length: | 39 μm |
| (2) y-Scribeline width: | 80 μm | (7) LA, LB bump edge to chip edge, y-length: | 71 μm |
| (3) Chip step, x-length: | 840 μm | (8) TestIO, Vss bump edge to chip edge, x-length: | 28 μm |
| (4) Chip step, y-length: | 620 μm | (9) TestIO, Vss bump edge to chip edge, y-length: | 33 μm |
| (5) LA bump edge to chip edge, x-length: | 41 μm | | |

Fig.1 Bondpad plan SL2 ICS11.

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7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T _{stg}	Storage Temperature Range		-55		+140	°C
T _j	Junction Temperature		-55		+140	°C
V _{ESD}	ESD Voltage Immunity	JEDEC, JESD 22 – A114-B, Human Body Model			±2	kV _{peak}
I _{max LA-LB}	Maximum Input Peak Current				±60	mA _{peak}

Notes

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

7.2 Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
T _{jop}	Operating Junction Temperature		-25		+85	°C
I _{LA-LB}	Input Current ⁽²⁾				30	mA _{rms}
V _{LA-LB rd}	Minimum Supply Voltage for READ			2.6	2.9	V _{rms}
V _{LA-LB wr}	Minimum Supply Voltage for WRITE			2.6	2.9	V _{rms}
f _{op}	Operating Frequency ⁽³⁾		13.553	13.560	13.567	MHz

Notes

- Typical ratings are not guaranteed. These values listed are at room temperature.
- The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I_{LA-LB}).
- Bandwidth limitation (±7 kHz) according to ISM band regulations.

7.3 Electrical Characteristics

T_{op} = -25 to +85 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
C _{res}	Input Capacitance between LA – LB ⁽²⁾	V _{LA-LB} = 2 V _{rms}	22.3	23.5	24.7	pF
P _{min rd}	Minimum Operating Supply Power for READ ⁽³⁾			400		μW
P _{min wr}	Minimum Operating Supply Power for WRITE ⁽³⁾			400		μW
t _{ret}	Data Retention	T _{amb} ≤ 55 °C	5			Years
n _{write}	Write Endurance	T _{amb} ≤ 55 °C	10000			Cycles

Notes

- Typical ratings are not guaranteed. These values listed are at room temperature.
- Measured with an HP4285A LCR meter at 13.56 MHz.
- Including losses in resonant capacitor and rectifier.

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8 FINAL WAFERTEST SPECIFICATION

- Minimum yield per wafer: 30 % of 56276 potential good dies.

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9 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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12 REVISION HISTORY**Table 1** Bumped Wafer Specification SL2 ICS11 Revision History

REVISION	DATE	CPCN	PAGE	DESCRIPTION
3.0	Jan 2004	-		Contents updated. Status now -> Product Specification
			4	Chapter 5 "ORDERING INFORMATION": - added Ordering Code
1.0	Oct. 2003	-		Initial version

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