

SL2 ICS12

I•CODE UID-OTP bumped wafer on UV-tape addendum

Rev. 3.0 — 15 May 2007
134730

Product data sheet
PUBLIC

1. General description

This specification describes electrical, physical and dimensional properties of Au-bumped, sawn wafers on FFC of I•CODE UID-OTP Smart Label IC.

2. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Ordering Code
SL2 ICS12 01DW/V1		Bumped die on sawn wafer	9352 831 35005

3. Mechanical specification

3.1 Wafer

- Diameter: 8"
- Thickness: 150 $\mu\text{m} \pm 15 \mu\text{m}$

3.2 Wafer backside

- Material: Si
- Treatment: ground and stress release
- Roughness: R_a max. 0.5 μm
 R_t max. 5 μm

3.3 Chip dimensions

- Chip size: x = 760 μm , y = 560 μm
- Scribe lines: x-line: 60 μm
y-line: 80 μm

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride(on top)
- Thickness: 500 nm / 600 nm

3.5 Au bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
 - within a die: $\pm 2 \mu\text{m}$
 - within a wafer: $\pm 3 \mu\text{m}$
 - wafer to wafer: $\pm 4 \mu\text{m}$
- Bump flatness: $\pm 1.5 \mu\text{m}$
- Bump size:
 - LA, LB 90 x 90 μm^2
 - VSS¹, TESTIO¹ 60 x 60 μm^2
- Bump size variation: $\pm 5 \mu\text{m}$
- Under bump metallization: sputtered TiW

3.6 Fail die identification

Every die is electrically tested according to data sheet. Identification of chips with electrical parameters not conform with the data sheet is done by inking and wafer mapping (all dies at wafer periphery are identified as 'FAIL').

The ink information refers to unsawn wafers. At sawn wafers (on FFC) additional ICs are marked as 'FAIL' in the wafer map if damaged during the sawing process. These ICs will not be inked.

3.6.1 Wafer Mapping

Wafer mapping for failed die information is available on Floppy-Disk.

Format: IBIS format

3.6.2 Final wafertest specification

- Minimum yield per wafer: 30 % of 56276 potential good dies.

1.Pads VSS and TESTIO are disconnected when wafer is sawn.

4. Limiting values

Table 2. Limiting values^{[1][2]}

Absolute Maximum Ratings

Symbol	Parameter	Min	Type	Max	Unit
T _{STOR}	Storage temperature range	-55		+140	°C
T _j	Junction Temperature	-55		+140	°C
V _{ESD}	Electrostatic discharge voltage	[3]		±2	kV _{peak}
I _{max LA-LB}	Maximum input peak current	-		±60	mA _{peak}
T _{jop}	Operating Junction Temperature	-25		+85	°C
I _{LA-LB}	Input Current	[4]		30	mA _{rms}

- [1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.
- [2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- [3] JEDEC, JESD 22 – A114-B, Human body model
- [4] The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I_{LA-LB})

5. Characteristics

5.1 Electrical Characteristics

T_{op} = -25 to 85°C

Table 3. Characteristics ^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{LA-LB rd}	Minimum Supply Voltage for READ			2.6	2.9	V _{rms}	
V _{LA-LB wr}	Minimum Supply Voltage for WRITE			2.6	2.9	V _{rms}	
f _{op}	Operating Frequency		[2]	13.553	13.560	13.567	MHz
C _{res}	Input Capacitance between LA – LB	V _{LA-LB} = 2 V _{rms}	[3]	22.3	23.5	24.7	pF
P _{min rd}	Minimum Operating Supply Power for READ		[4]		400		μW
P _{min wr}	Minimum Operating Supply Power for WRITE		[4]		400		μW
t _{ret}	Data Retention	T _{amb} ≤ 55 °C		5			Years
n _{write}	Write Endurance			not applicable (OTP)			

- [1] Typical ratings are not guaranteed. These values listed are at room temperature..
- [2] Bandwidth limitation (±7 kHz) according to ISM band regulations.
- [3] Measured with an HP4285A LCR meter at 13.56 MHz
- [4] Including losses in resonant capacitor and rectifier

6. Chip orientation and bond pad locations

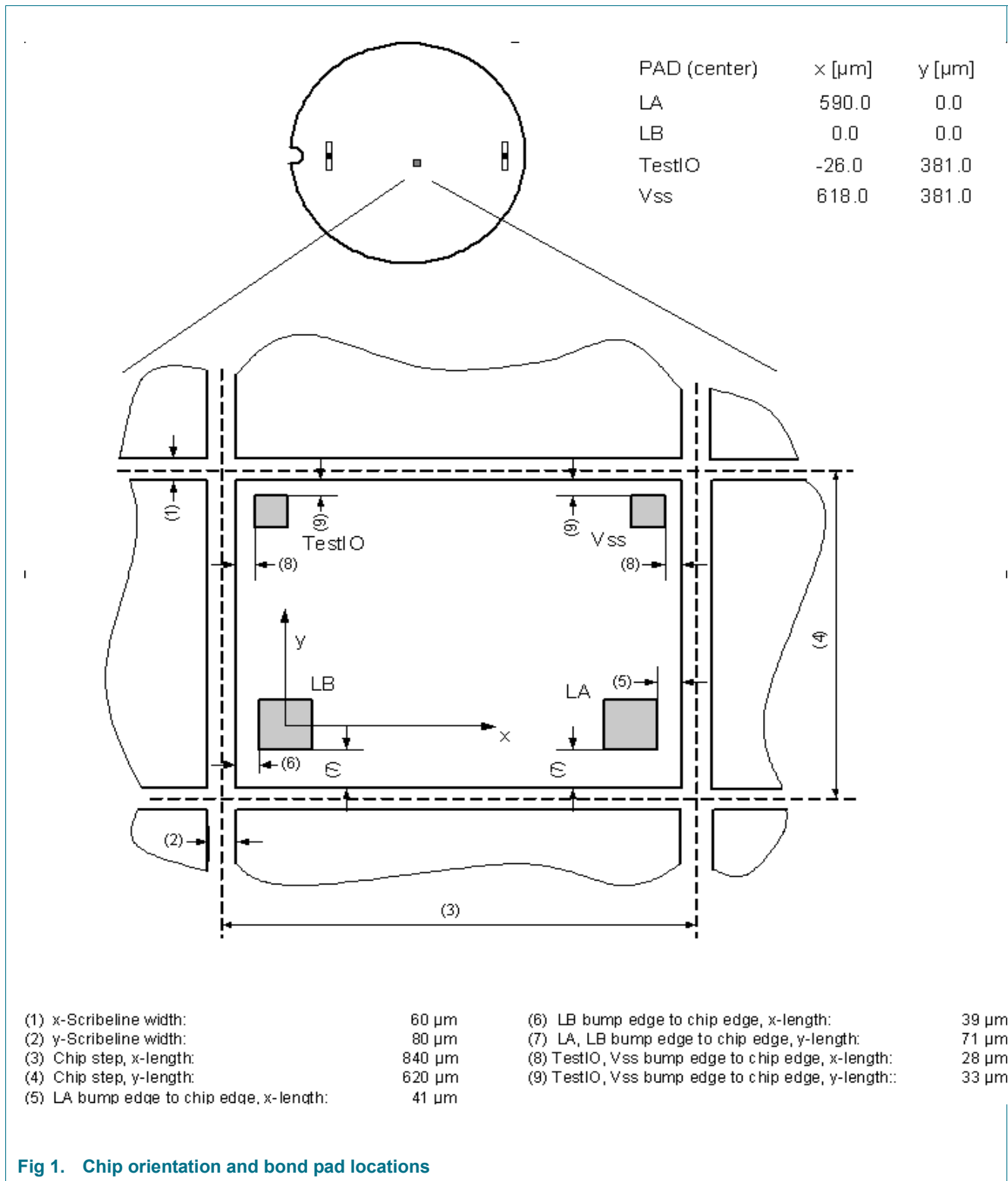


Fig 1. Chip orientation and bond pad locations

7. References

- [Data sheet 'general specification for 8" wafer on UV-tape'](#)
- [Data sheet 'general quality specification'](#)
- [Data sheet 'I-CODE UID-OTP smart label IC, functional specification'](#)
- [Data sheet 'specification of the IBIS wafermap'](#)
- [Application note 'coil design guide'](#)

8. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
134730	January 2007	Initial version		3.0

Modifications:

- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.
- Legal texts have been adapted to the new company name.

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 15 May 2007

Document identifier: 134730