

ERRATA SHEET

Type: P8xC591Vxx/00
Document Release: V1.1
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This errata sheet describes functional anomalies and parametrical deviations from the type specification known at the time of the release of this document.

Each anomaly and deviation is assigned a number and its history tracked at the end of the document.

Functional Deviations

Identification:

The typical P8xC591Vxx/00 devices have the following marking (top):

Line 1	P8xC591VFx/00
Line 2	[batch number]
Line 3	[manufacturing / date code]

INTEGRATED CIRCUITS

Deviation 1: CAN Reset Mode

An anomaly has been found in the CAN part of the device. This anomaly refers to the CAN reset mode (software reset). The external (hardware-) reset is not affected!

Description

The anomaly may occur whenever the user software enters the reset mode during normal operation or if the CAN controller enters the bus-off state.

In this case, the Receive Buffer Status and the Receive Message Counter are reset as specified. However, internal pointers for the RX FIFO and the Transmit Buffer are not reset correctly. As a consequence of this proper operation of the CAN controller after re-entering into operation mode is not given in all cases.

Work-around:

- 1.) It is strongly recommended to empty the RX FIFO before going into CAN reset mode. This is performed with the 'Release Receive Buffer' command.
- 2.) Entering CAN reset mode during a transmission (Transmit Status = 1) or reception (Receive Status = 1) is not allowed! A pending CAN transmission must be terminated (waiting for successful transmission or abort transmission) before the P8xC591VFX/00 may change into the CAN reset mode.

The code for the two cases would look like this:

```
do {
    // read message bytes
    Release Receive Buffer = 1; // empty RXFIFO
} while (RBS == 1);

do {} while (TS); // wait until Transmit Status = 0
do {} while (RS); // wait until Receive Status = 0

Release Receive Buffer = 1; // empty RXFIFO
ResetRequest = 1 // enter reset mode
```

INTEGRATED CIRCUITS

The code for this case would look like this:

```
-----> /* ----- */
          // Error Passive Interrupt or
          /* ----- */

AbortTransmission = 1;          // abort a running transmission

do {
    Release Receive Buffer = 1; // empty RXFIFO
} while (RBS == 1);

do {} while (TS);              // wait until Transmit Status = 0
do {} while (RS);              // wait until Receive Status = 0
Release Receive Buffer = 1;     // empty RXFIFO

Reset Request = 1;            // enter CAN reset mode

RXERR = 0;                    // Receive Error Counter = 0
TXERR = 0;                    // Transmit Error Counter = 0

Reset Request = 0;            // back into operating mode

/* ----- */

// continue normal operation
```

Deviation 2: Idle Mode Timer2 and PWM

An anomaly has been found in the Idle mode of the device. This anomaly inhibits Idle mode functions of Timer 2 and both PWM-channels.

All other P8xC591VFX/00 power saving modes are operating as specified in the data sheet.

Description

In Idle mode, Timer2 counter/timer and its prescaler and PWM1/PWM2 are not reset or halted. As a consequence the power savings in Idle mode (I_{ID}) will be less than specified.

Work-around:

To save power consumption in Idle mode, Timer 2 has to be halted and reset and PWM0 and PWM1 have to be reset.

INTEGRATED CIRCUITS

Deviation 3: ESD sensitivity

The ESD resistance of the VDD pin is proven up to 1.5kV ESD while all other pins resist more than 2kV ESD voltage according to human body model. All pins pass 250V ESD stress according to machine model.

Description

The ESD immunity of the VDD pin is limited to max. 1.5kV (acc human body).

Errata History

#	Published	Problem	Type	Description	Comment
1	2000-02-14	CAN Reset Mode	Function	When the P8xC591Sxx/00 enters CAN reset mode during normal operation, internal pointers may be set wrong.	
2	2000-02-14	Idle Mode T2 and PWM	Function	When the P8xC591Sxx/00 enters the Idle mode, Timer 2 is NOT halted and reset and PWM0/PWM1 is NOT reset.	
3	2000-08-07	ESD	Sensitivity	VDD pin is limited to 1.5kV ESD resistance.	