Accurate Drain Conductance Modeling for Distortion Analysis in MOSFETs

R. van Langevelde and F.M. Klaassen

Electronic Devices Group
Eindhoven University of Technology
Eindhoven, The Netherlands

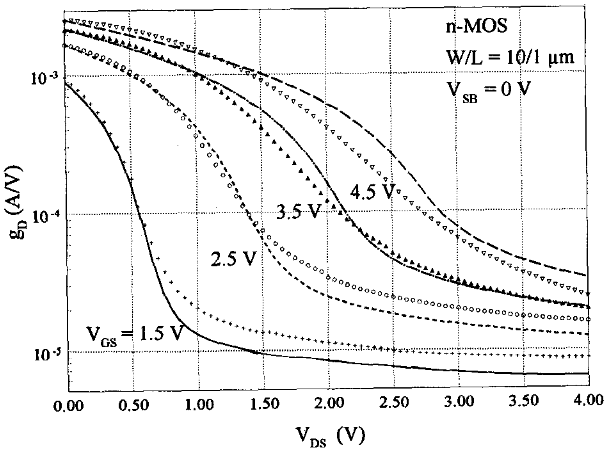
Abstract

Present compact circuit-level MOSFET models fail to accurately describe distortion effects, which is partly due to an imprecise modeling of conductance. A new MOS model has been developed which gives accurate results for distortion analysis, and incorporates a more precise description of various physical phenomena such as velocity saturation, channel length modulation, static feedback and self-heating.

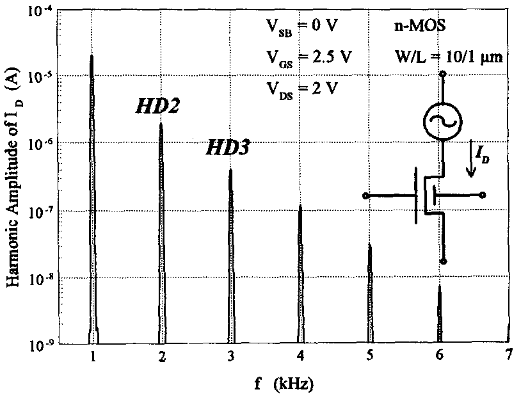
Introduction

For the design of MOSFET-based amplifier and integrator structures the accurate modeling of the bias voltage dependency of drain current I_D and conductance g_D (i.e. dI_D/dV_{DS}) is very important. Nonetheless the accuracy demands for low-distortion applications are even more stringent, especially in RF-applications. When a sinusoidal input signal is applied to a circuit, the output signal will not only contain the ground harmonic but also higher-order harmonics; this is called harmonic distortion. Generally distortion is caused by the higher-order derivatives of the drain current to the terminal voltages. All present compact MOSFET models (such as e.g. BSIM 3v3 [1] and Philips MOS9 [2]) fail to predict distortion effects satisfactorily in analog circuit design. For drain voltage induced harmonic distortion, this is shown in Fig. 1.

For low-distortion applications symmetrical circuits are used so that even-order harmonics are filtered out [3]. In this case the prediction of the DC bias values for which the third-order harmonic becomes zero is important, but as can be seen in Fig. 1 (c) present models completely fail to do this. Consequently an improved circuit-level MOS model is desirable. Such a MOS model is introduced in this paper.



(a)



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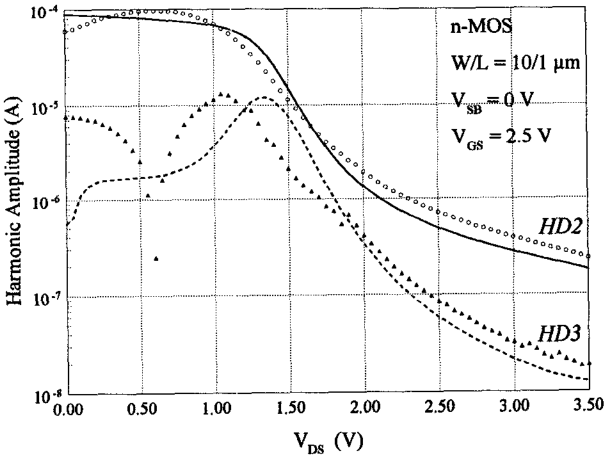

(c)

Fig. 1.: Results of **state-of-the-art** MOS model for a short-channel n-MOS transistor:
(a) Measured (symbols) and modeled (lines) conductance g_D as a function of V_{DS} for different V_{GS}-values.
(b) Measured frequency spectrum of I_D when a perfect sinusoidal voltage ($V_p \sin 2\pi f_0 t$) is applied to the drain terminal. ($V_P = 0.5$ V and $f_0 = 1$ kHz)
(c) Measured (symbols) and modeled (lines) second-order (*HD2*) and third-order (*HD3*) harmonic amplitude as a function of DC drain voltage V_{DS}.

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MOS Model Aspects

A. Drain Current

Generally the MOSFET drain current in strong inversion in the ohmic region can be given using the Gradual Channel Approximation (GCA):

$$I_D = \mu\cdot C_{OX}\cdot\frac{W}{L}\cdot\left[\left(V_{GS}-V_{fb}-2\phi_F-\frac{1}{2}\cdot V_{DS}\right)\cdot V_{DS} -\frac{2}{3}\cdot\gamma\cdot\left(\left(V_{DS}+V_{SB}+2\phi_F\right)^{\frac{3}{2}}-\left(V_{SB}+2\phi_F\right)^{\frac{3}{2}}\right)\right] \quad (1)$$

In most current compact MOSFET models (1) is simplified using a first-order Taylor expansion around V_{SB}:

$$I_D = \mu\cdot C_{OX}\cdot\frac{W}{L}\cdot\left[V_{GS}-V_{T_0}-\frac{1}{2}\cdot(1+\delta)\cdot V_{DS} -\gamma\cdot\left(\sqrt{V_{SB}+2\phi_F}-\sqrt{2\phi_F}\right)\right]\cdot V_{DS} \quad (2)$$

where the body parameter δ is dependent on channel length L and back-bias V_{SB}. In principle (2) can be maintained in the saturation region by introducing an internal saturation voltage V_{DSAT}.

In (1) μ denotes the channel mobility, which is gate-voltage dependent due to mobility degradation. Mobility degradation affects the transconductance g_m (i.e. dI_D/dV_{GS}) and thus the gate voltage induced harmonic distortion in MOS circuits. A precise, more physical model for mobility degradation has been accomplished recently [4]. Fig. 2 demonstrates that this leads to a much improved description of harmonic distortion.. Here also a gate voltage dependent series-resistance was taken into account for short-channel transistors [5].

The main advantage of (2) compared to (1) is that additional information on threshold voltage such as geometry dependence and effect of non-uniform substrate doping can be easily implemented. In fact threshold voltage can be easily extracted from DC-measurements.

When examining (2) for distortion analysis, it is clear that in the ohmic region the third-order derivative (i.e. d^3I_D/dV_{DS}^3) equals zero for all voltages, which is non-physical. For a more accurate description of the higher-order derivatives (1) can be expanded around $V_{SB}+½\cdot V_{DS}$ instead of V_{SB}, which results in:

$$I_D = \mu\cdot C_{OX}\cdot\frac{W}{L}\cdot\left[V_{GS}-V_{T_0}-\frac{1}{2}\cdot V_{DS} -\gamma\cdot\left(\sqrt{V_{SB}+\frac{1}{2}\cdot V_{DS}+2\phi_F}-\sqrt{2\phi_F}\right)\right]\cdot V_D \quad (3)$$

where all previous information on threshold voltage still can be used.

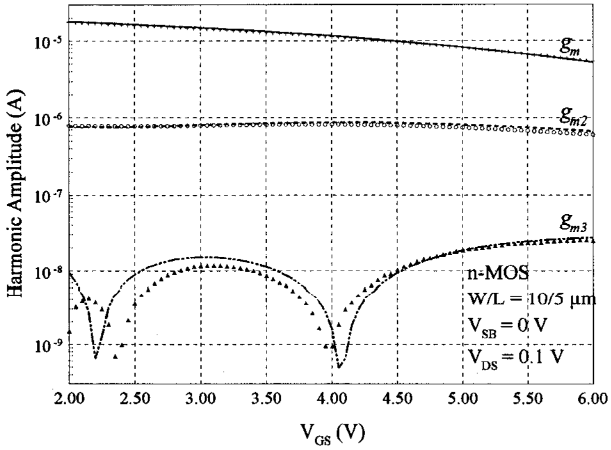


Fig. 2. Measured (symbols) and modeled (lines) first-order $\{g_m\}$, second-order $\{g_{m2}\}$ and third-order $\{g_{m3}\}$ harmonic amplitude as a function of gate voltage V_{GS} when a perfect sinusoidal voltage ($V_p\sin 2\pi f_0 t$) is applied to the gate terminal. Results are shown for an n-type MOS transistor (V_P = 1 V and f_0 = 1 kHz) using a new model for mobility degradation and gate voltage dependent series-resistance introduced in [4].

For short-channel transistors (3) becomes inaccurate, as the electric field along the channel E_y can reach large values, and velocity saturation has to be taken into account. Furthermore in the saturation region GCA no longer holds, which becomes apparent in physical phenomena such as Channel Length Modulation (CLM) and Static Feedback. In addition heat dissipation increases with decreasing channel length, which may result in self-heating.

For a good description of distortion behavior a more accurate description of all above phenomena has to be implemented in a new MOS model.

B. Velocity Saturation

Carrier velocity is often expressed by the following empirical relation [6]:

$$v = \frac{\mu\cdot E_y}{\left[1+\left(\frac{\mu}{v_{sat}}\cdot E_y\right)^{\alpha}\right]^{1/\alpha}} \quad (4)$$

where $\alpha = 2$ for electrons and $\alpha = 1$ for holes, and v_{sat} is the saturation velocity limited by optical phonon scattering. In most MOS-models $\alpha = 1$ is used for both electrons and holes, as it leads to an analytically solvable equation for drain current. A numerical problem occurring for other values of α may be circumvented by assuming that in first-order approximation E_y equals V_{DS}/L.

For holes however, it was found that the Scharfetter and Gummel expression [7] gives more accurate results:

$$v = \mu\cdot E_y\cdot\left[1+\frac{\left(\frac{\mu}{v_c}\cdot E_y\right)^2}{G+\frac{\mu}{v_c}\cdot E_y}+\left(\frac{\mu}{v_{sat}}\cdot E_y\right)^2\right]^{-1/2} \quad (5)$$

where v_c is a parameter corresponding to the velocity of the longitudinal acoustic phonons and G is a fitting parameter. Note that for $v_c \to \infty$ (5) reduces to the velocity equation for electrons, (4) with $\alpha = 2$.

C. Channel Length Modulation

When V_{DS} is larger than V_{DSAT}, the velocity saturation or pinch-off point moves towards the source, causing effectively that the channel length L is shortened by a length ΔL. A pseudo-2D analysis [8] shows that ΔL can be written as:

$$\frac{\Delta L}{L} = \frac{l_c}{L_{eff}}\cdot\ln\left(\frac{V_{DS}-V_{DSAT}+\sqrt{\left(V_{DS}-V_{DSAT}\right)^2+E_{SAT}^{\,2}\cdot l_c^{\,2}}}{E_{SAT}\cdot l_c}\right) \quad (6)$$

where E_{SAT} is the electric field at the saturation point, and l_c is dependent on oxide thickness and substrate doping concentration. Using e.g. equation (5), the effective channel length L_{eff} can be written as:

$$L_{eff} = \sqrt{L^2 + \frac{\left(\frac{\mu}{v_c}\cdot V_{DSAT}\right)^2}{G + \frac{\mu}{v_c}\cdot\frac{V_{DSAT}}{L}} + \left(\frac{\mu}{v_{sat}}\cdot V_{DSAT}\right)^2} \qquad (7)$$

D. Static Feedback

Extensive two-dimensional device simulations show that in the saturation region the inversion-layer charge increases with increasing drain voltage V_{DS}. This effect is ascribed to the electrostatic coupling between drain and channel region, it is often described as a linear threshold voltage shift with drain voltage [9]. For the above shift it was found empirically that:

$$\Delta V_T = \frac{-\sigma\cdot\sqrt{V_{DSAT}}\cdot V_{DS}}{L} \qquad (8)$$

where σ is a parameter. ΔV_T is not dependent on back bias V_{SB}.

E. Self-Heating

Self-heating may affect drain current significantly in submicron devices at high gate voltage values. The channel temperature in MOSFETs increases linearly with dissipated power [10]:

$$T = T_0 + R_{Th}\cdot I_D\cdot V_{DS} \qquad (9)$$

where T_0 is the ambient temperature and R_{Th} is the thermal resistance of the device. Naturally the latter affects the mobility. The thermal dependence of mobility is given by:

$$\mu(T) = \mu(T_0)\cdot\left(\frac{T}{T_0}\right)^{-k} \approx \mu(T_0)\cdot\left(1 - \frac{k\cdot R_{Th}\cdot I_D\cdot V_{DS}}{T_0}\right) \qquad (10)$$

where k is different for electrons and holes and has a value between 1.5 and 2.0. Assuming that all other electrical parameters change much less with temperature, equation (10) can be incorporated into the current equation (3) in the same way as was done with series-resistance [4].

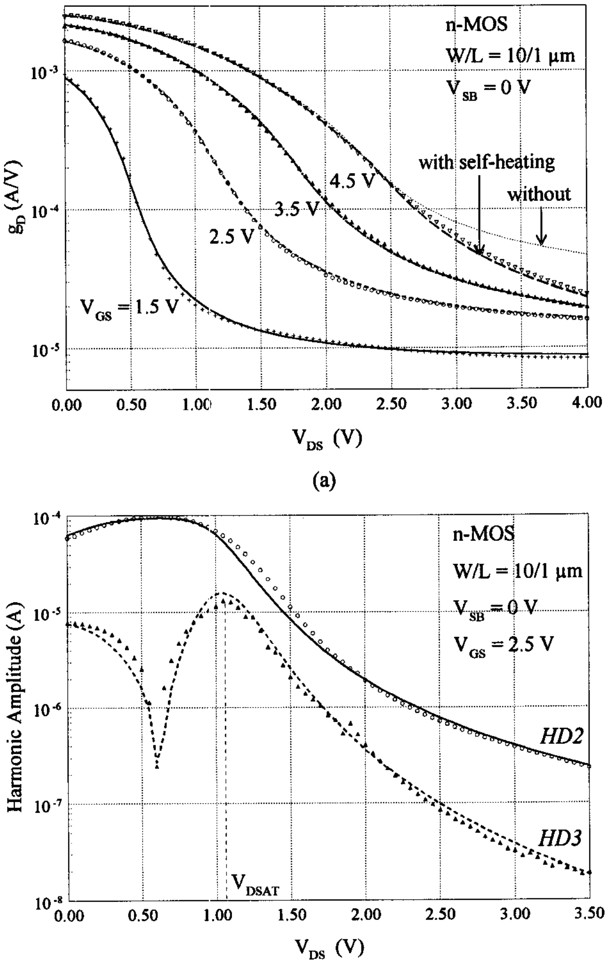
Equations (4)-(10) can be easily incorporated into the drain current equation (3). Here the division between ohmic region and saturation region is given by the saturation voltage V_{DSAT}, which can be calculated with some approximations in the usual way [6] using (3) and (5). It can be shown that the third-order derivative (i.e. d^3I_D/dV_{DS}^3) becomes maximum at $V_{DS} = V_{DSAT}$. The latter provides an additional check on the model accuracy.

Results and Discussion

For distortion measurements the set-up as described in [3] was used. Measurements were performed on both n-type and p-type MOSFETs from a commercially available submicron process. The n-channel MOSFETs have an LDD-structure, and the p-channel MOSFETs are of the buried type. The gate oxide thickness is about 150 Å. Measurements were done as a function of V_{DS} for a channel length range of minimum length 0.8 μm up to 10 μm, a gate voltage range of V_T + 0.25 V up to 4.5 V and a bulk voltage range of 0 V up to 5 V.

In the ohmic region for long-channel transistors the distortion behavior is mainly determined by the threshold voltage parameters (V_{T0}, γ and ϕ_F), which are extracted from I_D-V_{GS}-curves for V_{DS} = 0.1 V. For short-channel transistors in particular the velocity saturation parameters (G, v_c and v_{sat}) are responsible for a better description of distortion behavior. The drain current in saturation is affected by CLM, Static Feedback and self-heating. However as the latter two are linearly dependent on V_{DS}, only the CLM-equation (6) determines the higher-order derivatives and thus the distortion behavior. It was found that appropriate values for the parameters E_{SAT} and l_c give precise results for distortion analysis for the complete channel length and voltage range under consideration.

The results of the new MOS model can be seen in Fig. 3. (a) and (b) for a short-channel n-MOS transistor. The behavior in the ohmic region, notably the zero-crossing of the third-order harmonic, is determined by the description of velocity saturation (4) with α = 2. Furthermore it should be noted that the third-order harmonic becomes maximum at $V_{DS} = V_{DSAT}$. Incorporation of self-heating in the saturation region leads to a more accurate modeling of conductance at high V_{GS} values.
In Fig. 4, the higher-order harmonic results for a long-channel n-MOS transistor are shown. Here the drain voltage dependence of (3) dominates the behavior in the ohmic region; as a result there is no zero-crossing of the third-order harmonic.



(a)

(b)

Fig. 3.: Same measurement results (symbols) as in Fig. 1 (a) and (c), simulation results (lines) of new MOS model.

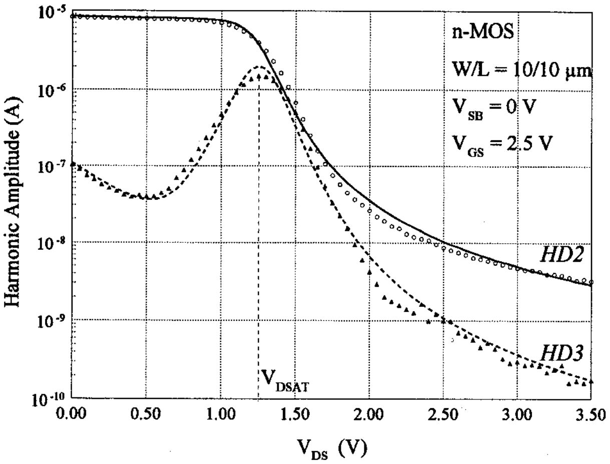


Fig. 4.: Results of the **new** MOS model for a long-channel n-MOS transistor. Measured (symbols) and modeled (lines) second-order (*HD2*) and third-order (*HD3*) harmonic of I_D when a sinusoidal voltage ($V_p \sin 2\pi f_0 t$) is applied to the drain terminal, as a function of DC drain voltage V_{DS}. (V_P = 0.5 V and f_0 = 1 kHz).

In saturation only Channel Length Modulation and Static Feedback determine the conductance, as heat dissipation is negligible for long-channel transistors.

For short-channel p-MOS transistors the results of the new MOS model are given in Fig. 5. In the ohmic region appropriate values for v_c and G result in an accurate description of the third-order harmonic; v_{sat} is only of minor importance.

Conclusions

Drain voltage induced harmonic distortion in the MOSFET drain current is mainly determined by velocity saturation in the ohmic region and Channel Length Modulation in the saturation region. Apart from this, for a correct conductance-modeling in saturation, Static Feedback and to a lesser extent self-heating have to be incorporated in the MOS model. The latter is only important for short-channel transistors.

In general the new MOSFET-model gives very accurate results for the drain current, the conductance and its higher-order derivatives for both n-type and p-type MOS transistors for a wide range of channel length, drain voltage, gate voltage and bulk voltage values using one scalable parameter set. For instance the important parameters G, v_c, v_{sat}, E_{sat}, l_c and σ are independent of channel length.

From a circuit design point of view, as distortion is maximum here, one should try to avoid biasing a MOS transistor at $V_{DS} = V_{DSAT}$ for low-distortion applications.

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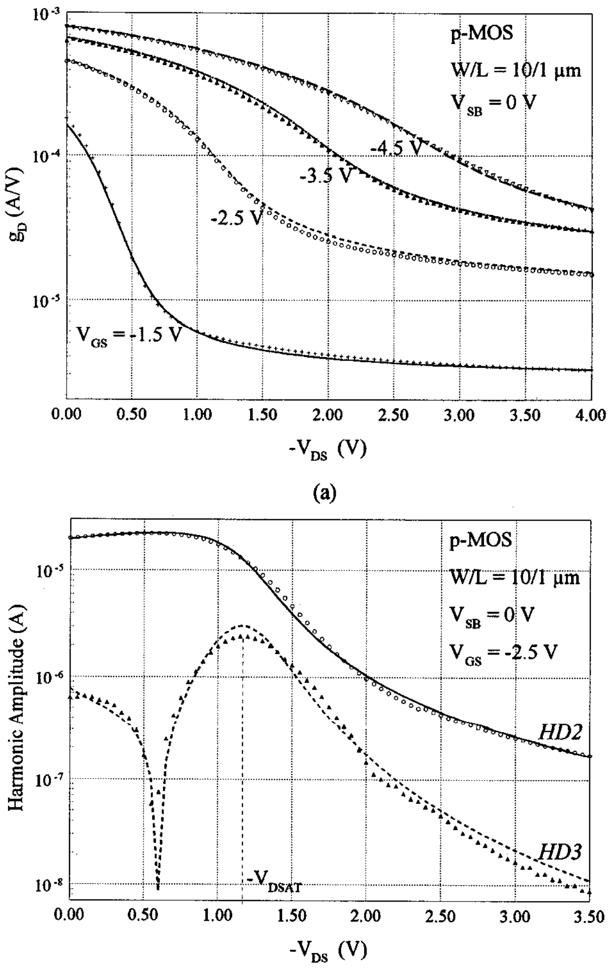

(a)

(b)

Fig. 5.: Same as Fig. 3, for short-channel p-type MOS transistor.