RF-Distortion in Deep-Submicron CMOS Technologies

R. van Langevelde, L.F. Tiemeijer, R.J. Havens, M.J. Knitel, R.F.M. Roes, P.H. Woerlee and D.B.M. Klaassen
Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands
Phone: +31-40-2743926; Fax: +31-40-2743390; E-mail: ronald.van.langevelde@philips.com

Abstract

The distortion behaviour of MOSFETs is important for RF-applications. In this paper the influence of technology variations (oxide thickness, substrate doping,...) on distortion is investigated using measurements and a recently developed compact MOSFET model. The influence on distortion of technology scaling down to 0.18μm is verified and further scaling according to the ITRS-roadmap is predicted.

Introduction

CMOS has become a serious option for wireless RF applications. An attractive feature of MOS devices is the high linearity (i.e. low distortion behaviour). System requirements on linearity become more stringent for future wideband RF applications such as 3G mobile terminals. In addition there is a trade-off between linearity and power consumption. Whether the superior linearity of MOSFETs is preserved with scaling according to the ITRS-roadmap [1] has not yet been published. **Here** we investigate the influence of technology variations (oxide thickness t_{ox}, substrate doping N_A, etc.) on MOSFET distortion behaviour. A recently developed compact MOS model [2,3] is validated on all variations and used to disentangle the different physical effects. Next the impact of technology scaling on distortion over 3 industrial CMOS generations is discussed, combining the effects of the above technology variations. Finally the effect of technology scaling following the ITRS-roadmap on distortion is verified and predicted.

Experimental Method and Linearity Figure of Merit

The distortion behaviour of a MOSFET in an amplifier structure is shown in Fig. 1. In circuits, using balanced topologies, even-order harmonics can be reduced by about 40dB. As a result the 3rd-order harmonic forms a lower limit for the total distortion. Both measurements and simulations indicate that MOSFET distortion does not change much with frequency up to 1GHz ([3], see Fig. 2), implying that RF-distortion is determined by the 3rd-order derivative of the drain current I_D to gate voltage V_{GS}. For typical analog bias conditions, i.e. $0.1\text{V} < V_{GS} - V_T < 0.6\text{V}$, a linearity figure of merit (FoM), which can be determined from dc measurements, is defined as [4]: $VIP_3 = \sqrt{24 \cdot g_m / g_{m3}}$. Here g_m is the transconductance and g_{m3} is $\partial^3 I_D / \partial V_{GS}^3$; both can be determined numerically. VIP_3 is the extrapolated input gate bias amplitude at which the 1st and 3rd-order output amplitudes (of drain current) are equal. For low-distortion operation VIP_3 should be as high as possible.

MOSFET Model for Distortion Analysis

The compact MOSFET model named MOS Model 11, the successor to MOS Model 9 [5], has been developed in order to accurately describe the higher-order derivatives of the drain current to any terminal voltage. It is *i)* symmetric; *ii)* surface-potential based; and *iii)* uses improved expressions for mobility reduction and velocity saturation as compared to contemporary models such as BSIM3v3 [6] and MOS Model 9. The superior distortion description of this model has been verified at low [2] and high frequencies [3], see Fig. 2. Since its original publication [2] the model has been improved on several details, a.o. poly depletion and quantum-mechanical effects have been included.

Technology Variations

MOS transistors have been investigated from a batch with *i)* physical oxide thickness t_{ox} between 2 and 10nm; and *ii)* substrate doping N_A equal to $5\times10^{16}\text{cm}^{-3}$ and $5\times10^{17}\text{cm}^{-3}$. On a different batch the pocket implantation dose has been varied between $4\times10^{12}\text{cm}^{-2}$ and $1.2\times10^{13}\text{cm}^{-2}$. At low gate drive VIP_3 is independent of drain bias (see Fig. 3), and correlates with the third-order output intercept point OIP_3 (see Fig. 2). An arbitrary V_{DS} value of 1.5 V has been chosen. In all figures symbols indicate measured results and lines indicate model results.

- Influence of Channel Length L

In general, with increasing gate bias, VIP_3 increases to a maximum value (i.e. $g_{m3} = 0$) followed by a local minimum, see Fig. 4. With decreasing channel length the maximum in VIP_3 shifts to lower V_{GS} and its local minimum decreases. Simulations show that this is caused by the increasing effect of series resistance and velocity saturation, see Fig. 5. The optimum bias condition for low-distortion is sensitive to (statistical) variation of threshold voltage, and may not be useful without special circuit measures.

- Influence of Oxide Thickness t_{ox}

The local minimum in VIP_3 decreases with oxide thickness t_{ox}, see Fig. 6, due to a decrease of the body effect and an increase in poly depletion. At high values of gate bias VIP_3 is independent of oxide thickness; here distortion is determined by velocity saturation. The position of the maximum VIP_3 is independent of effective gate bias and drain current, see Figs. 6 and 7.

- Influence of Substrate Doping N_A

The local minimum in VIP_3 increases with substrate doping N_A, see Fig. 8, which is due to an increase in body effect. The maximum VIP_3 shifts to higher effective gate bias values.

0-7803-6438-4/00/$10.00 ©2000 IEEE

- Influence of Pocket Implants

Pockets do affect the output conductance and consequently the voltage gain of MOS devices [7]. The linearity FoM, however, is independent of conductance, and as a result it is hardly affected by pocket implants, see Fig. 9 where the pocket implantation dose has been varied between $4\times10^{12}cm^{-2}$ and $1.2\times10^{13}cm^{-2}$.

Full Technology Scaling

In Fig. 10 (a) and (b) VIP_3 is shown for NMOS resp. PMOS transistors in 0.35μm, 0.25μm and 0.18μm industrial CMOS technologies. The scaling trend is similar for both NMOS and PMOS. The local minimum decreases with technology scaling. Although t_{ox} decreases and N_A increases, the body effect decreases moderately resulting in a slight increase in distortion. Due to the applied scaling scheme, poly depletion has no effect on distortion. The remaining increase in distortion is thus caused by an increased influence of series resistance and velocity saturation. At constant drain current, VIP_3 decreases (i.e. distortion increases) with technology downscaling, see Fig. 11. The same distortion is obtained only at higher drain current levels. To maintain the same current level, the channel width has to be scaled down. The impact of the ITRS roadmap [1] on distortion has been investigated by scaling the model parameters accordingly, the result is shown in Fig. 12. The linearity FoM decreases a factor of 2 over 7 technology generations. For future generations the effect of series resistance on distortion becomes almost negligible.

Conclusions

The impact of technology variations and scaling on distortion has been investigated. Our improved MOS model gives an accurate description of all distortion scaling trends, and provides insight into the underlying physical effects. Effects of velocity saturation and body effect become more important with technology scaling. For typical analog bias conditions this results in a moderate deterioration of MOSFET distortion behavior when scaled according to the ITRS-roadmap.

References

[1] International Technology Roadmap for Semiconductors, 1999 Edition: www.itrs.net/1999_SIA_Roadmap/Home.htm

[2] R. van Langevelde and F.M. Klaassen, "Accurate Drain Conductance Modeling for Distortion Analysis in MOSFETs," IEDM Tech. Dig., pp. 313-317, 1997; ibid., Ph.D. Thesis, Univ. of Techn. Eindhoven, 1998.

[3] L.F. Tiemeijer *et al.*, "RF Distortion Characterisation of Sub-Micron CMOS," Proceedings ESSDERC, pp. 464-467, 2000.

[4] P.H. Woerlee, R. van Langevelde, A.H. Montree, D.B.M. Klaassen, L.F. Tiemeijer and P.W.H. de Vreede, "RF-CMOS Performance Trends," Proceedings ESSDERC, pp. 576-579, 2000.

[5] MOS Model 9, see: www.semiconductors.philips.com/Philips_Models/

[6] BSIM3v3, see: www-device.eecs.berkeley.edu/~bsim3

[7] R.F.M. Roes, A.C.M.C. van Brandenburg, A.H. Montree and P.H. Woerlee, "Implications of Pocket Optimisation on Analog Performance in Deep Sub-Micron CMOS," Proceedings ESSDERC, pp. 176-179, 1999.

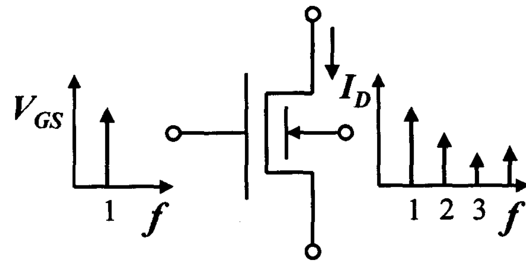
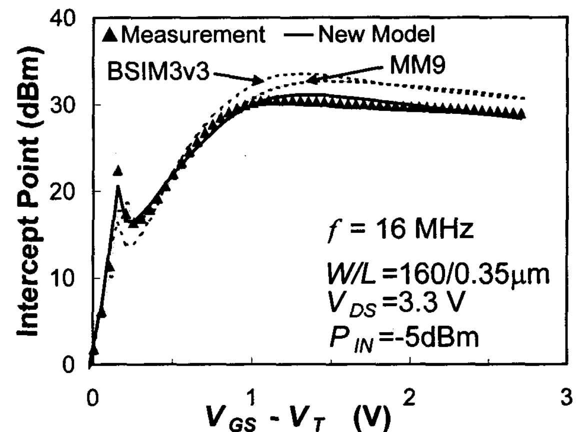
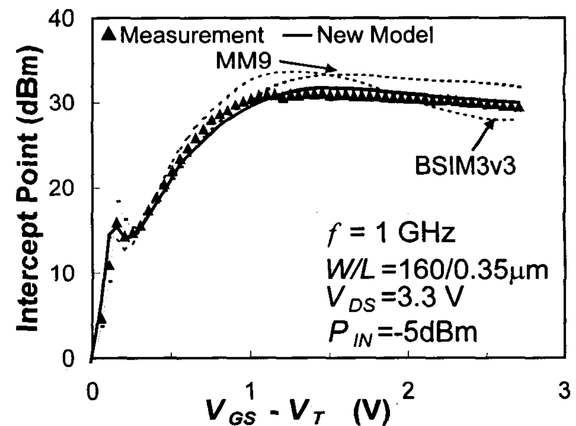


Fig. 1: A sinusoidal gate voltage V_{GS} results in a distorted drain current I_D containing not only the ground harmonic but also unwanted higher-order harmonics, due to the non-linear dependence of I_D on V_{GS}.



(a)



(b)

Fig. 2: Third-order output intercept point OIP_3 (i.e. extrapolated output power at which 1st and 3rd-order harmonic output power are equal) of short-channel *n*-MOS transistor for **frequencies** of (a) *f*=16 MHz, and (b) *f*=1 GHz.

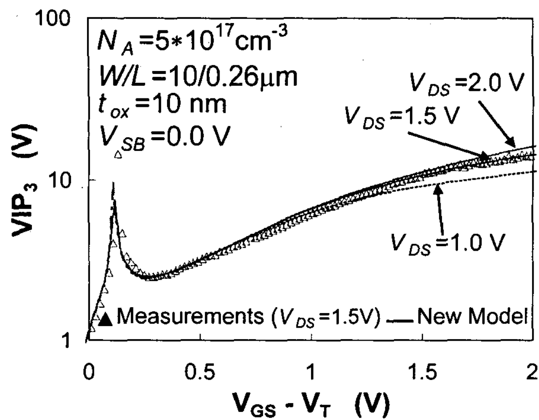


Fig. 3: Influence of **drain bias V_{DS}** on VIP_3 for n-type short-channel MOSFET. In the bias range of interest (i.e. 100mV < V_{GS}-V_T < 600mV) VIP_3 does not change much with varying drain bias.

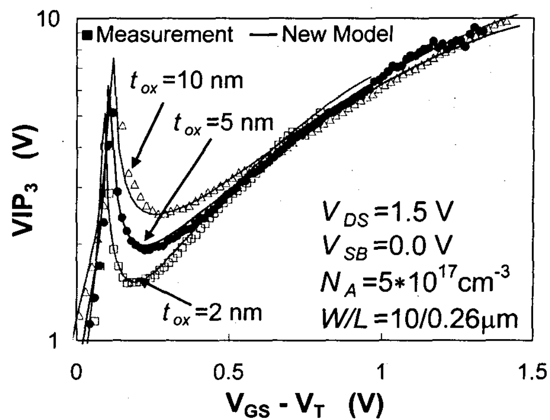


Fig. 6: VIP_3 as a function of effective gate bias for n-type short-channel MOSFETs with different values of **oxide thickness t_{ox}**. The local minimum in VIP_3 decreases with decreasing oxide thickness.

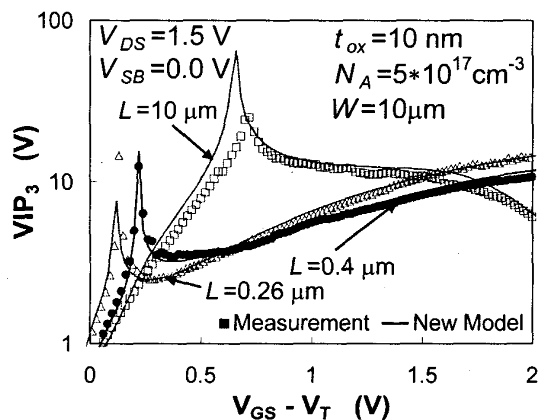


Fig. 4: VIP_3 as a function of effective gate bias for n-type MOSFETs with different values of **channel length L**. Above threshold VIP_3 increases to a maximum value, where distortion is minimum.

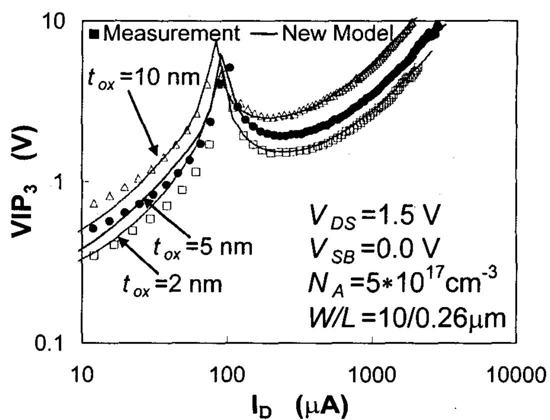


Fig. 7: VIP_3 same as in Fig. 6 now as a function of drain current I_D. For a constant value of I_D distortion increases with decreasing **oxide thickness t_{ox}**. The maximum in VIP_3 occurs at same value of I_D.

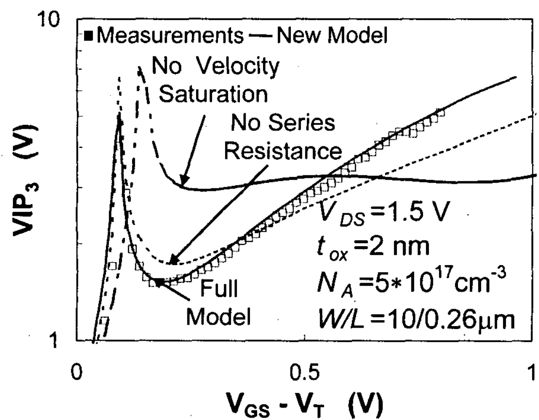


Fig. 5: Influence of **series resistance** and **velocity saturation** on the distortion behaviour of an n-type short-channel MOSFET. The local minimum in VIP_3 decreases when the above effects become more important.

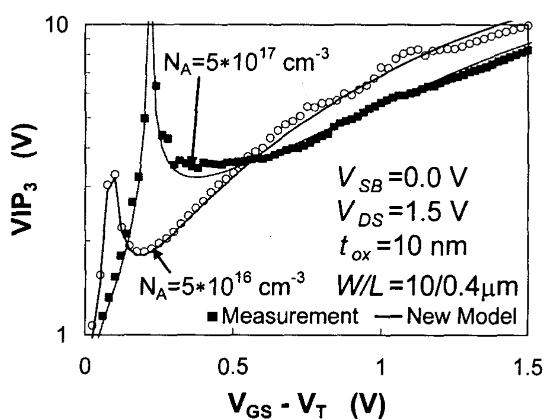


Fig. 8: VIP_3 as a function of effective gate bias for n-type short-channel MOSFETs with different values of **substrate doping N_A**. Minimum in VIP_3 increases with substrate doping N_A.

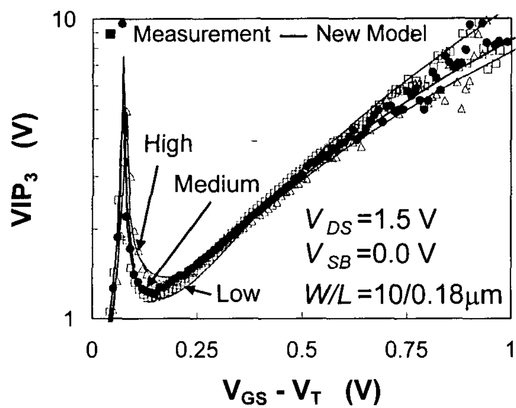


Fig. 9: VIP_3 as a function of effective gate bias for *n*-type short-channel MOSFETs where the **pocket implantation dose** has been varied (high, medium and low dose).

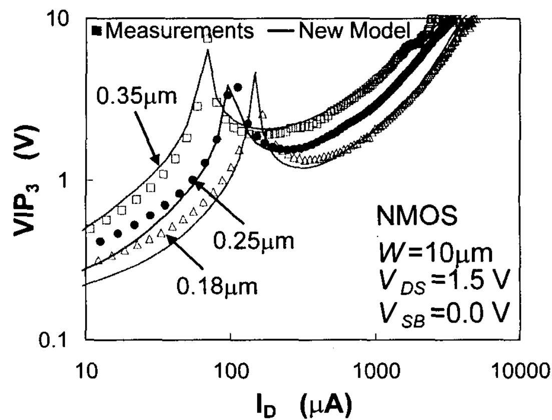
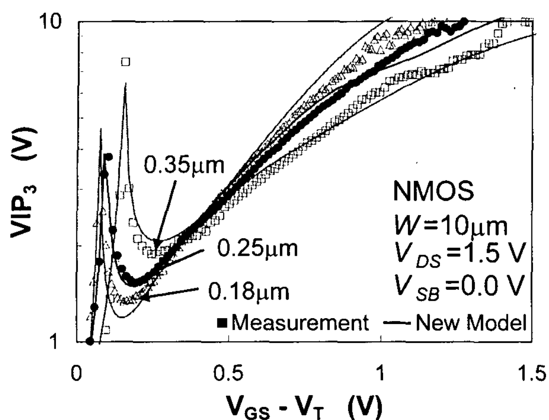
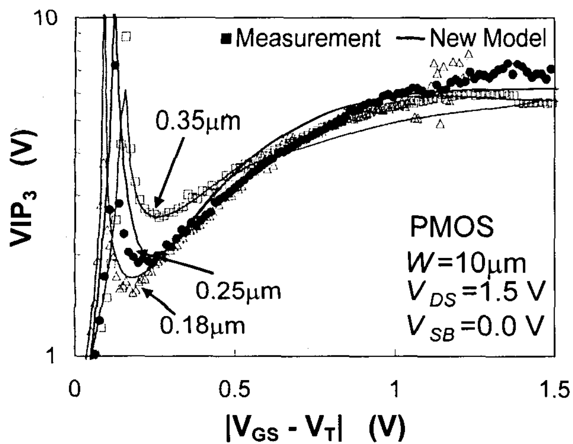


Fig. 11: VIP_3 same as in Fig. 10 (a) now as a function of drain current I_D. For constant I_D distortion increases with **technology downscaling**.



(a)



(b)

Fig. 10: VIP_3 as a function of effective gate bias for (a) *n*-type and (b) *p*-type short-channel MOSFETs in **0.35μm, 0.25μm and 0.18μm CMOS-technology**.

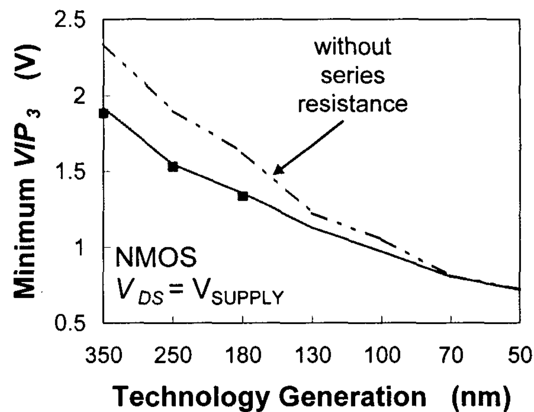


Fig. 12: Lines: compact model calculations for minimum VIP_3 following from ITRS-specifications, with and without series resistance. Symbols: measurements taken from Figs. 10 and 11.