

# Accurate Thermal Noise Model for Deep-Submicron CMOS

A.J. Scholten, H.J. Tromp, L.F. Tiemeijer, R. van Langevelde, R.J. Havens, P.W.H. de Vreede, R.F.M. Roes, P.H. Woerlee, A.H. Montree, and D.B.M. Klaassen

Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands  
Phone: +31-40-2742723; Fax: +31-40-2743390; E-mail: andries.scholten@philips.com

## Abstract

Extensive measurements of drain current thermal noise are presented for 3 different CMOS technologies and for gate lengths ranging from  $2\ \mu\text{m}$  down to  $0.17\ \mu\text{m}$ . Using a surface-potential-based compact MOS model with improved descriptions of carrier mobility and velocity saturation, all the experimental results can be described accurately without invoking carrier heating effects or introducing additional parameters.

## Introduction

Accurate modelling of high-frequency noise is a prerequisite for the application of modern CMOS technologies to low-noise RF circuit design. In a number of publications, a considerably enhanced thermal noise in submicron MOSFETs has been reported, which was attributed to hot-carrier effects [1,2]. Abidi [1] found that the thermal noise of an  $0.7\ \mu\text{m}$  n-channel MOSFET was enhanced by more than a factor of 10 (at specific bias conditions) compared to the long-channel theoretical result. Recently, a similar enhancement was observed by Klein [2] on  $0.65\ \mu\text{m}$  n-channel MOSFETs, while for p-channel MOSFETs a somewhat smaller enhancement was found. Device simulations seem to confirm these results [3]. In **this paper**, the drain current thermal noise of deep-submicron MOSFETs is studied experimentally by a thoroughly verified method for  $0.35\ \mu\text{m}$ ,  $0.25\ \mu\text{m}$  and  $0.18\ \mu\text{m}$  CMOS processes. Using a surface-potential-based compact MOS model [4], which incorporates improved descriptions of carrier mobility and velocity saturation, all our experimental results can be described accurately *without* invoking carrier heating effects or introducing additional parameters.

## Experimental Setup

Drain current thermal noise is investigated at intermediate frequencies, where  $1/f$  noise can be neglected. As the minimum noise figure  $F_{\min}$  decreases linearly with decreasing frequency, at these relatively low frequencies  $F_{\min}$  is close to 0 dB [5]. Therefore, instead of  $F_{\min}$ , we measure  $F_{50}$ , the noise figure at  $50\ \Omega$  generator impedance, which is much larger than  $F_{\min}$ , and dominated by the MOSFET drain current thermal noise, as can be seen in Fig. 1.

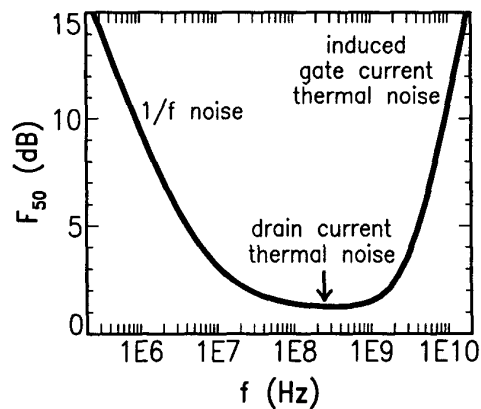


Figure 1: Simulated 50-Ohm noise figure vs. frequency, for a  $1000/0.25\ \mu\text{m}$  n-channel MOSFET. The various contributions to the noise figure are indicated. Measurements are performed at 248 MHz (indicated by arrow), where both  $1/f$ -noise and induced gate current thermal noise are small.

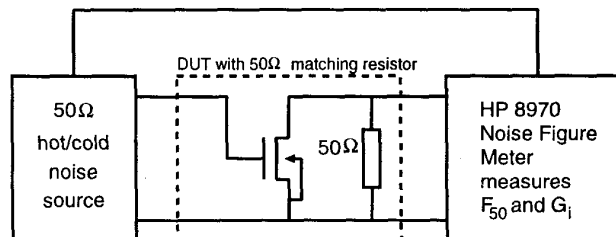


Figure 2: Principle of the experimental setup. Note the  $50\text{-}\Omega$  matching resistor needed for proper correction of the background noise of the noise meter. In the actual experiment, bias tees are used for DC-biasing of the device.

The measurements are performed using a conventional noise figure test set (Fig. 2), which measures both the 50-Ohm noise figure  $F_{50}$ , and the insertion gain  $G_i$ . A 50  $\Omega$  resistor is needed to match the output impedance to the noise figure meter input. The measurements are performed on-wafer at a frequency of 248 MHz. For all the measurements, it was verified experimentally that this frequency is in the regime where  $F_{50}$  is dominated by drain current thermal noise (cf. Fig. 1). Besides the noise measurements, standard DC-characterization has been performed in order to determine the compact model parameters for each device.

In the analysis, both  $F_{50}$  and  $G_i$  are calculated using a circuit simulator in which the compact model [4] mentioned above, has been implemented. Before analyzing the measured noise figures, it is of great importance to verify the modelling of  $G_i$  first: accurate modelling of  $G_i$  corroborates the validity of the compact model which is used to describe the MOSFET. Moreover, there is a direct relationship between noise figure and gain, so that the calculated value of  $G_i$  directly affects the prediction of  $F_{50}$ .

Besides the noise contribution of the MOSFET itself, all the device and interconnect parasitics, RF-probes, cables and biases and the 50  $\Omega$  matching resistor have been characterized experimentally and included in the simulation. In case of short-channel MOSFETs, which are of interest here, the dominating noise contribution is the noise of the MOSFET, as shown in Fig. 3.

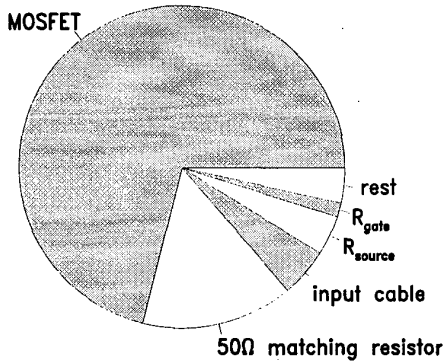


Figure 3: Contributions to the measured noise figure for a  $16 \times 10/0.35 \mu\text{m}$  n-channel MOSFET, biased at  $V_{GS} = V_{DS} = 3.3 \text{ V}$ .

#### Thermal noise model

Using the Langevin method, it can be shown [6] that the spectral noise density of the MOS drain current,  $S_{I_D}(f)$ , is given by:

$$S_{I_D}(f) = \frac{1}{I_D L^2} \cdot \int_0^{V_{DS(AT)}} 4k_B T_e \cdot g(V)^2 dV \quad (1)$$

where  $T_e$  is the temperature of the charge carriers (see below),

and  $g(V)$  is given by

$$g(V) = W \mu Q_i(V) \quad (2)$$

where  $V$  is the quasi-Fermi potential, and  $Q_i(V)$  is the inversion charge density. The effect of velocity saturation on the mobility  $\mu$  is given by

$$\mu = \frac{\mu_{\text{eff}}}{\left[1 + \left(\frac{E}{E_c}\right)^p\right]^{1/p}} \quad (3)$$

where  $E_c$  is the critical field,  $\mu_{\text{eff}}$  is the effective mobility, and  $p = 1$  and  $2$  for p-channels and n-channels, respectively [4].

The temperature of the charge carriers,  $T_e$ , is often thought to be elevated with respect to the lattice temperature  $T$  [1, 2]. The dependence of  $T_e$  on lateral electric field is usually modelled by

$$T_e = T \cdot \left(1 + \frac{E}{E_c}\right)^n \quad (4)$$

where  $n$  varies between 0 and 2 [7]. Evidently,  $n = 0$  corresponds to the absence of charge carrier heating. Using the above equations,  $S_{I_D}(f)$  has been calculated for  $n = 0, 1$  and  $2$ , in the framework of a recently developed surface-potential-based compact model [4].

#### Experimental results

In Figs. 4 and 5,  $F_{50}$  and  $G_i$  measured for n- and p-channel devices with different gate lengths, processed in  $0.35 \mu\text{m}$  technology, are compared to simulations using  $n = 0$ , i.e. without carrier heating effects. In Figs. 6 and 7 the same comparison is made for minimum length NMOS devices taken from  $0.25$  and  $0.18 \mu\text{m}$  technologies. For all devices the modelling of both  $G_i$  and  $F_{50}$  is excellent.

As carrier heating is switched on ( $n = 1$  or  $2$ ), systematic deviations between simulations and experiments are introduced, as shown in Fig. 8 for the  $0.17 \mu\text{m}$  NMOS device. Clearly, the best agreement is obtained when carrier heating is switched off ( $n = 0$ ). Because this observation is in contradiction with refs. [1-3], we extracted the so-called white noise  $\gamma$ -factor [1] from our measurements (see Fig. 9). The white noise  $\gamma$ -factor is, as usual, defined by

$$\gamma \equiv \frac{S_{I_D}(f)}{4k_B T g_{d0}} \quad (5)$$

where  $g_{d0}$  is the output conductance at zero drain bias [1]. For a gate length of  $2 \mu\text{m}$ , and in the saturation region,  $\gamma$  is observed to be equal to the long-channel theoretical result of  $\frac{2}{3}$ , which corroborates our experimental procedure. For n-channel devices with gate length as short as  $0.17 \mu\text{m}$   $\gamma$  values between 1 and 2 are found due to velocity saturation. Note however, that the order-of-magnitude increase in  $\gamma$ , as observed in refs. [1,2] is *not* found in the present investigation. In Abidi's work [1], the device output characteristics indicate the presence of excessive avalanche current. The excess noise associated with this avalanche current may possibly explain his results. It is not clear whether a similar explanation exists for the results of ref.[2].

## 7.1.2

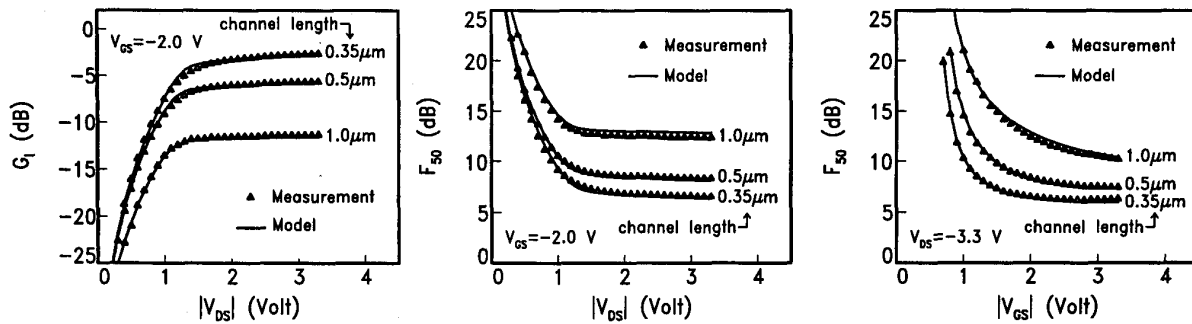


Figure 4: Insertion gain as a function of drain-source voltage (*left*), noise figure as a function of drain-source voltage (*middle*), and noise figure as a function of gate-source voltage (*right*), for p-channel MOSFETs in 0.35  $\mu\text{m}$  technology. Gate lengths are 1  $\mu\text{m}$ , 0.5  $\mu\text{m}$ , and 0.35  $\mu\text{m}$ , gate width is  $16 \times 10 \mu\text{m}$ . Symbols indicate measurements, lines indicate simulations.

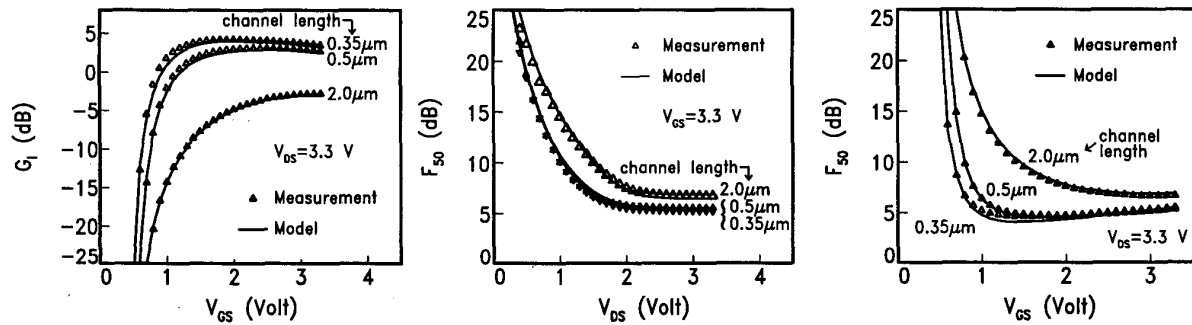


Figure 5: Insertion gain as a function of gate-source voltage (*left*), noise figure as a function of drain-source voltage (*middle*), and noise figure as a function of gate-source voltage (*right*), for n-channel MOSFETs in 0.35  $\mu\text{m}$  technology. Gate lengths are 2  $\mu\text{m}$ , 0.5  $\mu\text{m}$ , and 0.35  $\mu\text{m}$ , gate width is  $16 \times 10 \mu\text{m}$ . Symbols indicate measurements, lines indicate simulations.

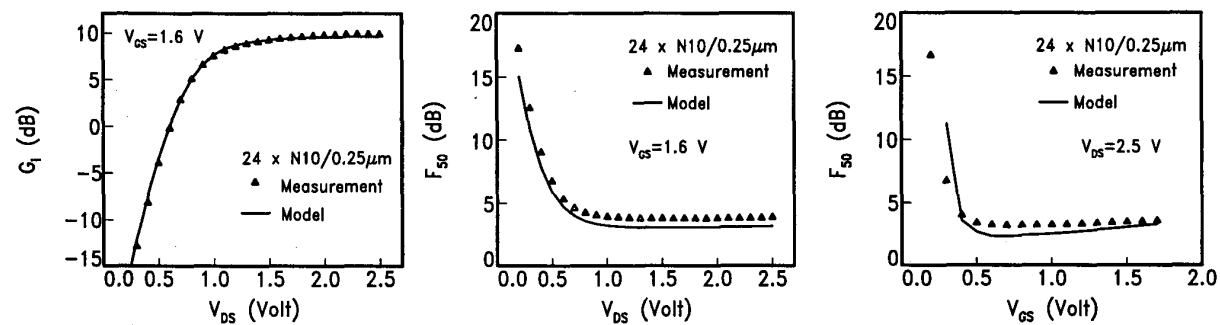


Figure 6: Insertion gain as a function of drain-source voltage (*left*), noise figure as a function of drain-source voltage (*middle*), and noise figure as a function of gate-source voltage (*right*), for an n-channel MOSFET in 0.25  $\mu\text{m}$  technology. The gate length is 0.25  $\mu\text{m}$ , the gate width is  $24 \times 10 \mu\text{m}$ . Symbols indicate measurements, lines indicate simulations.

### 7.1.3

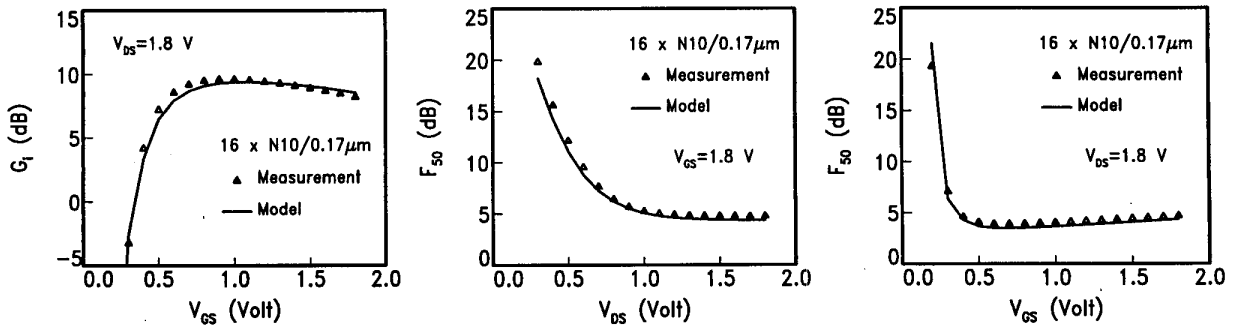


Figure 7: Insertion gain as a function of gate-source voltage (*left*), noise figure as a function of drain-source voltage (*middle*), and noise figure as a function of gate-source voltage (*right*), for an n-channel MOSFET in 0.18  $\mu\text{m}$  technology. The gate length is 0.17  $\mu\text{m}$ , the gate width is  $16 \times 10 \mu\text{m}$ . Symbols indicate measurements, lines indicate simulations.

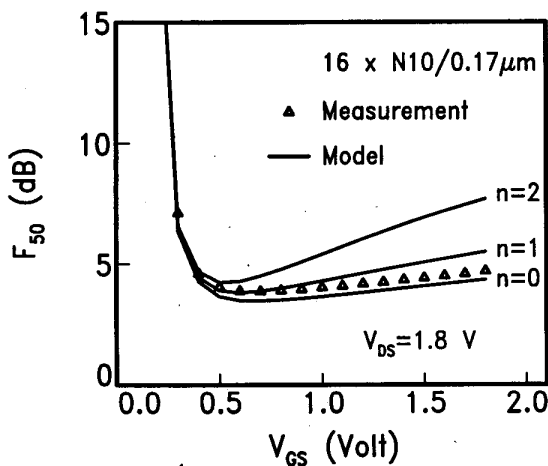


Figure 8: Symbols: measured noise figure as a function of gate-source voltage for an n-channel MOSFET in 0.18  $\mu\text{m}$  technology. Lines: simulated curves for  $n = 0$  (no electron heating), and for  $n = 1$  and  $n = 2$  (with electron heating).

### Conclusions

We have presented extensive measurements of drain current thermal noise for 3 different deep-submicron CMOS technologies with gate lengths ranging from 2  $\mu\text{m}$  down to 0.17  $\mu\text{m}$ . Using a surface-potential-based compact MOS model with improved descriptions of carrier mobility and velocity saturation, all our experimental results are described accurately *without* introducing additional parameters, or invoking carrier heating or new physical phenomena.

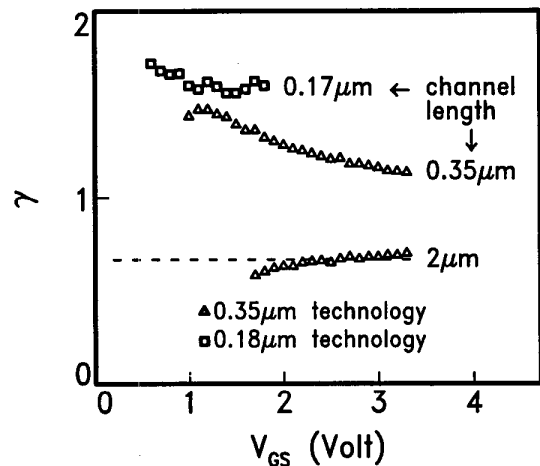


Figure 9: White-noise  $\gamma$ -factor [see Eq. (5)], extracted from the measurements on n-channel devices from 0.35  $\mu\text{m}$  and 0.18  $\mu\text{m}$  technologies ( $V_{\text{DS}} = V_{\text{supply}}$ ). The dashed line represents the theoretical long-channel result.

### References

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