

Compact modeling of drain and gate current noise for RF CMOS

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Abstract

A model for RF CMOS circuit design is presented that is capable of predicting drain and gate current noise without adjusting any parameters. Additionally, the presence of (i) noise associated to avalanche multiplication, and (ii) shot noise of the direct-tunneling gate current in leaky dielectrics is revealed.

Introduction

Accurate compact modeling of noise is a prerequisite for RF CMOS circuit design. Thermal noise of deep-submicron MOSFETs has received considerable attention lately, mainly triggered by reports of severe enhancements, up to a factor of 12, of the short-channel drain current noise (S_{Id}) with respect to long-channel theory [1,2]. Even more dramatic enhancements of the *gate* current noise (S_{Ig}), as large as a factor of 30, were reported for an $0.25\ \mu\text{m}$ n-channel MOSFET very recently [3]. Evidently, the reported noise enhancements [1,2,3] would seriously limit the viability of RF CMOS. In a previous study [4], we investigated S_{Id} at a relatively low frequency (248 MHz).

In this paper, we extend this work to RF frequencies and perform a detailed study of both S_{Id} , S_{Ig} , and their correlation. We will present a model for RF CMOS circuit design that is capable of *predicting* both S_{Id} and S_{Ig} without adjusting any parameters to fit the noise data. Additionally, we show experiments that reveal (i) the enhancement of S_{Id} by avalanche multiplication, and (ii) the enhancement of S_{Ig} by shot noise associated to the direct-tunneling gate current in leaky dielectrics.

Experiments

Noise measurements are performed on $0.18\ \mu\text{m}$ RF CMOS technology with an f_T of 70 GHz and an f_{max} as high as 150 GHz [5]. All devices have common source-bulk connection and consist of 64 fingers of $3\ \mu\text{m}$ width, based on the layout optimization of Fig. 1. RF noise measurements were performed using a HP8970 noise figure meter for a number of pre-characterized source impedances. Using open and short dummy structures, the MOSFET Y-parameters, measured using a HP8510C net-

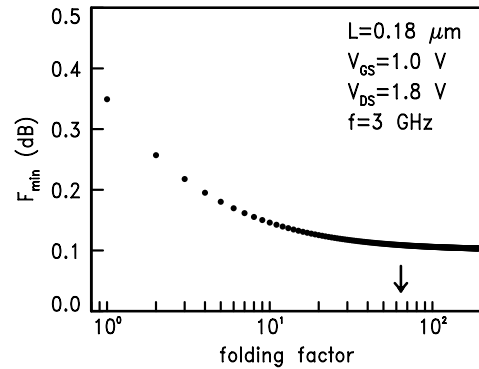


Fig. 1: Simulations of F_{min} versus folding factor for a $0.18\ \mu\text{m}$ gate length n-channel device with a total width of $192\ \mu\text{m}$. The arrow indicates the folding factor of 64 that we selected, corresponding to $3\ \mu\text{m}$ finger width.

work analyzer, and noise current sources are de-embedded to the DUT level along the lines of Ref. [6].

Model

The RF noise is modeled using the concept of channel segmentation, see Fig. 2. The ability of this model to describe the MOSFET RF behavior even in the non-quasi-static (NQS) regime has been demonstrated previously [7,8]. Here, every channel segment is modeled with MM11 [9], but the approach is applicable to any other compact model. Although we equip every segment with a drain current noise source only, calculated as in Ref. [4], the distributed gate capacitance in our model leads to induced gate noise naturally, as shown in Fig. 3. In contrast to expressions for S_{Ig} currently used in circuit design models [9,10], our model has the advantages that (i) it is not only valid in saturation, but in all MOSFET operating regimes (ii) it does not need correlated noise sources (iii) it automatically accounts for short-channel effects in S_{Ig} through the short-channel effects in S_{Id} [4], and (iv) it is valid even in the NQS regime. Further note that there are *no* adjustable parameters to fit the noise data: all model parameters follow from DC and CV measurements, except for the bulk resistance parameters, which follow from off-state Y-parameters.

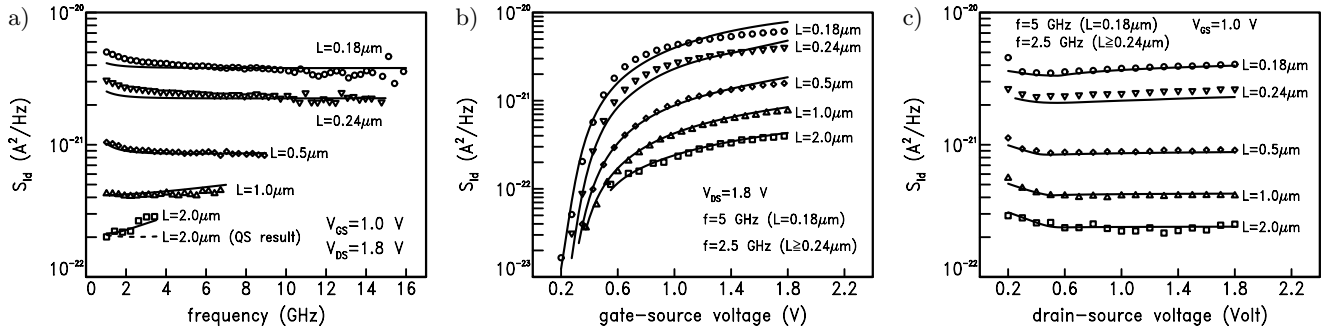


Fig. 4: Drain current noise versus frequency (a), V_{GS} (b), and V_{DS} (c), for a series of n-channel devices with different channel length. Markers represent the measurements, solid lines are model predictions. Dashed line in (a) represents the quasi-static (QS) result for the $L=2 \mu\text{m}$ device.

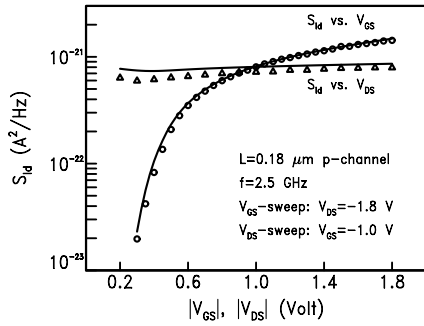


Fig. 5: Drain current noise versus V_{GS} , and V_{DS} , for a p-channel device with $0.18 \mu\text{m}$ channel length. Markers represent the measurements, solid lines are model predictions.

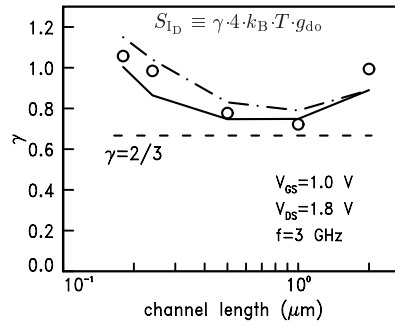


Fig. 6: White-noise gamma factor versus channel length. Markers: measured; solid line: compact model prediction; dash-dotted line: DD-MC simulation. ($g_{do} \equiv g_{ds}$ at $V_{DS} = 0 \text{ V}$.)

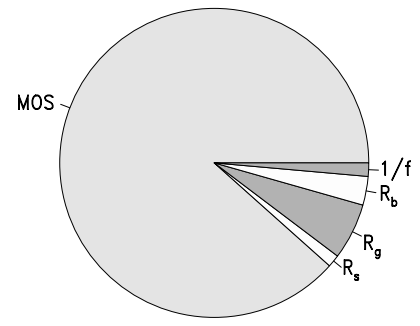


Fig. 7: Contributions to modeled drain current noise at $f=3 \text{ GHz}$ and a bias of $V_{GS}=1.0 \text{ V}$, $V_{DS}=1.8 \text{ V}$. The intrinsic MOSFET contribution dominates.

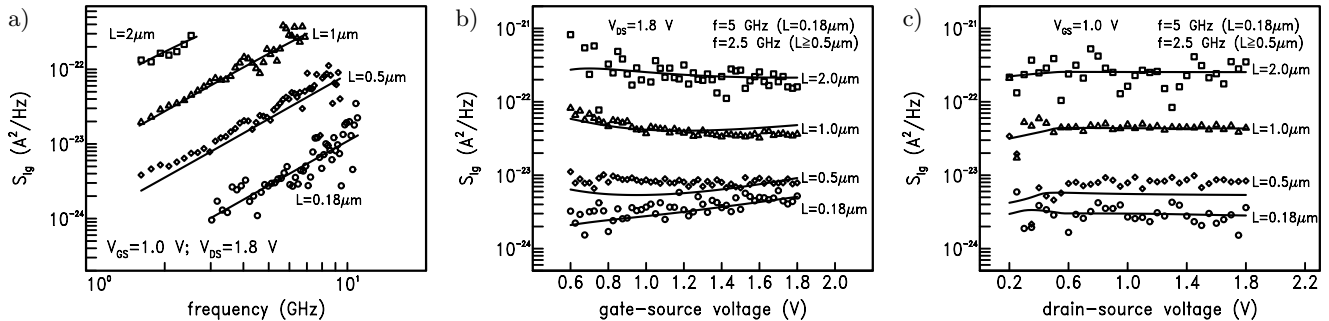


Fig. 8: Gate current noise versus frequency (a), V_{GS} (b), and V_{DS} (c), for a series of n-channel devices with different channel length (the $L=0.24 \mu\text{m}$ device is skipped here for clarity of the figure). Markers represent the measurements, solid lines are model predictions.

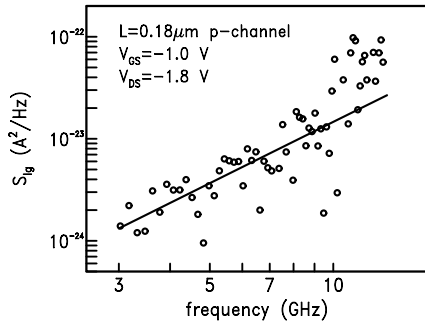


Fig. 9: Gate current noise versus frequency for a p-channel device with $0.18 \mu\text{m}$ channel length. Markers: measurements, solid line: model.

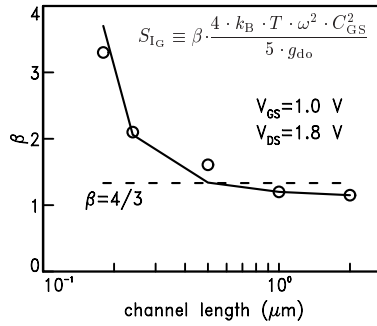


Fig. 10: The β factor, representing the amount of gate current noise, versus gate length.

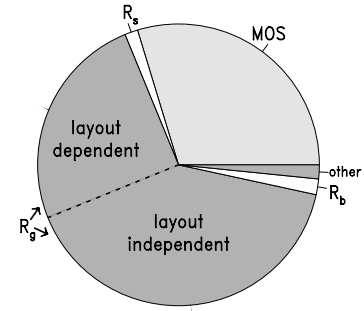


Fig. 11: Contributions to gate current noise at $V_{GS}=1.0 \text{ V}$, $V_{DS}=1.8 \text{ V}$, and $f=3 \text{ GHz}$. The noise from the gate resistance dominates.

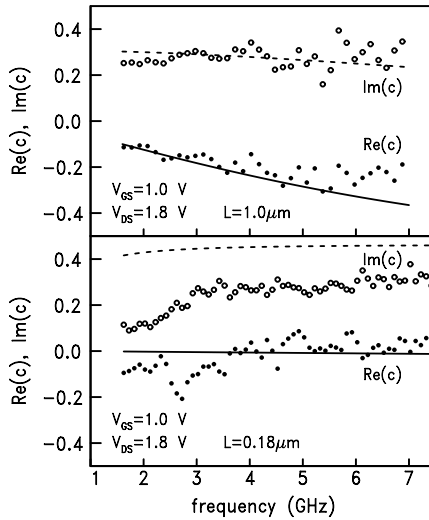


Fig. 12: Real and imaginary parts of the correlation coefficient for a $1 \mu\text{m}$ and an $0.18 \mu\text{m}$ long n-channel. Markers: measurements; solid lines: model prediction.

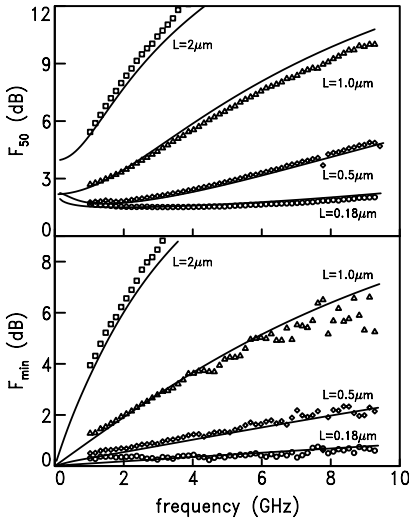


Fig. 13: Minimum and $50\text{-}\Omega$ noise figure versus frequency for a series of n-channel devices, biased at $V_{GS}=1 \text{ V}$ and $V_{DS}=1.8 \text{ V}$. Markers: measurements; solid lines: model prediction.

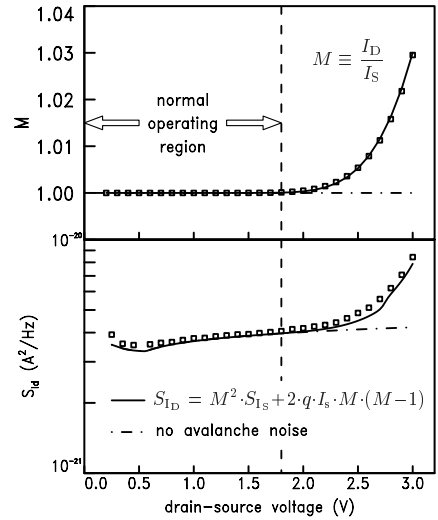


Fig. 14: Multiplication factor M and drain current noise versus V_{DS} (NMOS, $L=0.18 \mu\text{m}$, $V_{GS}=1 \text{ V}$, $f=5 \text{ GHz}$). Markers: measurements; solid and dash-dotted lines: model with and without avalanche.

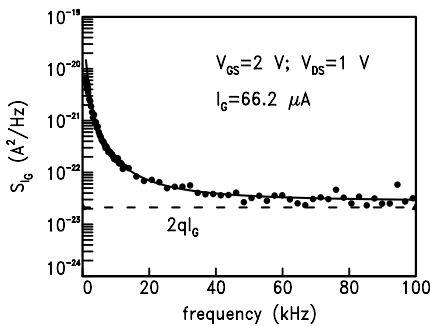


Fig. 15: Low-frequency gate current noise spectrum of a $10/10 \mu\text{m}$ MOSFET processed in 100-nm technology with a 1.5 nm EOT. Markers: measurements; solid line: fit with LF-noise and white contribution; dashed line: expected shot noise level.

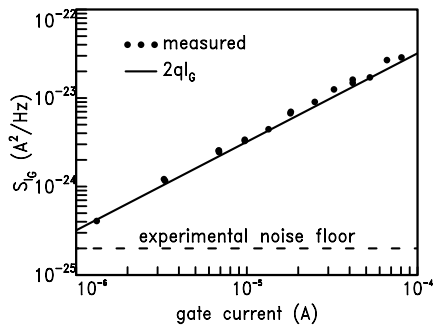


Fig. 16: Markers: white noise contribution to the gate current noise as a function of measured gate current. $V_{DS}=1 \text{ V}$ and V_{GS} is varied. Solid line: expected shot noise $2qI_G$.

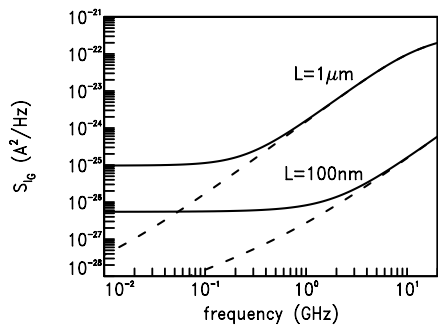


Fig. 17: Simulated gate current noise versus frequency for 100-nm technology, for $V_{DS}=V_{GS}=1 \text{ V}$. Dashed lines: without gate current shot noise. Solid lines: with gate current shot noise.