Anomalous geometry dependence of source/drain resistance in narrow-width MOSFETs

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Abstract— **The geometrical scaling of the intrinsic source/drain series resistance of MOSFETs is investigated using a large selection of transistor geometries in 0.5 μm CMOS technology. It is shown both experimentally and theoretically that for narrow-width MOSFETs with dogbone layouts the source/drain resistance is no longer inversely proportional to the channel width. A new scaling rule for the source/drain resistance and thus for the mobility reduction parameter θ_1 of MOS Model 9 leads to a considerably improved modelling accuracy in both the linear and saturation regime.**

Introduction

In state-of-the-art IC technologies the intrinsic source/drain series resistance (R_{SD}) of MOSFETs accounts for about 30 percent of the reduction of the current drive capability (saturation current, $V_{GS} = V_{DS} = V_{supply}$) [1]. For the linear current (i.e. the drain current for $V_{GS} = V_{supply}$ and $V_{DS} = 0.1$ V) the reduction due to R_{SD} can be as high as 50 percent. Consequently, accurate description of R_{SD} is of paramount importance for circuit simulation. Usually R_{SD} is assumed to be inversely proportional to the effective channel width W_E. Here we study the geometrical dependence of R_{SD} in MOSFETs and show that for very narrow channels this scaling rule no longer holds. A new scaling rule is derived and verified experimentally in a compact MOS model, MOS Model 9 (MM9) [2], resulting in considerable improvements of the modelling in both linear and saturation regime.

TABLE I. Transistor geometries used in this investigation. The dogbone devices are indicated by a ⋈. The number of contact holes is also indicated.

↓L W→	10	4	2	1.2	0.8	0.6
10	•	•	•	•	⋈	⋈
4	•		•		⋈	
2	•	•	•	•	⋈	⋈
1	•				⋈	
0.8	•					
0.7	•		•		⋈	
0.6	•		•		⋈	
0.5	•	•	•	•	⋈	⋈
# contacts	7	3	1	1	1	1

Test Structures

A large selection of 30 n- and p-channel MOSFET test structures with various geometries and realized in a 0.5 μm CMOS technology were used in the present investigation (see Table I). To allow for a detailed study of the geometrical dependence of the source/drain resistance the selection contained several series with fixed channel width and varying channel length and also several series with fixed channel length and varying channel width. One series with varying channel length was chosen at a channel width where 'dogboning' appears, i.e. the channel width is smaller than the contacted active area, as depicted in Figure 1. The minimum design rules determine the minimum effective width of this contacted active area (W_{EDOG}), whereas the width of the active area under the gate can be considerably smaller. The distance between the contact hole and the poly-Si of the gate is critical for the source/drain resistance. Consequently, minimum design rules have been used which is also the default in automated layout tools. Moreover the maximum number of contact holes was always used, see Table I.

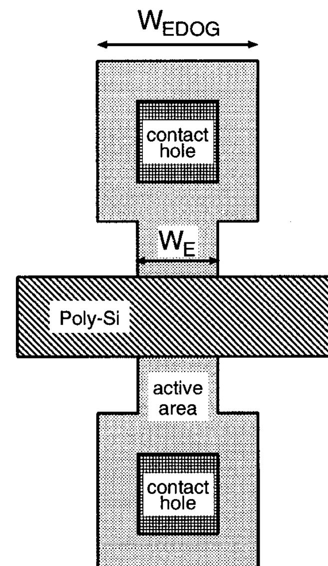

FIG. 1. Schematic layout of a transistor with dogboning.

Identification of the problem

Measurements allowing for MM9 parameter extraction have been performed and all the coefficients in the scaling rules of the parameters have been determined following the method presented in [2]. As shown in Table II, the resulting modelling accuracy is acceptable, which seems to indicate that all scaling rules are in perfect order. However, when a separate set of scaling rules for the compact model parameters is derived from the transistor geometries *without* dogboning, the modelling accuracy for these devices improves, while the accuracy for the structures *with* dogboning deteriorates considerably (see Table III). Moreover, the linear as well as the saturation current are underestimated systematically for all dogbone devices. This can be seen from the deviations between modelled and measured current, as shown in Figures 2 (linear current) and 3 (saturation current). As an example, the linear and saturation characteristics of the $0.8\mu m/0.5\mu m$ dogbone-device are shown in the inserts of Figures 2 and 3.

TABLE II. Relative deviation (modelled minus experimental value) of the linear and saturation currents, averaged over 30 geometries for the conventional scaling rule of MM9. (Absolute values were taken before averaging.)

	N-channels	P-channels
I_{lin}	3.3 %	2.3 %
I_{sat}	3.6 %	3.3 %

TABLE III. Relative deviations (averaged over all non-dogbone resp. dogbone geometries) between simulated and experimental linear currents using scaling rules for the compact model parameters derived from non-dogboning structures only (n-channels). (Absolute values were taken before averaging.)

	Non-dogbone	Dogbone
I_{lin}	1.2 %	13.7 %
I_{sat}	2.8 %	15.6 %

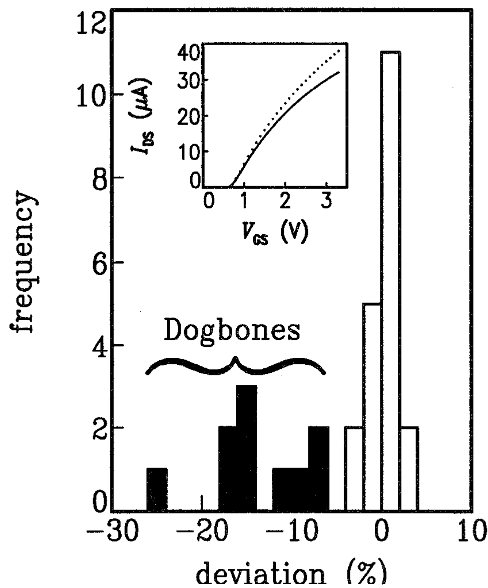

FIG. 2. Distribution of deviations between modelled and measured linear current of all 30 n-channel geometries. Scaling rules derived from the 20 non-dogbone structures (open bars) have been used. It is seen that the linear current of the dogbone geometries (filled bars) is underestimated systematically by the model.
Insert: Linear transfer graph (V_{DS} = 0.1 V) of the n-channel $0.8\mu m/0.5\mu m$ dogbone-device. The dots represent the measurements, the solid line represents the model derived from non-dogbone structures only.

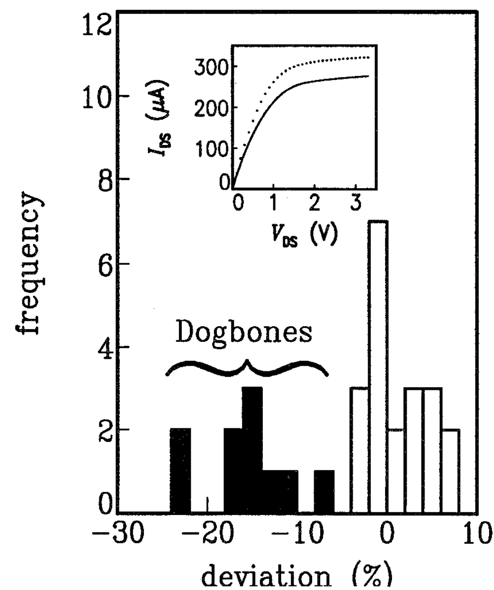

FIG. 3. Same as Figure 2, but now for the saturation current of the n-channels.
Insert: Saturation characteristic (V_{GS} = 3.3 V) of the n-channel $0.8\mu m/0.5\mu m$ dogbone-device. The dots represent the measurements, the solid line represents the model derived from non-dogbone structures only.

Two possibilities to explain the deviations that we find between model and measurements for dogbone devices (Figures 2 and 3) are:
1. The gain factor β may be underestimated for dogbone devices [3]. The sharp edges, as depicted in Figure 1, may be rounded off in practice, causing the MOSFET to be wider at the entrances. This could lead to a larger W_{E}, and thus a larger current than expected for dogbone devices.
2. The source/drain resistance R_{SD}, and thus θ_1 (see Eq.(3)), may be overestimated for dogbone devices, because the active areas around the contacts are wider than the actual device area. Note that the rounding-off of the sharp edges in the actually processed dogbone device, as we just discussed above, will reduce R_{SD} even more.

In order to distinguish between these two possibilities, we performed two further tests. First, we extracted for all 30 devices the so-called *miniset* parameters (threshold voltage V_{TO}, gain factor β, mobility reduction parameters θ_1, θ_2, θ_3, etc., see [2]), which describe the individual transistors very accurately. Now we calculated the linear current for all devices using these miniset parameters, except for the first mobility reduction parameter θ_1. For this parameter we fitted its MM9 scaling rule,

$$\theta_1 = \theta_{10} + \frac{S_{\mathrm{W};\theta_1}}{W_{\mathrm{E}}} + \frac{S_{\mathrm{L};\theta_1}}{L_{\mathrm{E}}} \tag{1}$$

to the θ_1 miniset-values of the 20 geometries *without* dogboning. Here, W_{E} and L_{E} are the effective channel width and length, respectively. $S_{\mathrm{W};\theta_1}$ and $S_{\mathrm{L};\theta_1}$ are the θ_1 width and length scaling coefficients (Note that for convenient notation, we have chosen $L_{\mathrm{ER}} = W_{\mathrm{ER}} = \infty$ for the length and width of the reference transistor). With θ_1, calculated from Eq. (1), the modelled currents of the non-dogbone geometries are of course in excellent agreement with the measurements. For the structures *with* dogboning however the latter calculation predicts consistently too low values for the linear current. This is seen from the upper frame of Figure 4, which shows that the distribution of dogbone devices is shifted considerably to the left with respect to the distribution of non-dogbone devices. This indicates that the scaling rule Eq. (1) may *not* be extrapolated from the non-dogbone into the dogbone geometry range.

A similar test was applied to the current gain factor β. Now for all parameters, except β, the miniset values were used, while for β we fitted its MM9 scaling rule to the β miniset-values of the 20 geometries *without* dogboning. The β scaling rule in MM9 reads:

$$\begin{aligned} \beta &= \beta_{\Box} \cdot \frac{W_{\mathrm{E}}}{L_{\mathrm{E}}} \\ L_{\mathrm{E}} &= L - \Delta L \\ W_{\mathrm{E}} &= W - \Delta W \ , \end{aligned} \tag{2}$$

where L and W are the drawn channel length and width, respectively, and ΔL and ΔW are constants that are independent of geometry and bias conditions. Now, using the β scaling rule as described above, the calculated linear currents are close to the measured ones over the entire geometry range. This is confirmed by the lower frame of Figure 4, where we see that the distributions of dogbone and non-dogbone devices nicely coincide. This shows that the scaling rule of β is correct, in contrast to what was observed in [3]. Moreover the latter test confirms that the determination of effective channel length and width has been performed accurately.

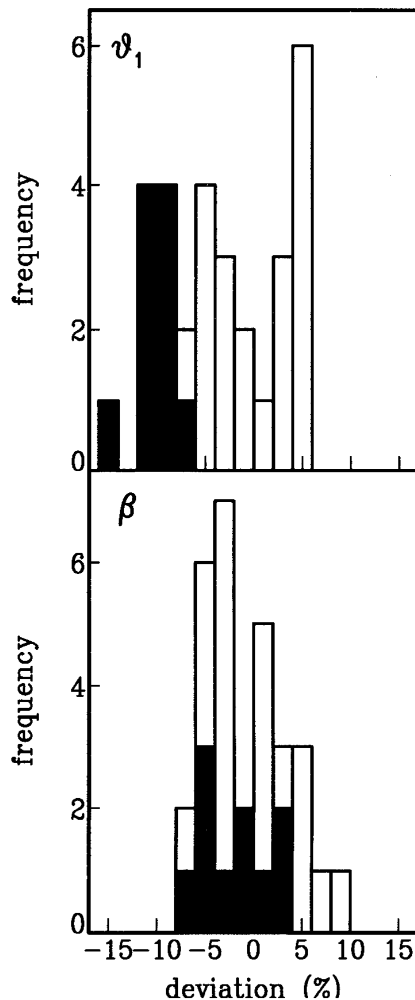

FIG. 4. Distributions of deviations between modelled and measured linear current. Filled bars represent the dogbone devices, and open bars the other devices.
Upper frame: Result of the the θ_1 scaling rule test, as described in the text.
Lower frame: Result of corresponding β scaling rule test, see text.

Analysis of the geometry dependence of the source/drain resistance

In MM9 the mobility reduction parameter θ_1 depends on both gain factor β and source/drain resistance R_{SD}

$$\theta_1 = \theta_{10} + \beta \cdot R_{\mathrm{SD}} \tag{3}$$

where θ_{10} accounts for the intrinsic mobility reduction due to the gate-induced field. For a fixed channel width R_{SD} can be determined from the slope of a θ_1 vs β plot for a series of channel lengths. Some examples are shown in Figure 5.

For both n- and p-channels, R_{SD} was determined for several channel widths. In order to make deviations from the $R_{\mathrm{SD}} \propto 1/W_{\mathrm{E}}$ relationship clearly visible, we plotted the product $R_{\mathrm{SD}} \times W_{\mathrm{E}}$ as a function of drawn channel width W, see Figure 6. From this Figure, it is observed that for small channel widths, R_{SD} is no longer inversely proportional to the effective channel width, and is severely overestimated (up to 25 %) when conventional width scaling is applied.

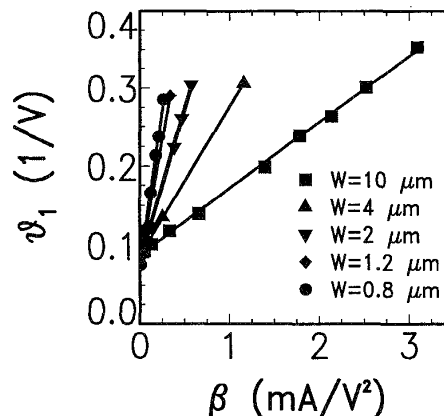

FIG. 5. Mobility reduction parameter θ_1 plotted as a function of current gain factor β for n-channel transistors with varying channel length and fixed channel width. Solid lines are fits of Eq. (1) to the data, yielding θ_{10} and R_{SD}.

New scaling rule for the source/drain resistance and mobility reduction parameter

Using a three-dimensional distributed resistor network accounting for the diffusion region, silicide layer, their contact resistance, and the number of contact holes, R_{SD} has been calculated as a function of channel width. The details of the calculation are given in Figures 7 and 8. The results of these calculations, shown in Figure 6 (solid line), agree very well with the data. Above $W = 1.2$ μm, the calculation shows that the $R_{\mathrm{SD}} \cdot W_{\mathrm{E}}$ product is almost constant, apart from small kinks due to the discrete number of contact holes. Thus it is seen that the conventional scaling rule works very well for $W > 1.2$ μm. However, $R_{\mathrm{SD}} \cdot W_{\mathrm{E}}$ displays a sharp drop below the width where dogboning sets in, $W = 1.2$ μm. Based on these observations we have formulated the following improvement of the scaling rule for the MM9 mobility reduction parameter θ_1 (and thus implicitly for the source/drain resistance):

For $W_{\mathrm{E}} < W_{\mathrm{EDOG}}$:

$$\theta_1 = \theta_{10} + \frac{S_{\mathrm{W};\theta_1}}{W_{\mathrm{E}}} + \frac{S_{\mathrm{L};\theta_1}}{L_{\mathrm{E}}} + S_{\mathrm{L};\theta_1} \cdot \frac{f_{\theta_1}}{L_{\mathrm{E}}} \cdot \left(\frac{W_{\mathrm{E}}}{W_{\mathrm{EDOG}}} - 1 \right) \tag{4}$$

Here, f_{θ_1} is a unitless parameter of the order of 1, and W_{EDOG} is the effective minimum width of the contacted active area. Eq. (4) is only valid for $W_{\mathrm{E}} < W_{\mathrm{EDOG}}$. For $W_{\mathrm{E}} \geq W_{\mathrm{EDOG}}$ no dogboning appears and the last term in Eq. (4) must be dropped, yielding the θ_1 scaling rule of Eq. (1), used until now in MM9. An example of the resulting description is given in Figure 6 (dotted line) and compared to the old description (dashed line).

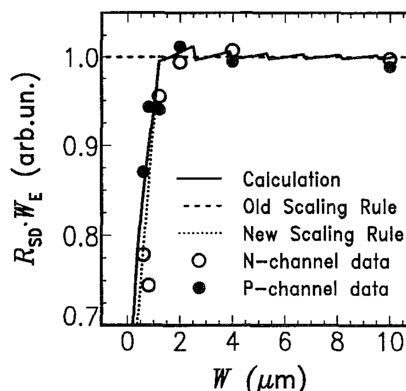

FIG. 6. Source/drain resistance multiplied by the effective channel width as a function of channel width. The n-channel and p-channel data were divided by 833 and 2200 Ωμm, respectively. The solid line represents the theoretical calculation. Dashed and dotted lines represent the old and new scaling rules, respectively.

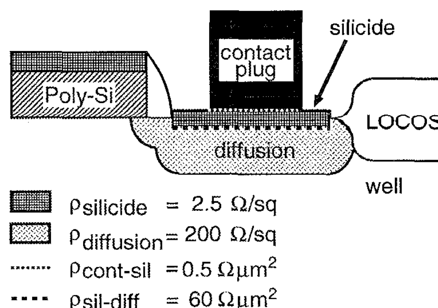

FIG. 7. Cross-section of a source/drain area (diffusion) with silicide layer, and resistivities used to calculate the solid line in Figure 6.

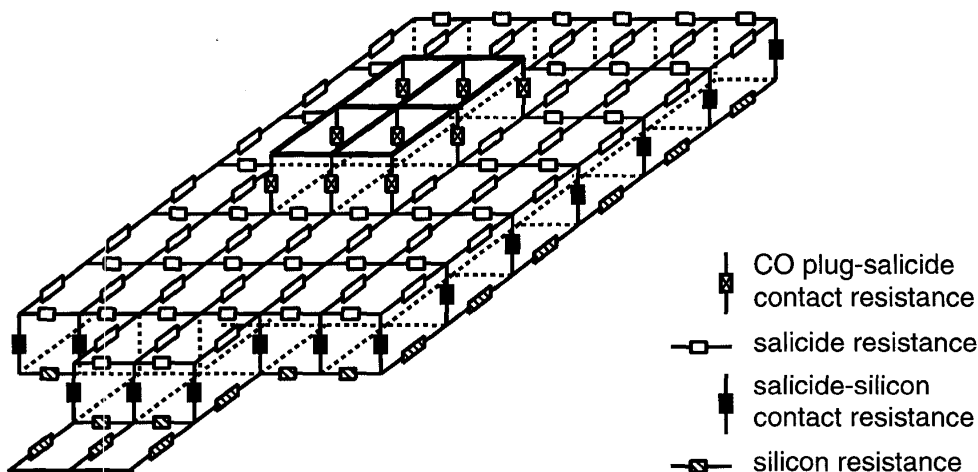

FIG. 8. Simplified schematic of a 3-dimensional resistor network utilised in the calculation of the resistance of a silicided source/drain area. The following simplifications have been made for clarity of the figure: the silicide resistor network actually continues under the contact; every node of the silicide resistor network is connected to a contact resistor, which is in turn connected to the the silicon resistor network; the latter also continues under the silicide resistors. Finally we note that the networks used in the actual calculations, have much more resistors (one per 50 nm) than sketched here.

Improved modelling accuracy

Some results for the 0.5 μm technology are shown in Figure 9, where the modelling accuracy of the old and new scaling rules are compared for the linear current of the n-channels. The improvement is evident from the narrowing of the distributions. The modelling of the saturation current of the n-channels is also improved as shown in Figure 10. The fact that the improvement is less pronounced than for the linear current is connected with the smaller influence of R_{SD} on the saturation current (see Introduction). Also for the p-channels both linear and saturation currents are modelled more accurately by the new scaling rule, see Figures 11 and 12.

This is confirmed by the relative deviations between model and measurement, averaged over all 30 devices, which are listed in Table IV for linear and saturation current, and for both n- and p-channels. It is seen that the modelling inaccuracy of the linear current is reduced by a factor of ~2. For the saturation current this reduction is typically a factor of ~1.5.

The new model, which is already implemented in MOS Model 9, has also been used for the modelling of 0.35 μm technology. In this case a selection of 11 transistors was measured, 3 of which were dogbones. Again the improvement caused by the new scaling rule is substantial, as can be seen from Table V.

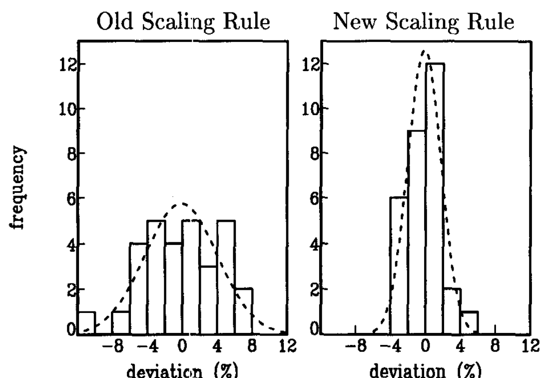

FIG. 9. Histograms of deviations between modelled and measured linear current of all 30 n-channel geometries for the old and new scaling rules.

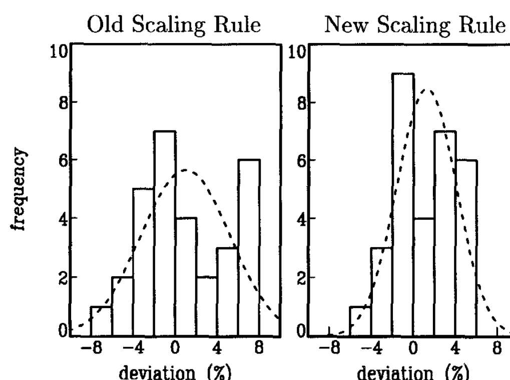

FIG. 10. Histograms of deviations between modelled and measured saturation current of all 30 n-channel geometries for the old and new scaling rules.

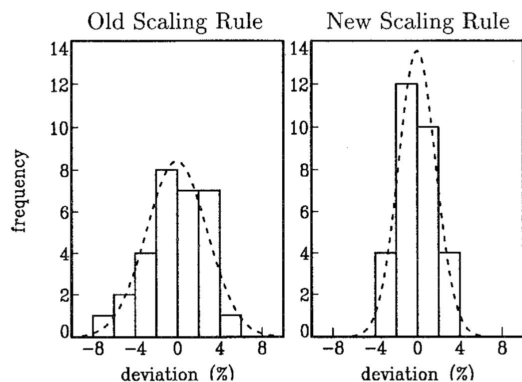

FIG. 11. Histograms of deviations between modelled and measured linear current of all 30 p-channel geometries for the old and new scaling rules.

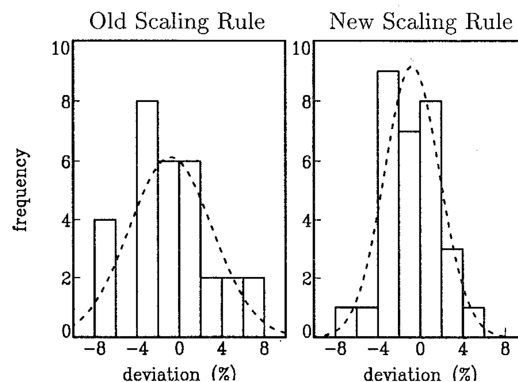

FIG. 12. Histograms of deviations between modelled and measured saturation current of all 30 p-channel geometries for the old and new scaling rules.

TABLE IV. Relative deviations between modelled and measured currents, averaged over all 30 geometries, for 0.50 μm technology. (Absolute values were taken before averaging.)

	N-channels		P-channels	
	Old	New	Old	New
$I_{\rm lin}$	3.3 %	1.5 %	2.3 %	1.4 %
$I_{\rm sat}$	3.6 %	2.5 %	3.3 %	2.2 %

TABLE V. Same as Table IV for 0.35 μm technology.

	N-channels		P-channels	
	Old	New	Old	New
$I_{\rm lin}$	3.2 %	1.9 %	2.2 %	1.7 %
$I_{\rm sat}$	4.5 %	2.7 %	3.4 %	3.1 %

Conclusions

Using a large selection of transistor geometries designed in 0.5 μm CMOS technology we have investigated the geometrical dependence of the source/drain resistance of MOSFETs. It has been shown that for narrow-width MOSFETs with dogbone layouts, the source/drain resistance is no longer inversely proportional to the channel width. The experimentally observed width dependence has been confirmed by three-dimensional distributed network calculations. A new scaling rule for the source/drain resistance and thus for the MM9 mobility reduction parameter θ_1 has been derived. The accuracy of the MM9 modelling of both the linear and saturation current is improved considerably for 0.5 μm as well as for 0.35 μm technology.

Acknowledgments

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