The high-frequency analogue performance of MOSFETs

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Abstract

The high-frequency (HF) behaviour of MOSFETs from different CMOS processes has been characterized. Small-signal Y-parameters and derived quantities such as current, voltage, and power gain have been measured and good agreement with calculations using the Philips compact model, MOS MODEL 9, has been obtained. Using HF measurements on MOSFETs and Bipolar devices, it is shown that the figures of merit, related to the gains mentioned above, are not sufficient to evaluate the HF capabilities of CMOS, BiCMOS and Bipolar technologies.

Introduction

Recent CMOS technologies with gate lengths of 0.1 μm have resulted in unity-current-gain frequencies (f_T) as high as 118 GHz [1] and ring-oscillator gate delays as low as 11.8 psec [2]. In the literature both quantities are used to benchmark the high-frequency (HF) performance of CMOS technologies relative to Si bipolar technologies, for which f_T's of 74 GHz and ECL gate delays of 15 psec have been reported [3]. The use of specific test circuits to evaluate the HF performance of different technologies emphasizes that specification of the maximum f_T is insufficient. Moreover, CMOS ring-oscillators and ECL are not quite comparable: they represent each only a limited application area of CMOS and bipolar technologies. Effective evaluation of different technologies should consist of *i)* HF characterization; *ii)* compact model verification; *iii)* (using this compact model) simulation of the performance of any analogue circuit, which may be processed in the technologies under investigation. Here we present a detailed HF characterization of CMOS devices from different process generations and the verification of the Philips compact MOS model MOS MODEL 9 [4] for these processes. It will be demonstrated that a fair comparison between the HF performance of Bipolar and CMOS processes can not be performed using figures of merit on device level.

Experimental set-up and test devices

Small-signal scattering (S) parameters in two-port configuration have been measured with an HP8510 Network Analyzer. To match the ground-signal-ground probes of Cascade Microtech, special test structures have been designed with the MOSFETs in common source-bulk configuration. Measured S-parameters have been converted to admittance (Y) parameters and dummy structures have been used to correct for interconnect parasitics. The individual terminal capacitances have been measured at low frequencies with an HP4284A LCR-meter.

Small-signal Y-parameters

In fig. 1 measurements of the real and imaginary part of the drain-gate admittance are plotted. In order to get insight in the quantities and parasitic elements determining the Y-parameters, approximate expressions for these parameters have been derived using the equivalent circuit of fig. 2. For the actual simulations we used the Philips compact model MOS MODEL 9 [4] with parameters obtained from DC current measurements. Overlap and depletion capacitances were determined from low-frequency capacitance measurements. The frequency dependence of the Y-parameters is strongly influenced by parasitic elements. To illustrate this, the forward admittance (Y_{dg}), is plotted in fig. 1. Using the equivalent circuit of fig. 2 and neglecting the influence of the bulk resistance, Y_{dg} can be expressed as:

$$Y_{dg} = \frac{g_m - \omega^2 R_g C_{dg} C_{in} - j\,\omega(g_m R_g C_{in} + C_{dg})}{1 + \omega^2 R_g^2 C_{in}^2}$$

where $C_{in} = C_{gg} + C_{gdo} + C_{gso}$. The bulk resistance, R_b, has a non-negligible influence only on Y_{dd}. For a one-side contacted gate, the gate resistance, R_g, can be derived from transmission-line theory, yielding: $R_g \simeq W R_{\Box,\,poly} / 3L$. By introducing this "effective" gate resistance, a good agreement between measurements and simulations for Y_{gg} and Y_{dg} (see fig. 1,3b) is demonstrated.

Current, voltage and power gain

The current gain can be expressed in Y-parameters, leading to an approximate expression for f_T, $f_T \simeq g_m/(2\pi C_{in})$. The DC transconductance, g_m, and input capacitance, C_{in}, are plotted in fig. 3, while f_T is plotted in fig. 4. For short-channel devices f_T is in the saturation region almost independent of the gate bias (see fig. 4). This can be explained from the mobility degradation (see fig. 3a), caused by the lateral and transversal electrical field. Expressed in Y-parameters, the voltage gain, A_v, reads

$$A_v = -\frac{Y_{dg}}{Y_{dd} + Y_L}$$

where Y_L is the load admittance. In fig. 5 two load

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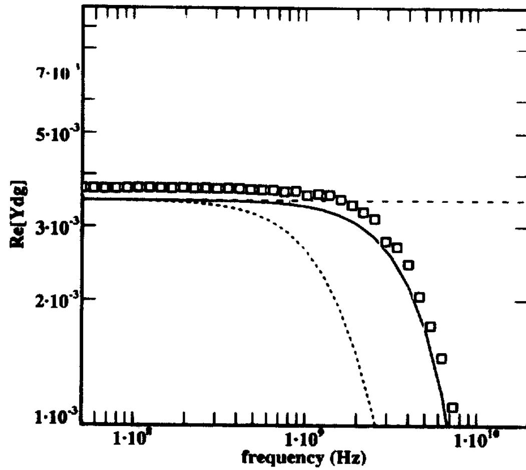

Figure 1a: Real part of Y_{dg} vs. frequency for a 40/1 n-channel at $V_{gs} = V_{ds} = 4V$. Symbols represent measurements, lines represent simulations with a gate resistance of $R_g = 0$ (dashed line); $R_g = (W R_{\square, poly})/(3L)$ (solid line); and $R_g = (W R_{\square, poly})/L$ (dotted line).

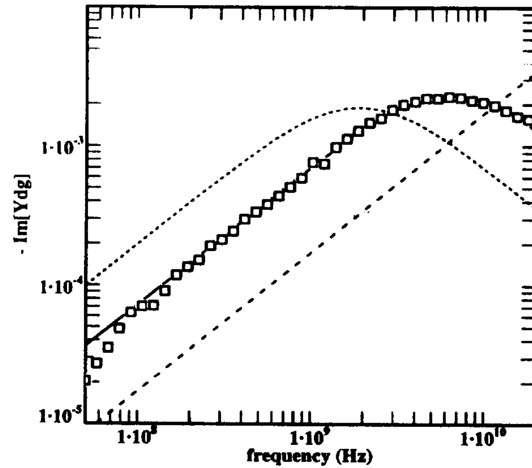

Figure 1b: Imaginary part of Y_{dg} vs. frequency for a 40/1 n-channel at $V_{gs} = V_{ds} = 4V$. Symbols represent measurements, lines represent simulations with a gate resistance of $R_g = 0$ (dashed line); $R_g = (W R_{\square, poly})/(3L)$ (solid line); and $R_g = (W R_{\square, poly})/L$ (dotted line).

conditions are evaluated for a 40/1 n-channel: *i)* an open output ($Y_L = 0$), which yields the maximum achievable voltage gain; *ii)* loaded with an identical device, which in its turn is unloaded ($Y_L = 1/Z_{gg}$). The maximum available power gain, G_{max}, is shown in fig. 6 (i.e. the transducer power gain under simultaneous conjugate-match conditions). For G_{max} and for the unity-power-gain frequency f_{max} the bulk resistance is of paramount importance. This is demonstrated in fig. 6 where G_{max} for a 40/2 n-channel from the 1 μm process and a 20/0.5 n-channel from the 0.5 μm process is plotted. The poly gates from the 0.5 μm process are silicidised which results in a much lower gate resistance. However, in both processes the bulk resistance still limits f_{max}. The value for the bulk resistance, which is independent of channel length, has been obtained from the frequency dependence of Y_{dd}.

Comparison of different technologies

Devices from a number of processes have been analyzed: *i)* two standard CMOS processes with minimum gate lengths of 0.5 μm (with gate oxide thickness, t_{ox}=12.5 nm) and 1 μm (t_{ox}=20 nm) *ii)* a standard 1 μm BiCMOS process; and *iii)* a HF double-polysilicon bipolar process [5]. f_T is independent of channel width and emitter length. In fig. 7 the maximum f_T, $f_{T,max}$, is shown as a function of gate length and emitter width. From this figure it can be seen that the values of $f_{T,max}$ are almost the same for the two CMOS processes. Furthermore the 0.5 μm CMOS process yields an $f_{T,max}$, which is only half the value obtained in the HF bipolar process. However, as already mentioned in the introduction, the HF performance of a process for a wide range of applications can not be judged from $f_{T,max}$. This is once more illustrated in fig. 8, where f_T for a 0.5 μm MOS device and for a 1 μm device from the HF bipolar process are shown as function of the drain current per unit channel width and collector current per unit emitter length, respectively. At low current levels, the MOSFET has a higher f_T than the npn from the bipolar HF process in which an ECL gate delay of 18 psec has been obtained [5]. In fig. 8 f_T curves simulated with the Philips compact models show good agreement with the experimental results [4, 6]. In fig. 9 f_{max} is plotted versus channel length for a width of 40 μm for n-channels from the two CMOS processes. Note that (fig. 9) the shortest channel length devices of the silicidised process have a significant larger f_{max} value in spite of the smaller gate-oxide thickness (see e.g. equation 1.10.5 of [7]). However, for the longer channel length devices of the silicidised process, the source series resistance limits f_{max} (see e.g. equation 4.15 of [8]). The channel width dependence of f_{max} hampers a direct comparison with f_{max} values from bipolar transistors (as shown in fig. 8 for $f_{T,max}$). Compact modeling is the ideal tool to make such a comparison.

Conclusions

The HF performance of MOSFETs from different process generations has been characterized in detail. Excellent agreement between measurements and simulations

using MOS MODEL 9 has been obtained for Y-parameters, the current, voltage and power gain and the corresponding unity-gain frequencies. This demonstrates that compact models for circuit simulation are an excellent tool to evaluate the HF analogue performance of a wide range of circuits in CMOS, BiCMOS and Bipolar technologies.

References

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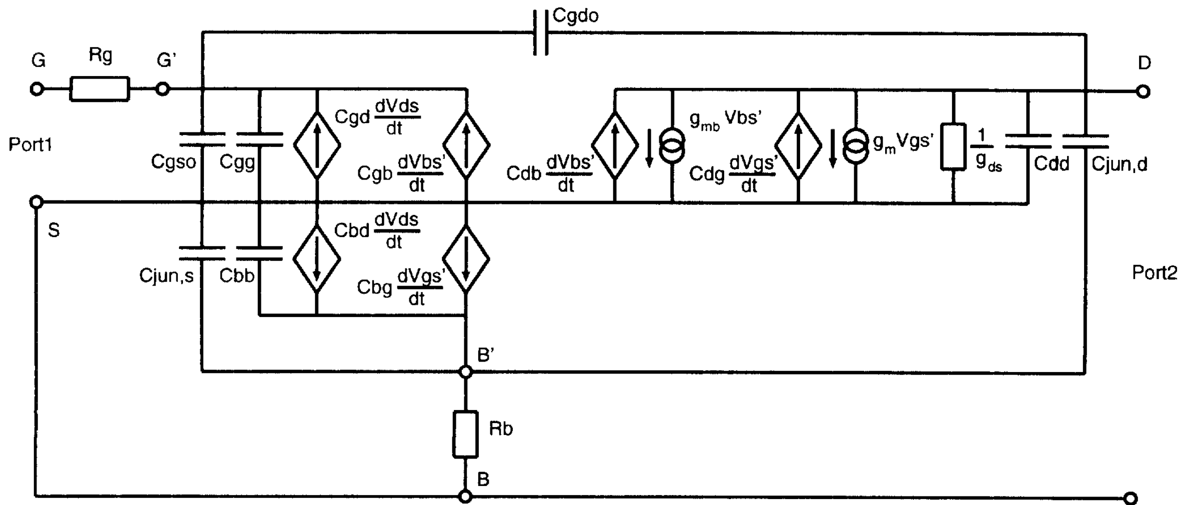

Figure 2: Equivalent circuit of a MOSFET in two-port common source-bulk configuration. The overlap capacitances are indicated with C_{gso} and C_{gdo}; the junction capacitances are indicated with $C_{jun,s}$ and $C_{jun,d}$. The gate resistance is indicated with R_g and the bulk resistance is indicated with R_b. The source and drain series resistances are incorporated in MOS MODEL 9.

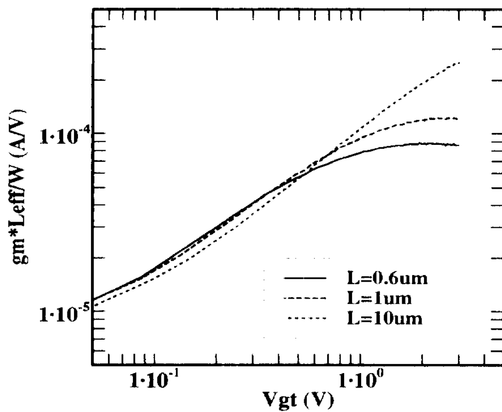

Figure 3a: Normalized transconductance g_m vs. V_{gt} measured in the saturation region for different channel lenghts of 0.6 μm, 1.0 μm, and 10 μm.

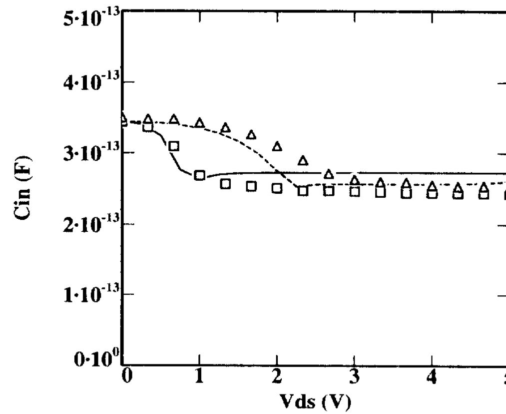

Figure 3b: measured (symbols) and simulated (lines) input capacitance as a function of V_{ds} for NMOS 40/5 at V_{gs} =2V (squares) and 4V (triangles).

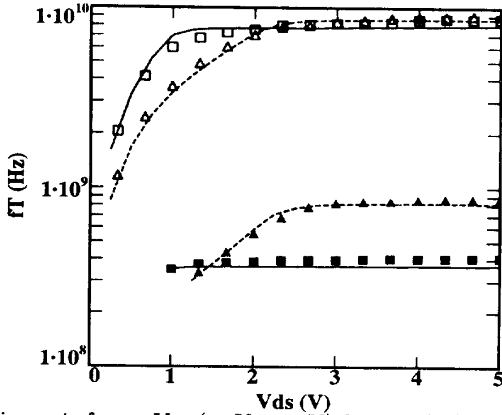

Figure 4: f_T vs. V_{ds} (at V_{gs} =5V) for a 40/5 (filled symbols) and 40/1 (open symbols) n-channel at V_{gs} = 2V (squares) and 4V (triangles). Symbols represent measurements, lines represent simulation results.

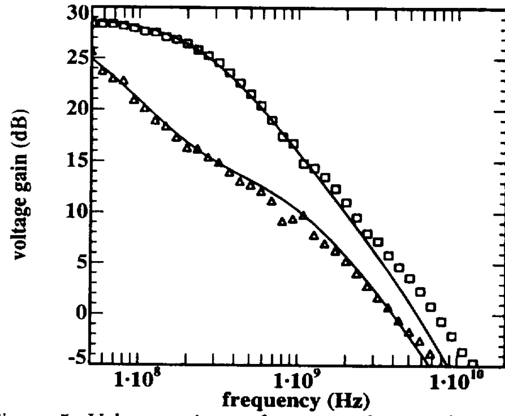

Figure 5: Voltage gain vs. frequency for a 40/1 n-channel at V_{gs} = 2V, V_{ds}=5V. Symbols are measurements: $Y_L = 0$ (squares), $Y_L = 1/Z_{gg}$ (triangles) ; lines are simulations.

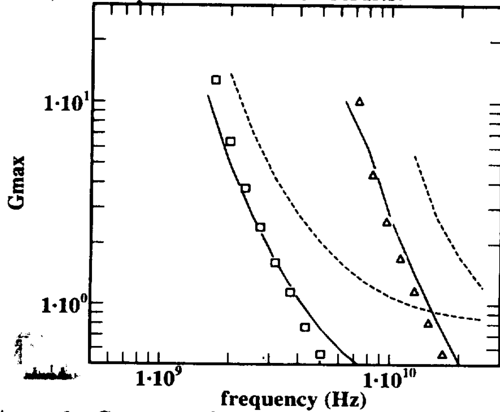

Figure 6: G_{max} vs. frequency for a 40/2 n-channel at V_{gs} = 2V, V_{ds}=5V (squares) and a 20/0.5 n-channel at $V_{gs} = V_{ds} = 3.5V$ (triangles); simulations are with (fully drawn line) and without (dashed line) bulk resistance.

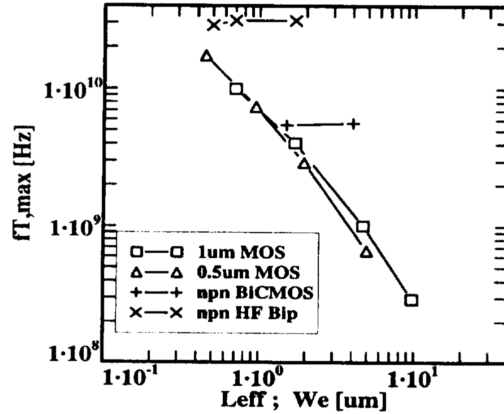

Fig. 7: $f_{T,max}$ vs. the effective channel length (MOS: n-channels) or emitter width (bipolar).

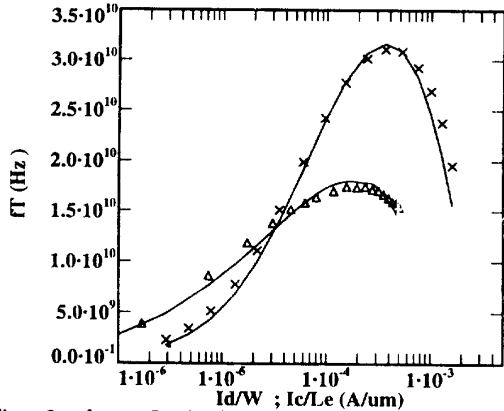

Fig. 8: f_T vs I_C (I_D) per unit length(width); 0.5 μm NMOS (triangles), 1 μm NPN from HF DP process (crosses); MOS MODEL 9, MEXTRAM simulations (lines).

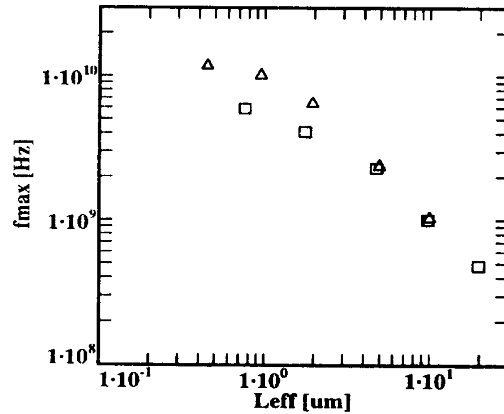

Figure 9: measured values of f_{max} for n-channels vs. L_{eff}: squares represent the 1 μm process; triangles represent the 0.5 μm process.

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