RF Noise Modelling of 0.25 μm CMOS and Low Power LNAs

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Abstract

A prototype 0.5 μm CMOS LNA with a noise figure of 2.2 dB and a gain of 16.9 dB at 900 MHz at a power consumption of 1.8 mW is reported. This result, and the noise figures obtained on 0.25 μm CMOS, are reproduced by simulations, confirming that RF noise modeling can be accurately performed using our public domain MOS Model 9. Simulations are presented for similar LNAs realized in standard CMOS processes with gate dimensions down to 0.13 μm. Provided high Q matching circuitry is used, for the latter gate length a noise figure of only 1.1 dB and 27 dB gain at 1800 MHz, at a minimal power consumption of only 0.2 mW, is predicted.

Introduction

With the scaling towards minimum gate lengths of 0.25 μm and below the use of CMOS has become a serious option in several wireless RF applications previously considered to be the exclusive domain of bipolar and III-V technologies [1]. Top of the line CMOS with 0.12 μm gate length has a cut-off frequency beyond 150 GHz and a minimum noise figure of 0.51 dB at 2 GHz [2]. To enable the cost effective CMOS option to circuit designers adequate RF modelling tools are a prerequisite. Having verified the DC and AC modelling accuracy of our public domain MOS Model 9 (MM9) [3] in earlier work [4,5], this paper focusses on noise figure modelling for the design of RF Low Power Low Noise Amplifiers (LNAs). First an experimental verification of the noise level predicted by MM9 is presented, which demonstrates for the first time, that the RF noise behaviour for CMOS process generations down to 0.25 μm is modelled well by a compact model such as MM9. The value of this noise modelling is then confirmed by simulation and experimental verification of a two-stage (cascode) LNA fabricated in an industrial process with minimum dimensions of 0.5 μm. Finally, by simulating CMOS LNAs fabricated in processes with gate lengths down to 0.13 μm, the high potential of standard CMOS is revealed, reflected by the feasibility of 27 dB gain and 1.1 dB noise figure at 1800 MHz at a power consumption of only 0.2 mW.

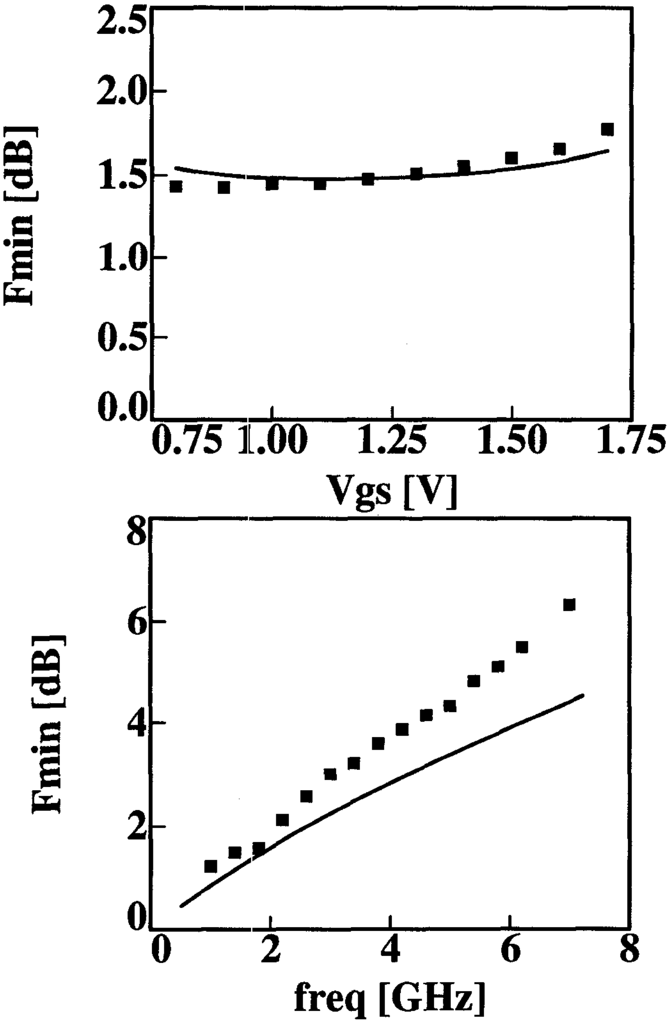

Figure 1: *Measured (symbols) and simulated noise figure versus gate voltage at a frequency of 1.8 GHz and versus frequency at* $V_{gs} = 1.1V$*, of a 0.25 um nMOS with 4.5 nm gate oxide in common source configuration at* $V_{ds} = 1.2V$.

Experimental Results

The noise figure measurements were performed on-wafer using a Maury Microwave automated tuner system and a noise figure test-set, with the input tuned for minimum

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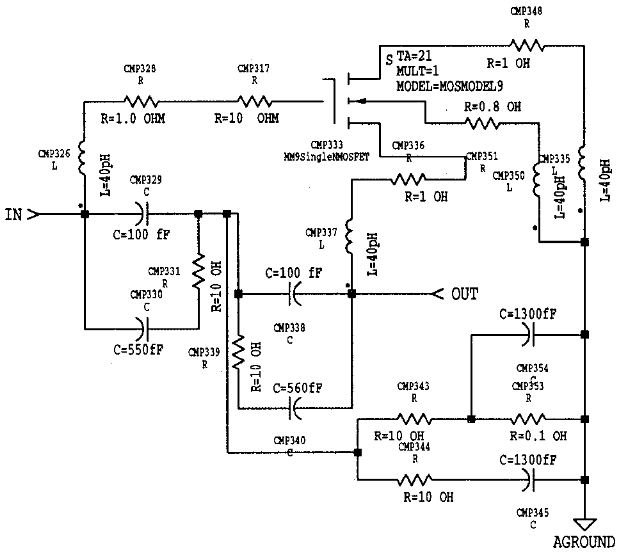

Figure 2: *Equivalent circuit of the MOS device embedded in the test structure as used in MDS.*

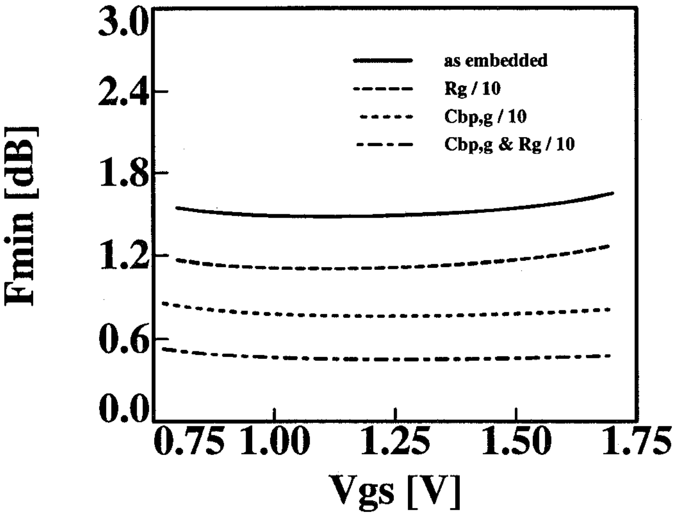

Figure 3: *Simulated minimum noise figure versus gate voltage at a frequency of 1.8 GHz and* $V_{ds} = 1.2V$ *of the 0.25 um nMOS.*

noise figure and the output conjugately matched for optimal power extraction. For model verification an on-wafer test structure containing 15 conventional 20/0.25 devices [6] in a parallel common source-bulk configuration, which could be contacted by ground-signal-ground coplanar RF probes, was used. Fig. 1 on the previous page shows minimum noise figures, which were measured versus gate voltage at 1.8 GHz and versus frequency at $V_{gs} = 1.1V$. The solid lines represent simulated values of the minimum noise figure. The starting point for the simulations are the MM9 current, charge and noise models. The junction capacitances are supplied by the JUNCAP model [3]. In the MM9 noise model both thermal noise from the channel current as well as the high frequency noise induced in the gate are included [3]. The effective gate resistance, 1/3 of the poly line resistance for a gate contacted at one side, 1/12 of the poly line resistance for a gate contacted at two sides, and the equivalent circuit of the on-wafer test structure are added. Finally the noise performance is calculated using the circuit simulator MDS. The equivalent circuit of the test structure was derived from its layout, verified against the S-parameters of representative "open" and "short" structures, and found to be accurate up to frequencies of 10 GHz. In general the interpretation of this kind of test structure results must be done with care because the noise performance measured at the RF probe tips might be degraded due to a limited Q of the bondpad and interconnect capacitances. In our case the simulations show that the extrinsic 1.5 dB noise figure at

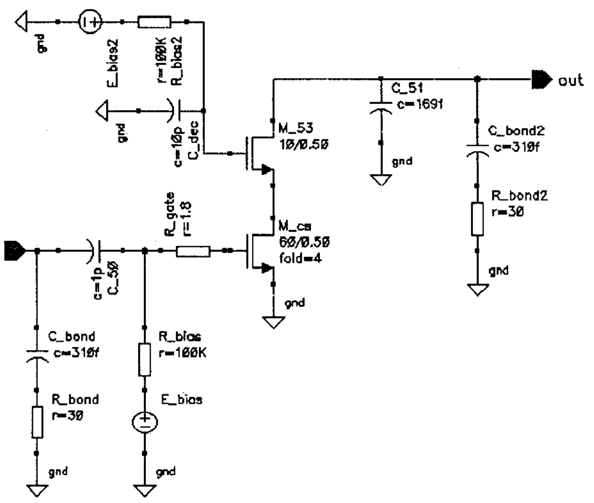

Figure 4: *Circuit of the Low Noise Amplifier realized in an industrial 0.5 μm IC process. The nMOS dimensions are 60/0.5 and 10/0.5. The on-chip bias circuits have been simplified.*

LNA @ 900 MHz	**Fmin dB**	**Ga dB**	$\|\Gamma opt\|$	$\angle\Gamma opt$	**Pd mW**
Measured	**2.2**	**16.9**	**0.923**	**14.64**	**1.8**
Simulated	**2.3**	**16.4**	**0.950**	**15.96**	**1.8**

Table 1: *Measured and simulated noise performance at 900 MHz of the LNA realized in an industrial 0.5 μm IC process. F is the minimum noise figure and Ga the associated available gain, both at the optimum source reflection coefficient* Γopt*. Pd is the total dissipated power.*

1.8 GHz of the embedded 0.25 μm MOS device can be improved to 0.76 dB when the lossy gate bondpad capacitance is removed (fig.3). The 0.25 μm test structure was primary designed for RF MM9 verification, and therefore its layout was not optimized for minimum gate resistance. However a gate resistance reduction from 10 to 1 Ω is quit feasible using a multi-finger structure. Simulations show that this would enable a noise figure of only 0.45 dB.

To investigate the feasibility of RF-CMOS for radio front-ends, and to verify noise figures at the circuit level, a two-stage (cascode, 60/0.5 and 10/0.5) LNA operating at 900 Mhz, was designed and realized in an industrial 0.5 μm IC process (fig. 4). On chip bias circuitry was included to adjust Ids to 550 μA, which according to the simulations would allow 16 dB gain and an input referred IP3 of -16 dBm. The LNA was designed for off-chip matching and therefore the noise parameters were measured as before using the automated tuners of the test setup for impedance matching. A minimum noise figure of 2.2 dB and an associated available gain of 16.9 dB were obtained. These values are in excellent agreement with the simulations (table 1). For the optimum source impedance a small deviation from the simulated value was found, mainly in its real part, which might be attributed to the fact that the influence of the substrate resistance [4,5] was not included in the circuit simulations. However the influence of the substrate resistance is generally only seen at frequencies much higher that the operating frequency of this circuit [4,5]. The excellent noise and gain performance were obtained at a record low power consumption of only 1.8 mW.

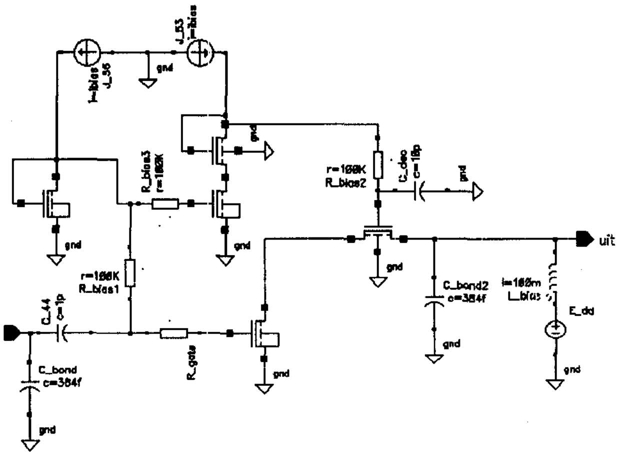

Figure 5: *Low Noise Amplifier design used for the performance scaling simulations. Note that the bondpad Q has been improved.*

Performance Scaling

Having verified that the RF noise behaviour for CMOS process generations down to 0.25 μm is modelled well by MM9, and that the noise figure of LNAs can be accurately simulated, the performance scaling of CMOS LNAs going towards smaller gate dimensions has been investigated. In this study the bondpad is shielded from the resistive substrate, resulting in the design depicted in fig. 5. Fig. 6 on the next page shows plots of the minimum noise figure and associated available gain versus dissipated power for a linear shrink of this LNA using the improved 0.5 μm version as a starting point. The simulations were performed with MM9 for three standard CMOS processes covering a range of five technology generations, with minimum gate dimensions of 0.5, 0.25, and 0.13 μm [6,7], and with scaled down supply voltages of 3.3, 2.5 and 1.5 Volts, respectively. These simulations demonstrate the great potential of RF-CMOS, particularly in the field of low power applications. Apart from the 0.5 μm process, the processes studied are sufficiently fast to allow high gain LNAs at frequencies up to 1800 MHz with noise figures below 1 dB. The increase in cut-off frequency with the decreasing effective gate length is clearly reflected in the improved LNA noise figure. Results like these allow the designer to chose the right CMOS process for realizing a specific circuit performance. The potential for power consumption reduction is reflected by the predicted feasibility of 27 dB gain and 1.1 dB noise figure at 1800 MHz at a minimal power consumption of only 0.2 mW for LNAs in 0.13 μm CMOS technology. This power consumption compares favorably to the 5 mW of their bipolar counterparts [8] which typically require a collector current of a few mA for optimal noise performance.

The need for impedance matching, which in this work is assumed to be taken care of by high Q off-chip components, is an issue which much be considered comparing RF designs made in bipolar, III-V and CMOS technologies. In fact, the reported 1.8 mW LNA requires an input VSWR of 25 for optimal performance (table 1), an issue which in practice will call for some attention. For bipolar devices the input VSWR is much lower due to the fairly high base resistance. This makes the matching circuit for bipolar easier to construct. On the other hand however, due to the high input VSWR of CMOS the large input voltage gain due to the use of high Q matching circuitry can more than compensate the approximately 3-fold smaller transconductance of the MOS-FET at identical drive current as compared to bipolar. Going to low power consumption and smaller dimensions, for CMOS the input VSWR increases even further, allowing the matching circuitry to compensate for a fairly large extend for the decrease in transconductance (fig. 6). With respect to the CMOS option it can be concluded that although high quality matching circuitry is required for optimum performance, the simulations reported here indicate that sufficient headroom exists with respect to available gain and

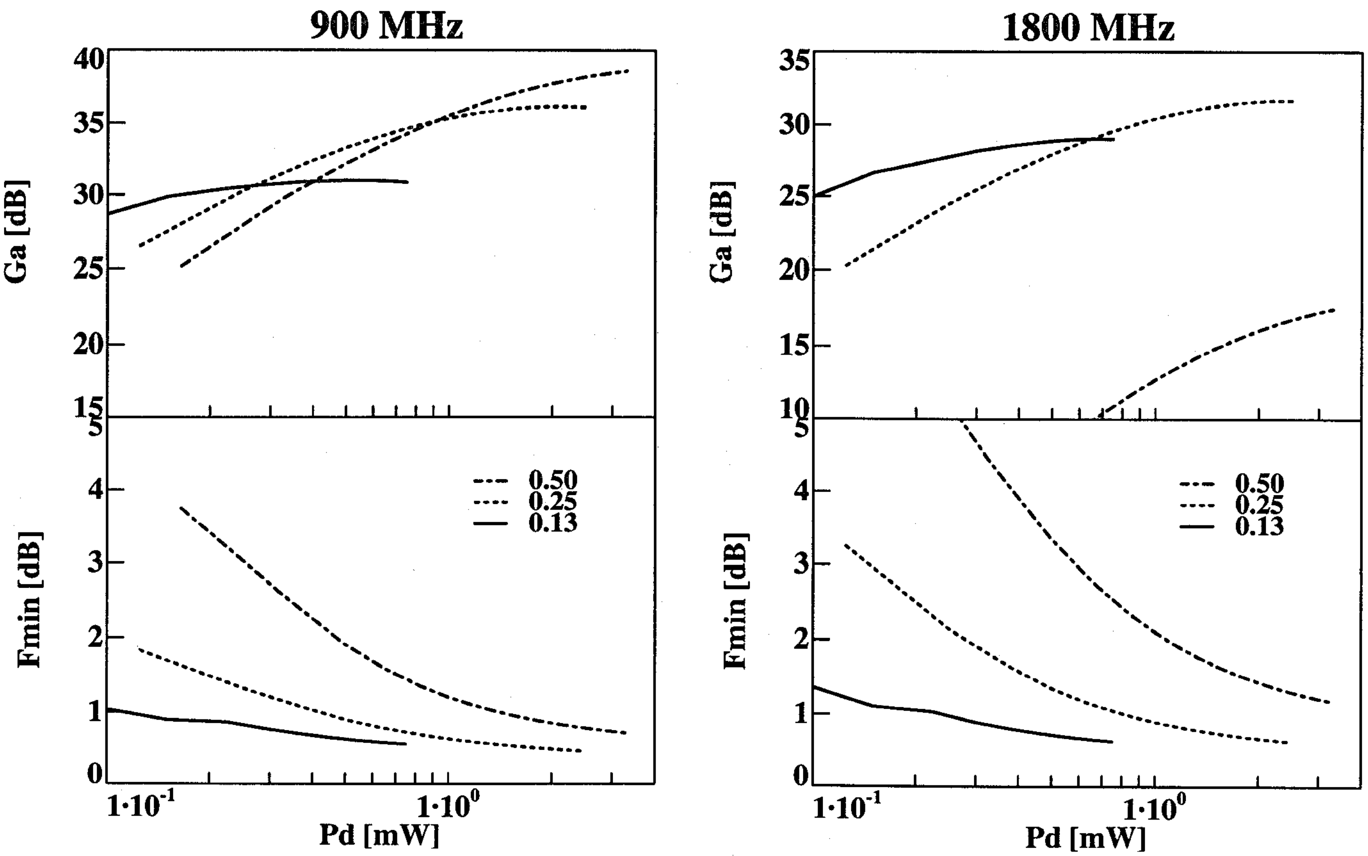

Figure 6: *Simulated LNA performance at 900 and 1800 MHz with respect to minimum noise figure and associated available gain. Results are shown versus dissipated power for processes with minimum gate dimensions of 0.5, 0.25, 0.18, and 0.13 μm, with down scaled supply voltages of 3.3, 2.5, 1.8 and 1.5 Volts, respectively.*

noise figure to compromise with practical matching solutions. The modelling tools presented here allow the circuit designer to exploit this option efficiently.

Conclusions

With the verification of the MM9 noise model on 0.25 μm CMOS and low power LNAs, a complete RF modelling tool for modern CMOS technology has been made available to the circuit designer. This is very significant, as CMOS LNAs can operate at extremely low power, provided suitable matching circuitry is used. This is illustrated by our prototype realized in an industrial 0.5 μm CMOS process, which achieved a noise figure of 2.2 dB at 900 MHz at a record low power consumption of only 1.8 mW. Furthermore simulations performed with parameter sets of standard CMOS processes with smaller gate dimensions reveal a great potential for further improvement. These simulations predict a noise figure of only 1.1 dB and 27 dB gain at 1800 MHz, at a power consumption of only 0.2 mW for a similar LNA in 0.13 μm CMOS technology.

Acknowledgments

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