

Compact MOS modeling for analog circuit simulation.

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Abstract

Analog applications of MOS transistors in integrated circuits impose enhanced requirements on the compact MOS models used in circuit simulators. Here we present for the Philips MOS MODEL 9 the successful confrontation with these analog requirements, the scaling of parameters with geometry, the accuracy of the model over the whole geometry range of a process, its capabilities in the description of various processes at least down to $0.35\ \mu\text{m}$ and a comparison with advanced analog models available in commercial circuit simulators.

Introduction

The enhanced requirements that have to be fulfilled by compact MOS models in analog design, have been reviewed recently [1]. A number of benchmark tests for analog compact MOS models have been presented and it has been demonstrated that even the most advanced commercially available models fail on a number of these tests [1]. In this paper we present a compact MOS model, MOS MODEL 9, that has been developed within Philips for analog applications and that until recently has been proprietary. Although our model has only half the number of parameters, it offers an even better performance than commercially available models and it is the first model to pass the benchmark tests for analog models mentioned above.

MOS MODEL 9

In our model all significant features of MOS transistor operation are included: e.g. back-bias dependence of the threshold voltage due to non-uniform doping [2], drain-induced barrier-lowering (for the subthreshold characteristics) [2], source and drain series resistance [3], avalanche multiplication and static feedback (for the drain conductance), channel-length modulation (in strong inversion) [4] and an accurate description of the charges [5, 6]. The main principles of the model have been discussed in the above references. Here the overall performance will be presented.

In MOS MODEL 9 the same expression for the current is used throughout all operating regions of the transistor. This leads to a smooth transition between the subthreshold and strong inversion regimes [7] (benchmark tests #1 and #2 of [1]), a smooth transition between the linear

and saturation regions (test #3 of [1]), and easy convergence during circuit simulation. The model uses only 15 electrical parameters to describe the individual transistor characteristics. Three additional parameters describing the avalanche multiplication are obtained from the substrate current. Due to this relatively small number of parameters and the physical basis of the model, parameters dominating the transistor behavior in each operating region are easily identified, which leads to unambiguous parameter extraction.

In figs. 1 to 4 the measured and simulated transistor characteristics are compared for an n-channel transistor with a gate width (W) of $10\ \mu\text{m}$ and a gate length (L) of $0.35\ \mu\text{m}$. This transistor was obtained from a $0.35\ \mu\text{m}$ CMOS process with $10\ \text{nm}$ gate oxide thickness (process 5 from table 3). In all transistor characteristics, symbols represent measurements and lines represent calculations with MOS MODEL 9. In addition in fig. 5 the measured and simulated output conductance of an n-channel transistor with $W/L=1.2/10$ from a process with $15\ \text{nm}$ gate oxide thickness is given (process 3 from table 3). The output conductance increasing with V_{ds} indicates avalanche multiplication. In particular for narrow transistors with low output conductance this effect is apparent. Well-scaled processes show little avalanche effects for small transistors as shown in fig. 4. The accurate modeling of the output conductance at gate voltages slightly above threshold, which is of paramount importance for analog applications, is also clearly demonstrated. The smooth transition between the subthreshold and strong inversion regimes is illustrated by the transconductance in fig. 6.

From figs. 1 to 6 it can be seen that MOS MODEL 9 describes individual transistors accurately and passes the benchmark tests for analog compact models mentioned above [1]: see fig. 3 for benchmark test #1; fig. 6 for test #2; and figs. 4 and 5 for a test that is more severe than #3 because of the logarithmic scale for the output conductance.

Scaling of parameters and accuracy over the geometry range of a process

The effective channel length and width are calculated using the gain factors (model parameter) and the mask length and width of the different transistors. Simple scaling rules describe the electrical parameters as a function of

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effective channel length and width (see e.g. figs. 7 and 8, where symbols represent the individual parameters and lines represent the scaling rules). These scaling rules have been derived from the physics on which our model is based, yielding 46 geometry-independent parameters. Additional scaling rules for the temperature dependence have also been established.

For analog applications the accuracy of compact MOS models cannot be indicated by comparing measured and simulated current levels for a few transistor geometries. Complete measured and simulated characteristics have to be compared in different operating regions, i.e. linear region (fig. 1), saturation region (fig. 2), subthreshold region (fig. 3), and output conductance (fig. 4). Moreover, these characteristics have to be compared over the whole geometry range of a process.

Table 1

L (in μm)	W (in μm)					
	10	5	2.4	2	1.2	1
10	×	×		×	×	×
5	×					
2	×	×				
1.6			×			
1.2	×					
1	×					
0.9	×					
0.8	×					×

Table 1 : Geometries with different gate width (W) and length (L) used to evaluate the accuracy of MOS MODEL 9 presented in table 2.

Using the electrical parameters following from the scaling rules mentioned above, the accuracy of MOS MODEL 9 was evaluated for process 3 from table 3. For all geometries indicated in table 1 the mean absolute deviation (in %) between the measured and simulated characteristics was calculated according to

$$\frac{1}{N} \sum_N \left| \frac{I_{\text{measured}} - I_{\text{simulated}}}{I_{\text{measured}}} \right|,$$

where N is the number of data for a specific bias condition. These deviations, averaged over several bias conditions (see figs. 1-4) and over the 14 transistor geometries of process 3 (given in table 1), are presented in table 2.

The deviations for the subthreshold region and the output conductance are much larger than those for the linear and the saturation region. This is due to the fact that both the subthreshold currents and the output conductance vary over several decades as can be seen from the logarithmic plots in figs. 3 to 5, while still the relative linear deviation is evaluated.

From table 2 it is clear that over the whole geometry range of the process our model achieves a high accuracy.

Table 2

		n-channel	p-channel
Linear region	$V_{sb} = 0 V$	1.2%	1.9%
	$V_{sb} \neq 0 V$	2.8%	3.2%
Saturation region	$V_{sb} = 0 V$	6.1%	4.7%
	$V_{sb} \neq 0 V$	5.9%	5.4%
Subthreshold region	$V_{sb} = 0 V$	12%	17%
	$V_{sb} \neq 0 V$	20%	31%
Output conductance	$V_{sb} = 0 V$	24%	15%
	$V_{sb} \neq 0 V$	23%	16%
Substrate current		26%	27%

Table 2 : Mean absolute deviation (in %) between the measured and simulated characteristics averaged over several bias conditions and over the 14 transistor geometries of process 3 given in table 1.

Comparison with commercially available models

In commercially available circuit simulators one of the most advanced compact MOS models for analog applications is the BSIM2 model. With more than 30 electrical parameters and 90 geometry-independent parameters, BSIM2 uses twice the number of parameters needed for MOS MODEL 9. As already mentioned in the literature [1], BSIM2 predicts the output conductance rather inaccurately in the transition from the linear to saturation regime (test #3 of [1]). Our model, however, describes this transition accurately (see figs. 4 and 5). If a whole range of geometries is taken into account, the above deficiency of BSIM2 becomes even more severe.

Modeling of various processes down to 0.35 μm

Circuit simulation in general and parameter extraction in particular are greatly facilitated if the same compact MOS model can be used for a large number of processes. MOS MODEL 9 is used for production processes and has been tested extensively on research processes. A selection of processes for which parameter extraction has been performed is shown in table 3.

Table 3

Process	T_{ox}	Minimal gate length
1	25.0 nm	1.6 μm
2	20.0 nm	1.0 μm
3	15.0 nm	0.8 μm
4	12.5 nm	0.5 μm
5	10.0 nm	0.35 μm

Table 3 : Different processes [8, 9] with gate oxide thickness and minimal gate length for which parameter sets for MOS MODEL 9 have been determined.

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For the p-channel transistors of the processes in table 3, fig. 7 shows the parameter V_{TO} , the threshold voltage, as a parabolic function of the inverse effective length (symbols represent the individual parameters and lines represent the scaling rules). The threshold voltage roll-up is clearly visible [10]. The scaling of the parameter θ_1 , including both the mobility reduction due to the transversal field and effects of series resistance, is shown in fig. 8 for the p-channel transistors. Differences in series resistance between the processes are reflected by the slope of the lines. The intercept of the y-axis represents the influence of the transversal field. Both in series resistance and in transversal field buried p-channel transistors (processes 1-4) and surface p-channel transistors (process 5) are quite different [3].

From figs. 7 and 8 (and figs. 1-4) it is clear that our model is process-independent and it can be used without modifications for processes down to $0.35 \mu\text{m}$. The performance for a $0.25 \mu\text{m}$ process [11] is currently under investigation.

Conclusions

The Philips compact MOS MODEL 9: 1) is excellently suited for both digital and analog applications; 2) is the first compact MOS model to pass the benchmark tests for analog models [1]; 3) offers a better performance than the more complicated BSIM2 model, although it has only half the number of parameters; 4) describes the full range of geometries available in an IC process with excellent accuracy; 5) maintains this accuracy for processes at least down to $0.35 \mu\text{m}$.

Acknowledgement

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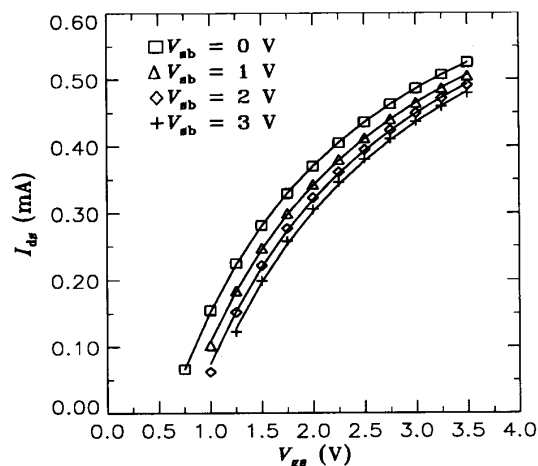


Figure 1: Linear characteristics ($V_{ds} = 0.1 \text{ V}$) of a $10/0.35$ n-channel transistor of process 5 (table 3).

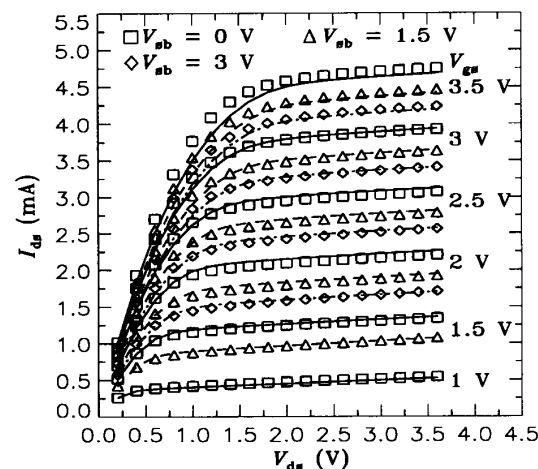


Figure 2: Saturation characteristics of a $10/0.35$ n-channel transistor of process 5 (table 3).

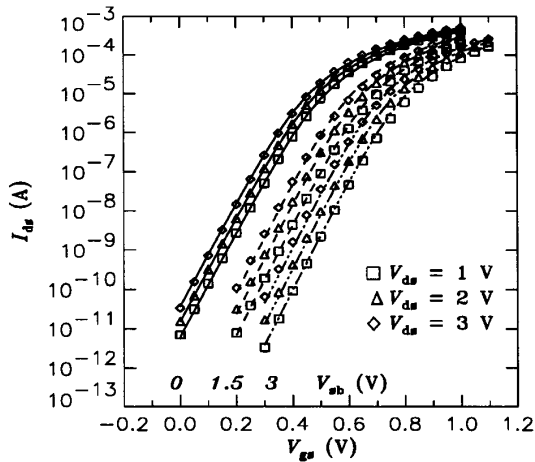


Figure 3: Subthreshold characteristics of a 10/0.35 n-channel transistor of process 5 (table 3).

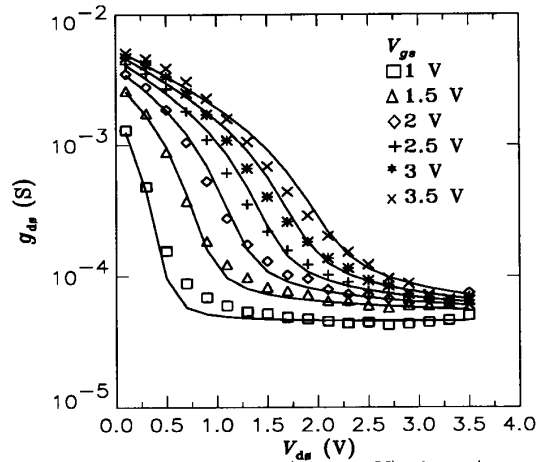


Figure 4: Output conductance ($V_{sb} = 0$ V) of a 10/0.35 n-channel transistor of process 5 (table 3).

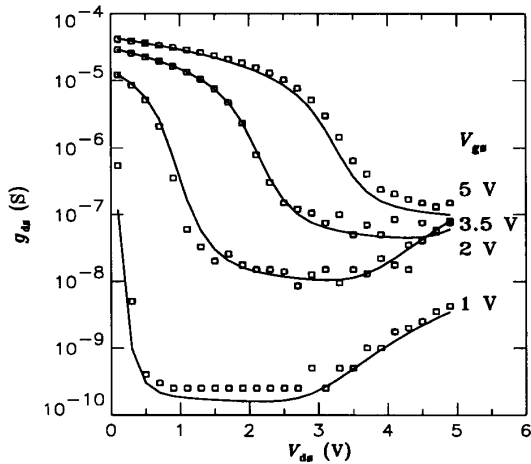


Figure 5: Output conductance ($V_{sb} = 0$ V) of a 1.2/10 n-channel transistor of process 3 (table 3).

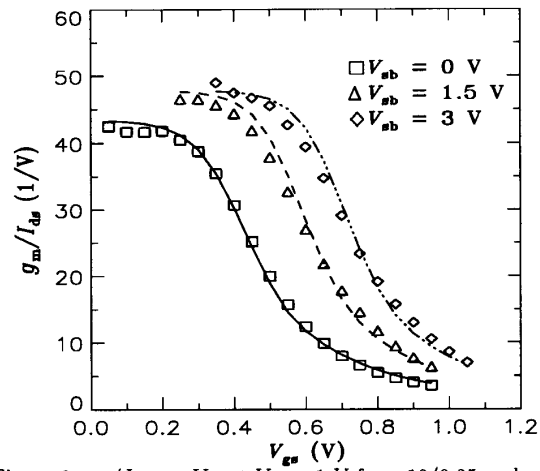


Figure 6: g_m/I_{ds} vs. V_{gs} at $V_{ds} = 1$ V for a 10/0.35 n-channel transistor of process 5 (table 3).

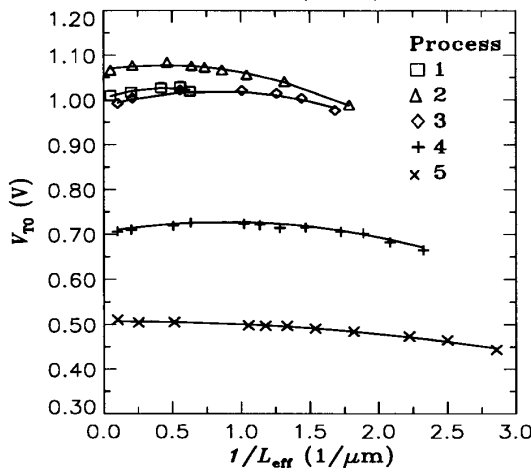


Figure 7: Scaling of the threshold voltage V_{T0} as a function of $1/L_{eff}$ for p-channel transistors of the 5 processes in table 3.

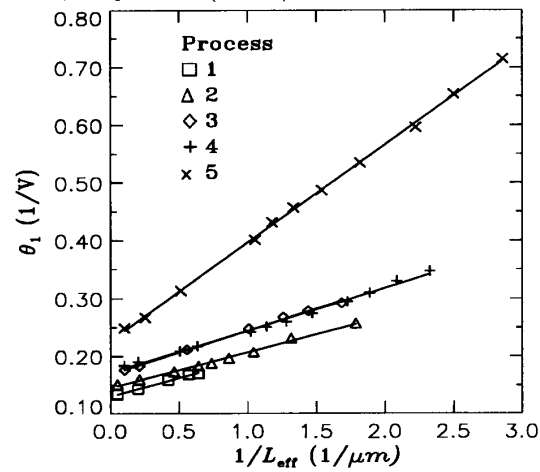


Figure 8: Mobility reduction parameter θ_1 as a function of $1/L_{eff}$ for p-channel transistors of the 5 processes in table 3.

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