14-Bit Bus Switch/Multiplexer for DDR2/DDR3/DDR4 Applications

CBTW28DD14

Archived

This page contains information on a product that is no longer manufactured (discontinued). Specifications and information herein are available for historical reference only.

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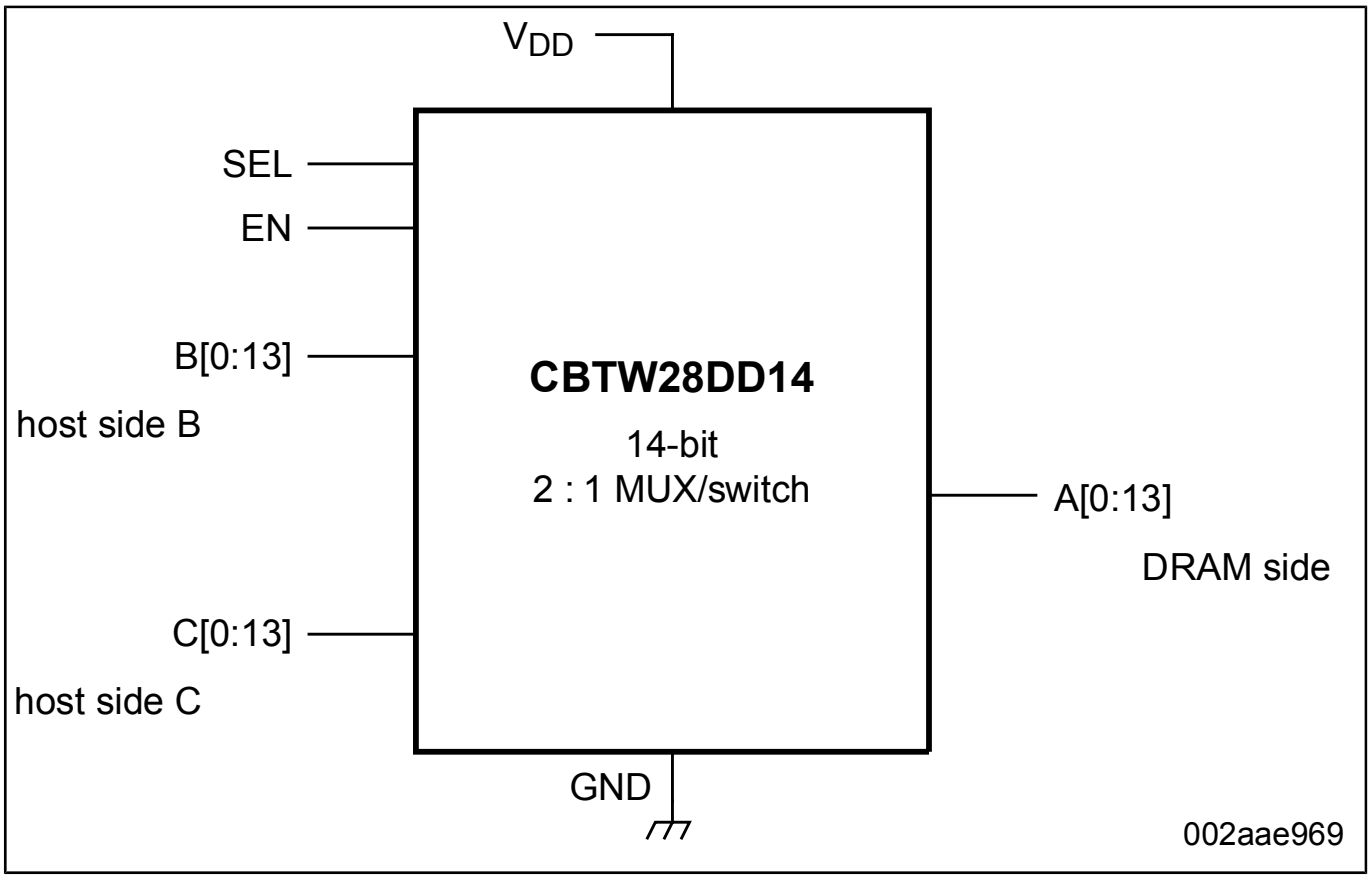
This 14-bit bus switch/multiplexer (MUX) is designed for 1.5 V or 1.8 V supply voltage operation, POD_12, SSTL_12, SSTL_135, SSTL_15 or SSTL_18 signaling and CMOS select input levels. It is designed for operation in DDR2, DDR3 or DDR4 memory bus systems.

The CBTW28DD14 has a 1 : 2 switch or 2 : 1 multiplex topology and offers a 14-bit wide bus. Each 14-bit wide A-port can be switched to one of two ports B and C, for all bits simultaneously. The selection of the port is by a simple CMOS input (SELect). Another CMOS input (ENable) is available to allow all ports to be disconnected. Each port is non-directional due to the use of FET switches, allowing a multitude of applications requiring high-bandwidth switching or multiplexing.

The SEL and EN input signals are designed to operate transparently as CMOS input level signals in both 1.5 V and 1.8 V supply voltage conditions.

CBTW28DD14 uses NXP proprietary high-speed switch architecture providing high bandwidth, very little insertion loss at low frequency, and very low propagation delay, allowing use in many applications requiring switching or multiplexing of high-speed signals. It is available in a 4.5 mm x 4.5 mm TFBGA48 package with 0.5 mm ball pitch, for optimal size versus board layout density considerations. It is characterized for operation from -10 °C to +85 °C.

CBTW28DD14 Block Diagram Block Diagram



View additional information for 14-Bit Bus Switch/Multiplexer for DDR2/DDR3/DDR4 Applications.

Note: The information on this document is subject to change without notice.