Parallel Bus to Three-Channel Fm+ I²C-Bus Controller

PCA9663B

Archived

This page contains information on a product that is no longer manufactured (discontinued). Specifications and information herein are available for historical reference only.

Last Updated: May 26, 2023

The PCA9663 is an advanced single leader mode I²C-bus controller. It is a fourth generation bus controller designed for data intensive I²C-bus data transfers. It has three independent I²C-bus channels with data rates up to 1 Mbits/s using the Fast-mode Plus (Fm+) open-drain topology. Each channel has a generous 4352 byte data buffer which makes the PCA9663 the ideal companion to any CPU that needs to transmit and receive large amounts of serial data.

The PCA9663 is a 8-bit parallel-bus to I²C-bus protocol converter. Each channel can be configured to communicate with up to 64 followers in one serial sequence with no intervention from the CPU. The controller also has a sequence loop control feature that allows it to automatically retransmit a stored sequence.

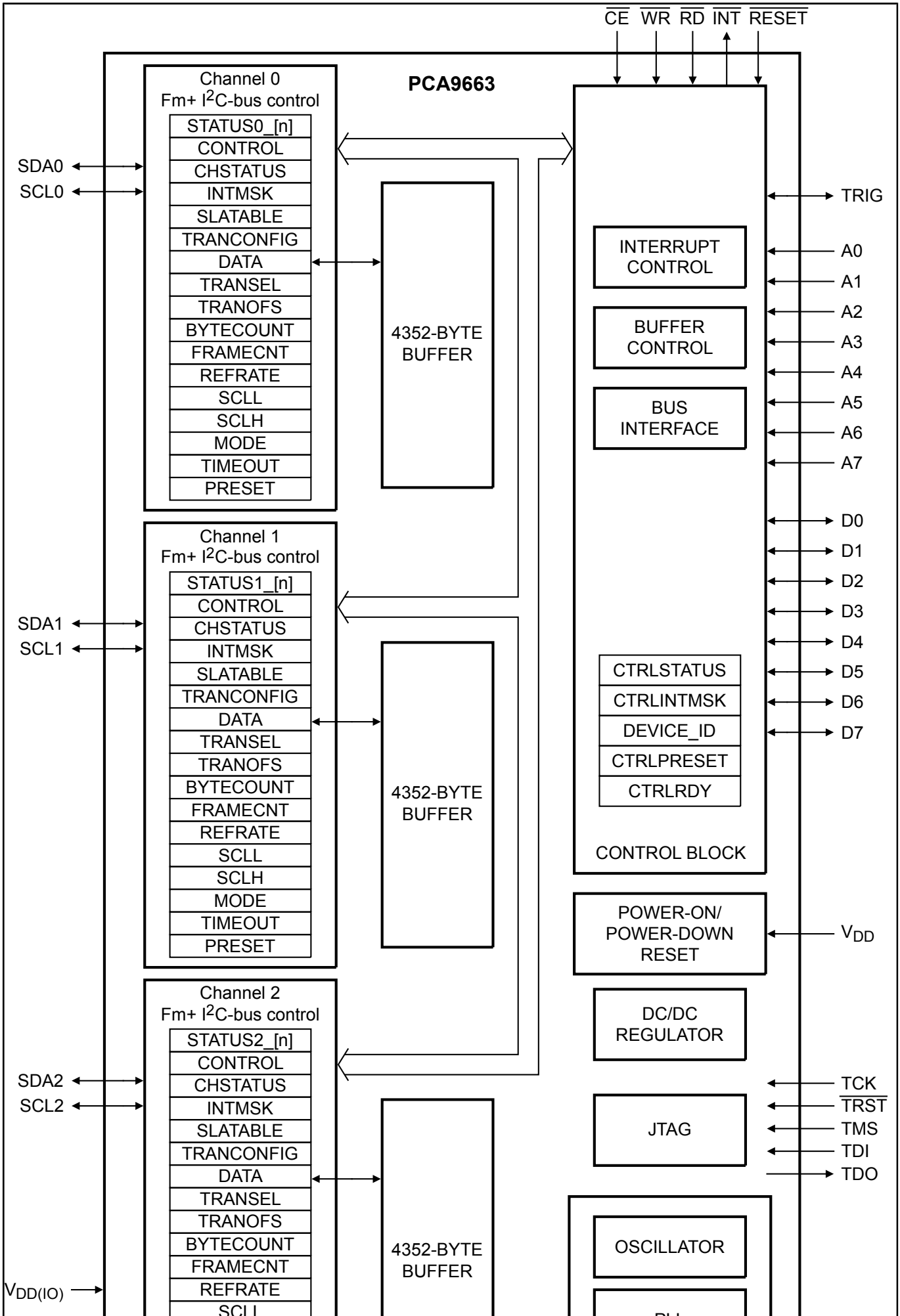
Its onboard oscillator and PLL allow the controller to generate the clocks for the I²C-bus and for the interval timer used in sequence looping. This feature greatly reduces CPU overhead when data refresh is required in fault tolerant applications.

An external trigger input allows data synchronization with external everts. The trigger signal controls the rate at which a stored sequence is re-transmitted over the I²C-bus.

Error reporting is handled at the transaction level, channel level and controller level with a simple interrupt tree and interrupt masks allow further customization of interrupt management.

The controller and parallel bus interfaces run at 3.3 V and the I²C-bus I/Os are 5 V tolerant with logic levels referenced to a dedicated VDD(IO) input pin with a range of 3.0 V to 5.5 V.

PCA9663 BLOCK DIAGRAM Block Diagram


PCA9663
CE
WR
RD
INT
RESET
Channel 0
Fm+ I2C-bus control
STATUS0_[n]
CONTROL
CHSTATUS
INTMSK
SLATABLE
TRANCONFIG
DATA
TRANSEL
TRANOFS
BYTECOUNT
FRAMECNT
REFRATE
SCLL
SCLH
MODE
TIMEOUT
PRESET
4352-BYTE BUFFER
Channel 1
Fm+ I2C-bus control
STATUS1_[n]
CONTROL
CHSTATUS
INTMSK
SLATABLE
TRANCONFIG
DATA
TRANSEL
TRANOFS
BYTECOUNT
FRAMECNT
REFRATE
SCLL
SCLH
MODE
TIMEOUT
PRESET
4352-BYTE BUFFER
Channel 2
Fm+ I2C-bus control
STATUS2_[n]
CONTROL
CHSTATUS
INTMSK
SLATABLE
TRANCONFIG
DATA
TRANSEL
TRANOFS
BYTECOUNT
FRAMECNT
REFRATE
SCLL
4352-BYTE BUFFER
SDA0
SCL0
SDA1
SCL1
SDA2
SCL2
VDD(IO)
INTERRUPT CONTROL
BUFFER CONTROL
BUS INTERFACE
CTRLSTATUS
CTRLINTMSK
DEVICE_ID
CTRLPRESET
CTRLRDY
CONTROL BLOCK
POWER-ON/ POWER-DOWN RESET
DC/DC REGULATOR
JTAG
OSCILLATOR
TRIG
A0
A1
A2
A3
A4
A5
A6
A7
D0
D1
D2
D3
D4
D5
D6
D7
VDD
TCK
TRST
TMS
TDI
TDO

View additional information for Parallel Bus to Three-Channel Fm+ I²C-Bus Controller.

Note: The information on this document is subject to change without notice.