



# Fm+ Parallel Bus to I<sup>2</sup>C-Bus Controller

## PCA9665\_PCA9665A

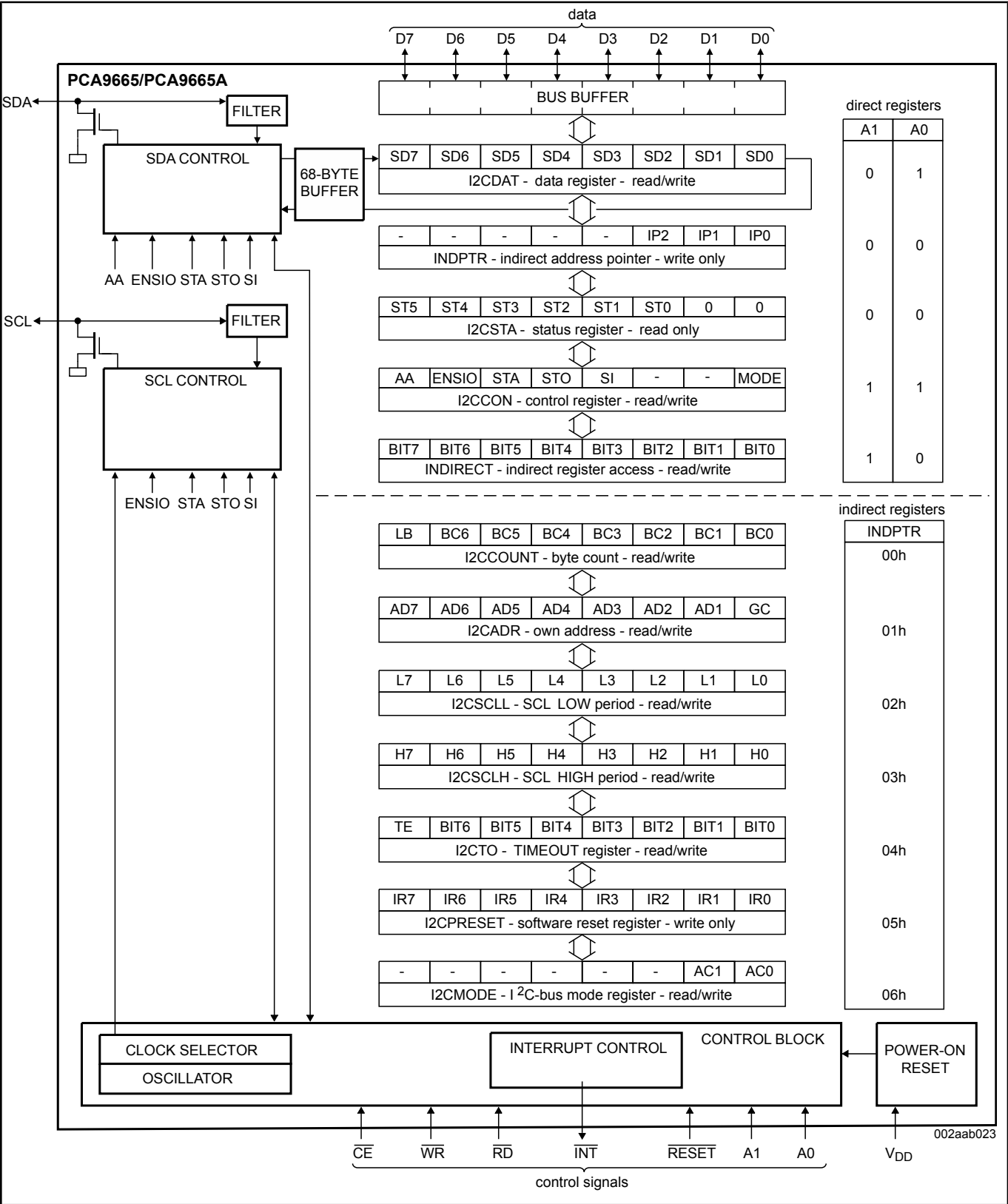
Last Updated: Jun 15, 2022

The PCA9665/PCA9665A serves as an interface between many standard parallel-bus microcontrollers/microprocessors and the serial I<sup>2</sup>C-bus and allows the parallel bus system to communicate bidirectionally with the I<sup>2</sup>C-bus. The PCA9665/PCA9665A can operate as a leader or a follower and can be a transmitter or receiver. Communication with the I<sup>2</sup>C-bus is carried out on a Byte or Buffered mode using interrupt or polled handshake. The PCA9665/PCA9665A controls all the I<sup>2</sup>C-bus specific sequences, protocol, arbitration and timing with no external timing element required.

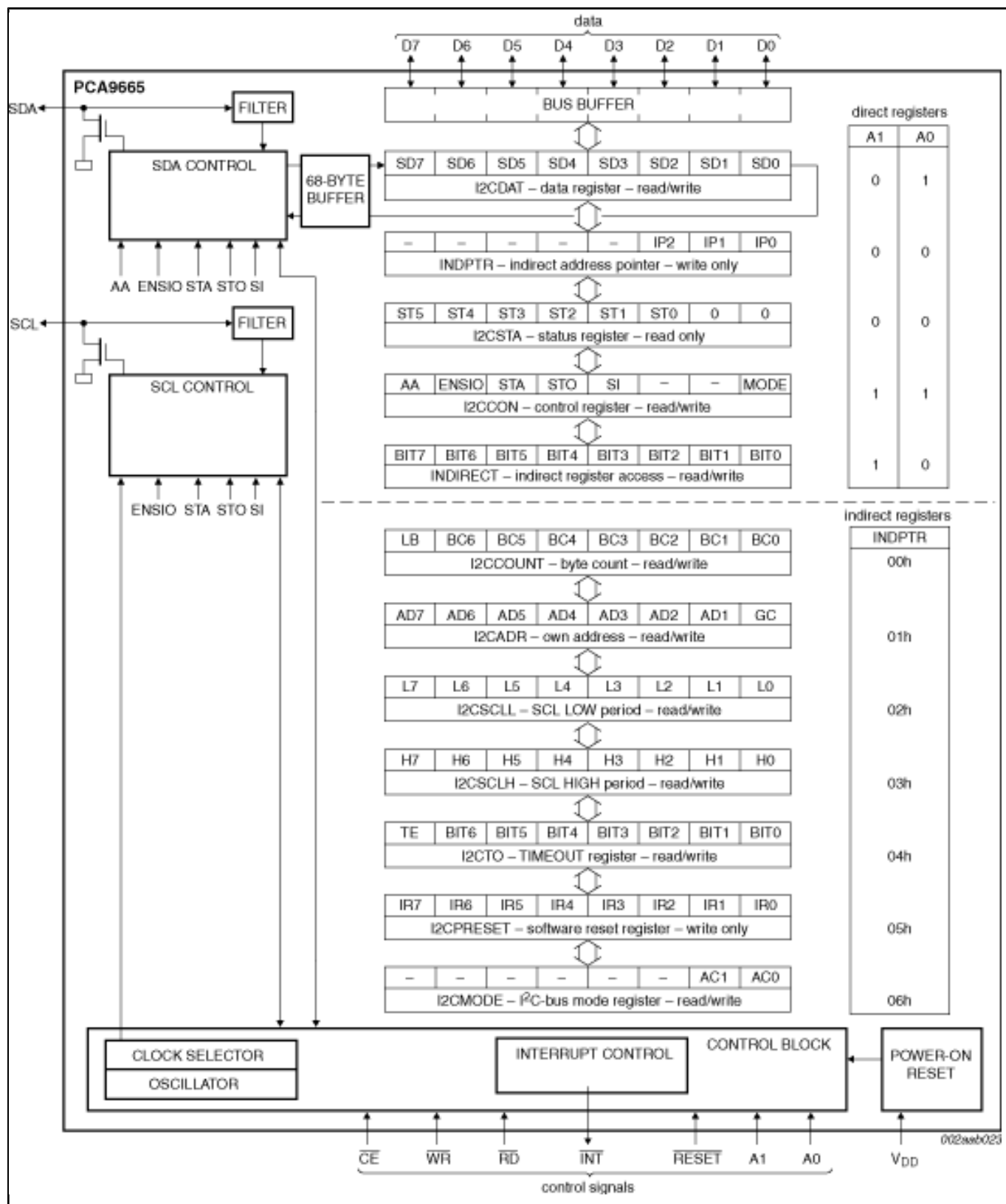
The PCA9665 and PCA9665A have the same footprint as the PCA9564 with additional features:

- 1 MHz transmission speeds
- Up to 25 mA drive capability on SCL/SDA
- 68-byte buffer
- I<sup>2</sup>C-bus General Call
- Software reset on the parallel bus

PCA9665\_PCA9665A BLOCK DIAGRAM Block Diagram



Block diagram: PCA9665BS, PCA9665D, PCA9665N, PCA9665PW Block Diagram



View additional information for [Fm+ Parallel Bus to I<sup>2</sup>C-Bus Controller](#).

Note: The information on this document is subject to change without notice.

**[www.nxp.com](http://www.nxp.com)**

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2024 NXP B.V.