



Remote 8-Bit I/O Expander for Fm+ I²C-Bus with Interrupt and Reset

PCA9672

Last Updated: Mar 18, 2024

The PCA9672 provides general-purpose remote I/O expansion via the two-wire bidirectional I²C#bus (serial clock (SCL), serial data (SDA)).

The devices consist of eight quasi-bidirectional ports, 1 MHz 30 mA drive I²C#bus interface, three hardware address inputs and a reset input operating between 2.3 V and 5.5 V. 1 MHz I²C#bus Fast-mode Plus (Fm+) can support PWM dimming of LEDs and higher I²C#bus drive 30 mA allows more devices to be on the bus without the need for bus buffers. The quasi-bidirectional port can be independently assigned as an input to monitor interrupt status or keypads, or as an output to activate indicator devices such as LEDs. The system controller can read from the input port or write to the output port through a single register.

The low current consumption of 2.5 μ A (typical, static) is great for mobile applications and the latched output ports have 25 mA high current sink drive capability for directly driving LEDs.

The PCA9672 has two hardware address pins, allowing sixteen of each device to be on the same I²C#bus without the need for bus buffers, so there can be supporting up to 128 I/Os (for example, 128 LEDs).

The active LOW open-drain interrupt output (INT) can be connected to the interrupt logic of the microcontroller and is activated when any input state differs from its corresponding input port register state. It is used to indicate to the microcontroller that an input state has changed and the device needs to be interrogated without the microcontroller continuously polling the input register via the I²C#bus.

The internal Power-On Reset (POR) and active LOW hardware reset pin (RESET) initialize the I/Os as inputs with a weak internal pull-up 100 μ A current source.

The block diagram illustrates the internal architecture of the PCA9672 chip. Key components and their connections include:

- External Pins:**
 - $\overline{\text{INT}}$: Interrupt output pin.
 - AD0 , AD1 : Address pins for the I/O port.
 - SCL , SDA : I²C bus pins.
 - $\overline{\text{RESET}}$: Reset pin.
 - V_{DD} , V_{SS} : Power supply pins.
 - P0 to P7 : 8-bit parallel data port.
- Internal Blocks:**
 - LP FILTER**: Low-pass filter for the interrupt signal.
 - INTERRUPT LOGIC**: Manages the interrupt signal.
 - INPUT FILTER**: Filters the SDA pin for noise.
 - I²C-BUS CONTROL**: Manages communication with the I²C bus.
 - SHIFT REGISTER**: Converts parallel data from the I/O port to serial data for the I²C bus.
 - I/O PORT**: An 8-bit parallel port connected to pins P0-P7.
 - POWER-ON RESET**: Resets the chip upon power-up.
- Connections:**
 - $\overline{\text{INT}}$ is connected to the Interrupt Logic and passes through an LP Filter.
 - AD0 and AD1 are connected to the I/O Port.
 - SCL and SDA are connected to the I²C-Bus Control and the Input Filter.
 - $\overline{\text{RESET}}$ is connected to the Power-On Reset block.
 - V_{DD} and V_{SS} are connected to the Power-On Reset block.
 - The I²C-Bus Control is connected to the Shift Register and the I/O Port via 8-bit data buses.
 - The Shift Register is connected to the I/O Port via 8-bit data buses.
 - The I/O Port is connected to the external P0 to P7 pins.
 - The I²C-Bus Control is also connected to the Input Filter and the LP Filter.

The block diagram of the PCA9672 chip shows the following internal components and connections:

- External Inputs/Outputs:**
 - INT**: Interrupt output.
 - AD0, AD1**: Address inputs.
 - SCL, SDA**: I²C bus signals.
 - RESET**: Reset input.
 - V_{DD}, V_{SS}**: Power supply inputs.
 - P0 to P7**: General-purpose I/O port outputs.
- Internal Blocks:**
 - POWER-ON RESET**: Receives **RESET**, **V_{DD}**, and **V_{SS}** signals.
 - INPUT FILTER**: Receives **SCL** and **SDA** signals.
 - I²C-BUS CONTROL**: Receives **AD0** and **AD1** signals, and is connected to the **INPUT FILTER**, **SHIFT REGISTER**, and **I/O PORT**.
 - SHIFT REGISTER**: Connected to the **I²C-BUS CONTROL** and **I/O PORT**. It has **write pulse** and **read pulse** inputs.
 - I/O PORT**: Connected to the **SHIFT REGISTER** and provides **P0 to P7** outputs.
 - LP FILTER**: Connected to the **I/O PORT** and **INT**.
 - INTERRUPT LOGIC**: Receives signals from the **LP FILTER** and **I²C-BUS CONTROL** to generate the **INT** signal.

View additional information for [Remote 8-Bit I/O Expander for Fm+ I²C-Bus with Interrupt and Reset](#).

Note: The information on this document is subject to change without notice.

www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2024 NXP B.V.