2-1 I2C-Bus Controller Selector with Interrupt Logic and Reset

PCA9541A

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The PCA9541A is a 2-to-1 I²C-bus controller selector designed for high reliability dual controller I²C-bus applications where system operation is required, even when one controller fails or the controller card is removed for maintenance. The two controllers (for example, primary and back-up) are located on separate I²C-buses that connect to the same downstream I²C-bus target devices. I²C-bus commands are sent by either I²C-bus controller and are used to select one controller at a time. Either controller at any time can gain control of the target devices if the other controller is disabled or removed from the system. The failed controller is isolated from the system and will not affect communication between the on-line controller and the target devices on the downstream I²C-bus.

Two versions are offered for different architectures. PCA9541A/01 with channel 0 selected at start-up, and PCA9541A/03 with no channel selected after start-up.

The interrupt outputs are used to provide an indication of which controller has control of the bus. One interrupt input (INT_IN) collects downstream information and propagates it to the 2 upstream I²C-buses (INT0 and INT1) if enabled. INT0 and INT1 are also used to let the previous bus controller know that it is not in control of the bus anymore and to indicate the completion of the bus recovery/initialization sequence. Those interrupts can be disabled and will not generate an interrupt if the masking option is set.

A bus recovery/initialization if enabled sends nine clock pulses, a not acknowledge, and a STOP condition in order to set the downstream I²C-bus devices to an initialized state before actually switching the channel to the selected controller.

An interrupt is sent to the upstream channel when the recovery/initialization procedure is completed.

An internal bus sensor senses the downstream I²C-bus traffic and generates an interrupt if a channel switch occurs during a non-idle bus condition. This function is enabled when the PCA9541A recovery/initialization is not used. The interrupt signal informs the controller that an external I²C-bus recovery/initialization must be performed. It can be disabled and an interrupt will not be generated.

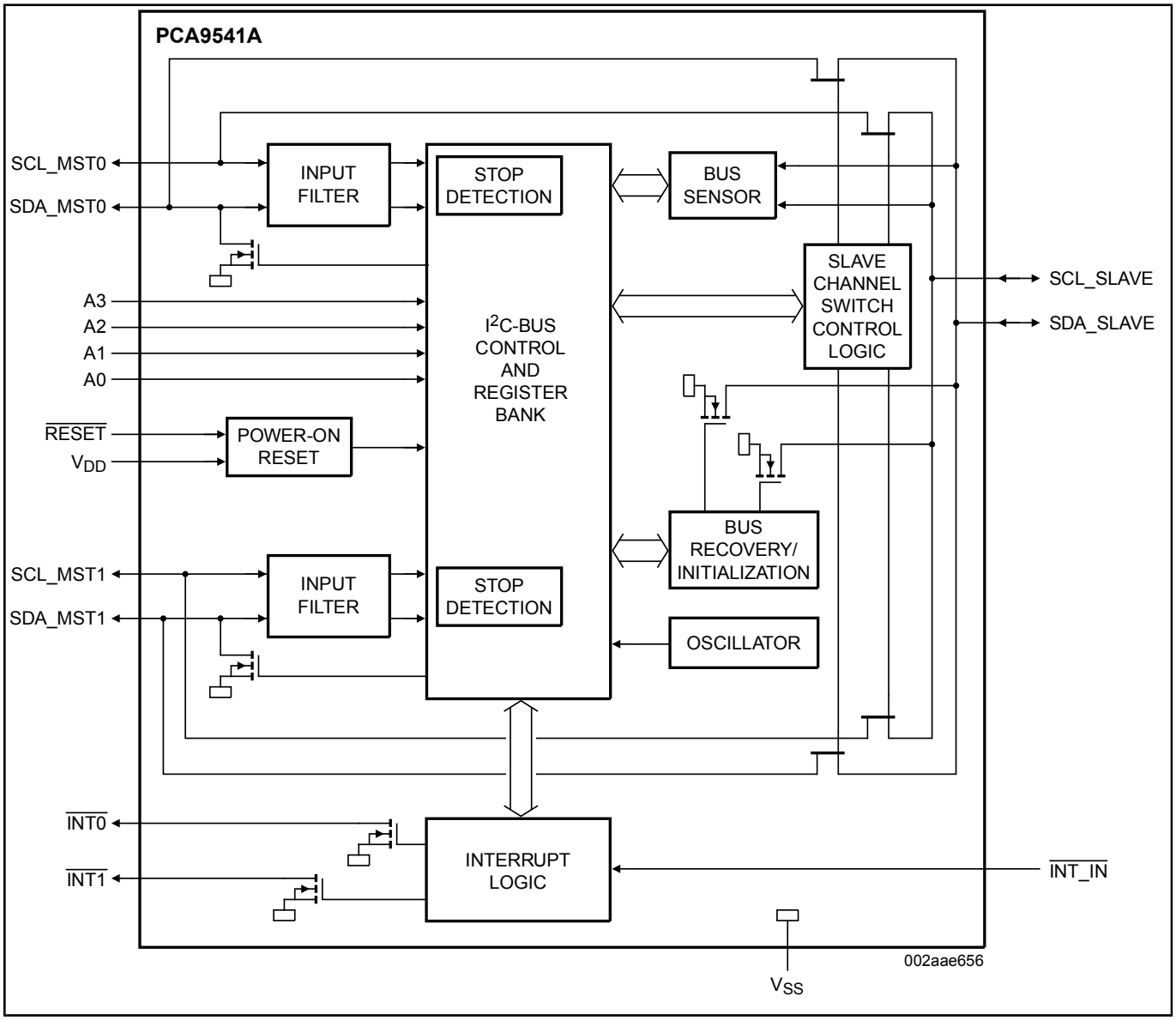
The pass gates of the switches are constructed such that the VDD pin can be used to limit the maximum high voltage, which will be passed by the PCA9541A. This allows the use of different bus voltages on each pair, so that 1.8 V, 2.5 V, or 3.3 V devices can communicate with 5 V devices without any additional protection.

The PCA9541A does not isolate the capacitive loading on either side of the device, so the designer must take into account all trace and device capacitances on both sides of the device, and pull-up resistors must be used on all channels.

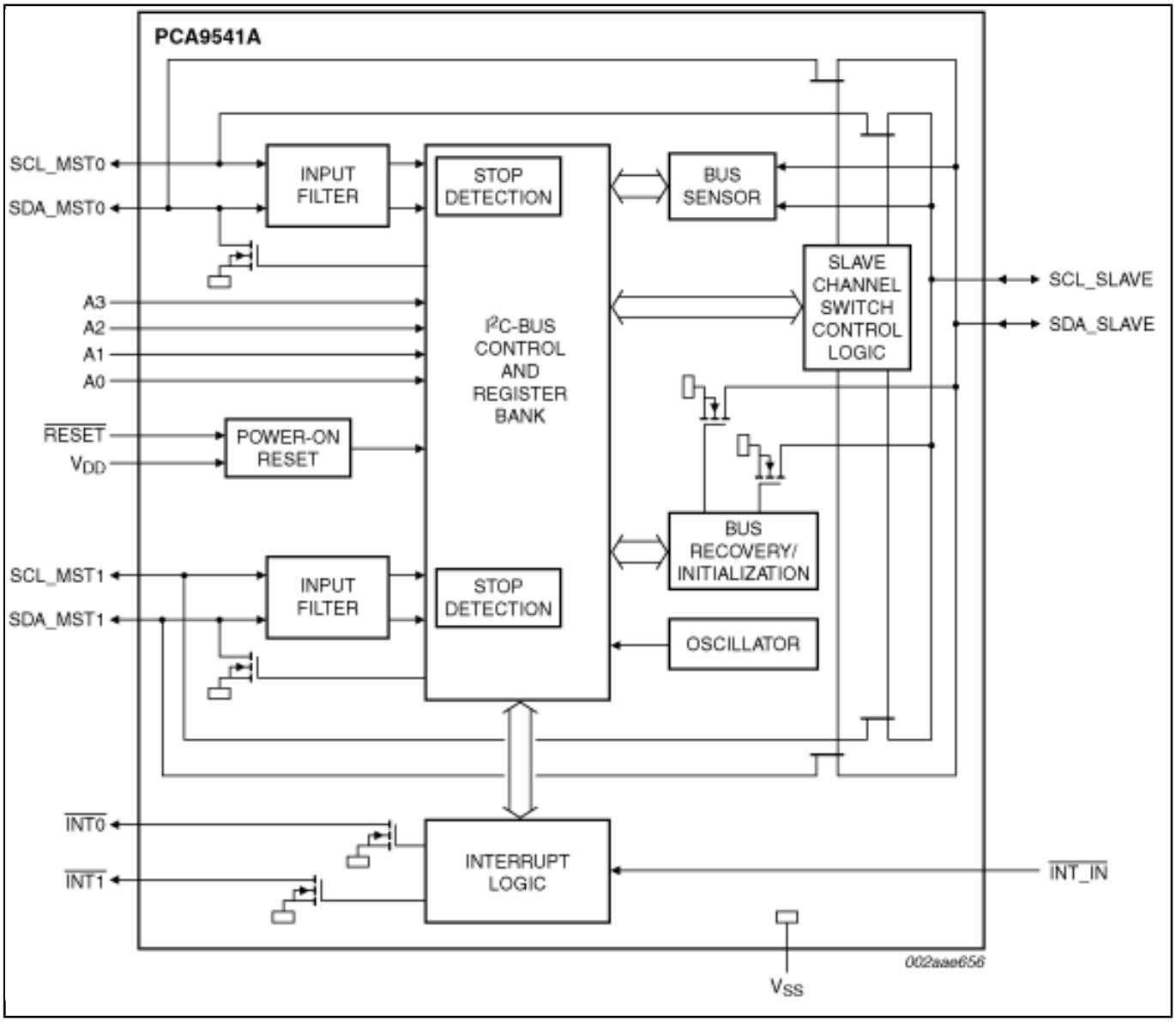
External pull-up resistors pull the bus to the desired voltage level for each channel. All I/O pins are 6.0 V tolerant.

An active LOW reset input allows the PCA9541A to be initialized. Pulling the RESET pin LOW resets the I²C-bus state machine and configures the device to its default state as does the internal Power-On Reset (POR) function.

PCA9541A Block Diagram



PCA9541ABS, PCA9541AD, PCA9541APW Block Diagram



View additional information for 2-1 I2C-Bus Controller Selector with Interrupt Logic and Reset.

Note: The information on this document is subject to change without notice.