Orlando
2005

Freescale
Technology
Forum

Network. Connect. Explore.

Discover the Power of ‘e’

Comparing and Contrasting Freescale's PowerPC® SoC Platforms

e300 e500 e600

Kyle S. Aubrey
Freescale Field Applications Engineer, Silicon Valley

freescale semiconductor

Freescale Technology Forum
NAR477 Session Abstract

- **Length:** 1 Hour (Tuesday 11:00am-12:00pm)
- **Abstract Title:** "Discover the Power of 'e': Comparing and Contrasting Freescale's PowerPC® SoC Platforms – e300, e500, e600"
- **Presenter's Name & Title:**
  Kyle Aubrey, Freescale NCSG Field Applications Engineer – Silicon Valley, CA
- **Level:** Intermediate
- **Architecture:** PowerQUICC™ II-PRO, PowerQUICC™ III, PowerPC®, Next Generation
- **Abstract:** Freescale's PowerPC System-on-Chip (SoC) Platforms combine the company's PowerPC core portfolio with its broad Intellectual Property (IP) portfolio to deliver scalable performance, from low to high, to meet a wide spectrum of processing, I/O, and functional requirements. This session is designed to assist development engineers to quickly gain an understanding of Freescale's e300, e500, and e600 PowerPC SoC platforms, and how they compare. In addition, hardware and software design considerations and strategies for migrating through the platforms are discussed. Basic familiarity of the PowerPC architecture and data communications is required.
- **Intended Audience:** Networking, communications, and pervasive computing engineers developing a low- to high-end platform strategy or planning to upgrade or cost reduce their current PowerPC based design for scaled performance, connectivity, and integration while leveraging existing design investments.

Session Overview

- **Introduction to Freescale's SoC Platforms**
  - History and Evolution of SoC at Freescale
  - MPC83xx, 85xx, 86xx Platforms and Available Standard Products
- **Scalable Performance**
  - Core Comparisons and Advantages: e300, e500, e600
  - Application Software Compatibility
- **Scalable Connectivity**
  - Peripherals and Interfaces
- **Scalable Integration**
  - Buses and Controllers
  - Driver Software Compatibility
- **Session Summary**
- **Questions**

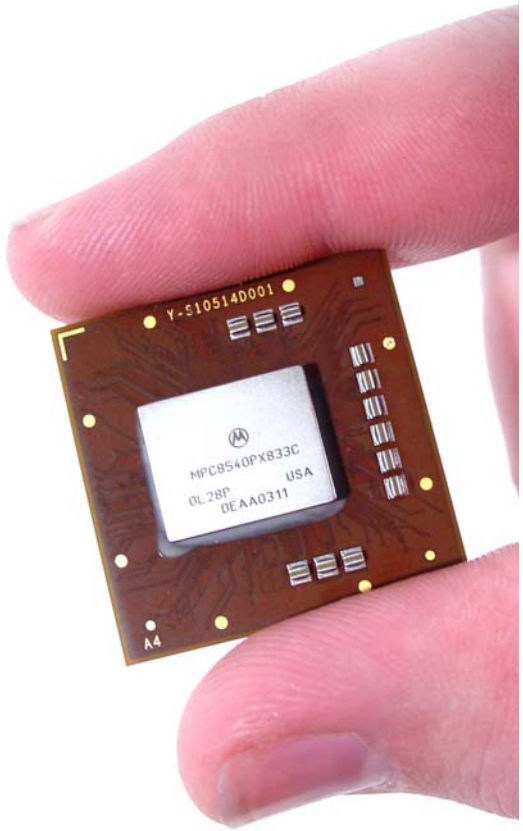
Freescale SoC Platforms: A Little History...

MPC8560 PowerQUICC III

Best High-Performance Embedded Processor

Microprocessor Report Analysts' Choice

Freescale's First SoC Platform



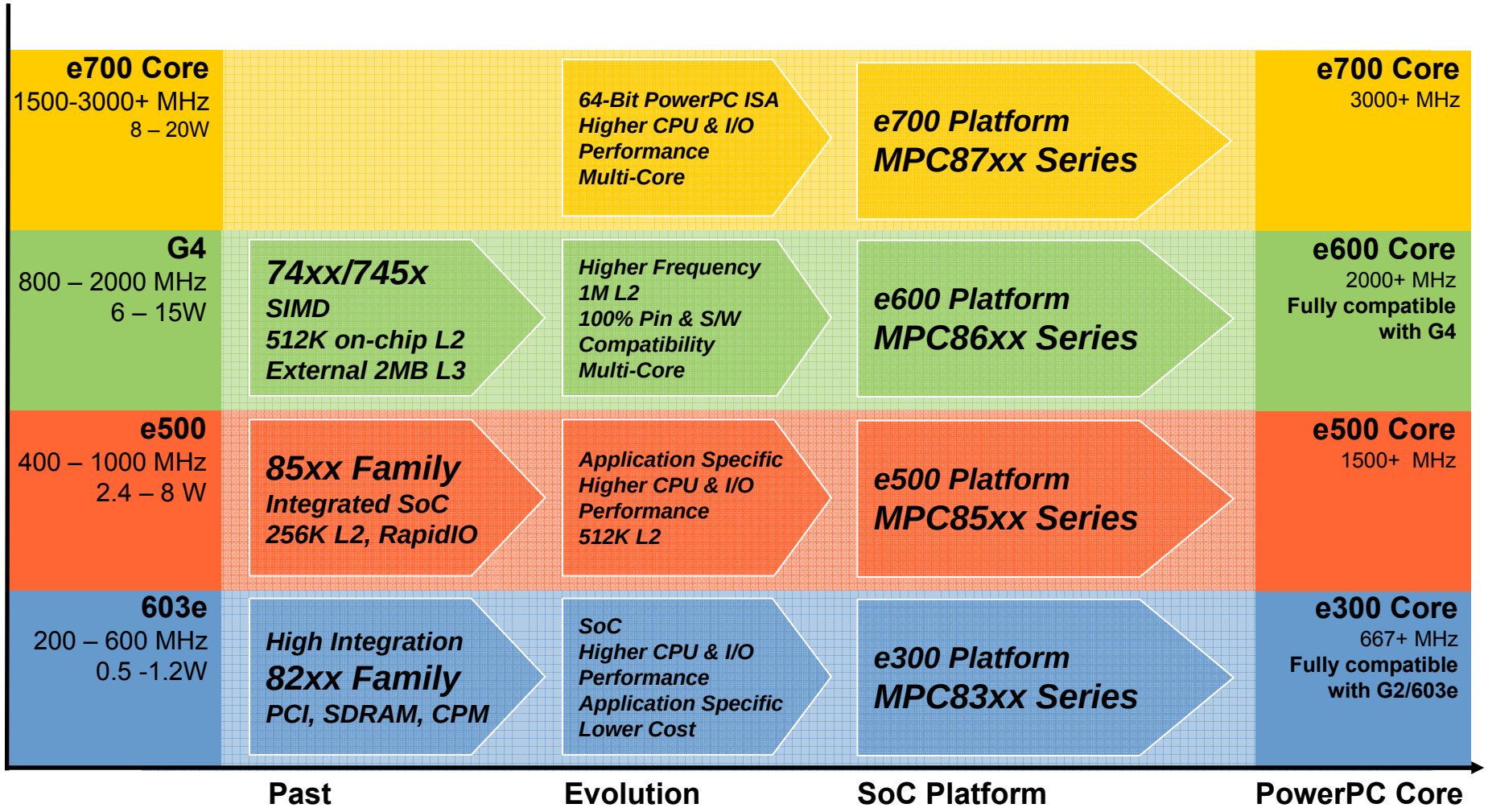
"On the basis of overall performance, efficiency, power consumption, and integration, Motorola's MPC8560 clearly wins the contest. As companies resume investing in communications equipment, Motorola should have no trouble finding good homes for this product."

Markus Levy
MicroDesign Resources

We have expanded the ***e500 Platform's***
flexible ***SoC Methodology***
across our entire PowerPC portfolio

Common SoC Platforms
that enable us to
speed Time-to-Market
and continue to meet customers'
performance *and* ***price*** *requirements.*

‘e’ is for Evolution to SoC
Highly Integrated PowerPC Based SoC Platforms



‘e’ is for Embedded
Performance, Connectivity & Integration

Scalable Performance

e300 Core | e500 Core | e600 Core | e700 Core

Scalable Connectivity

Interconnect

Host Peripheral Bus:
- PCI, PCI-X
- PCI-Express
- PCMCIA
- 60x, MPX
- Local Bus

System Fabric:
- RapidIO
- SERDES

General Peripherals:
- USB High/Full/Low speed
- USB Full/Low Speed
- I^2C, DUART

Networking:
- UTOPIA/POS PHY
- GMII, MII, RGMII, TBI etc.
- XAUI

Network Acceleration

Networking Protocols:
- Ethernet (10/100/1000)
- Serial (Tx/Rx)
- HDLC
- T1/E1/T3/E3 (TDM)
- ATM (AAL0,1,2,5, IMA)
- IP (ML/MC-PPP, PPPmux)
- BPON

Security:
- Encryption
- Authentication
- Public Key
- RNG
- DES/3DES/SHA1

Scalable Integration

Integration Structures:
- Copper Line
- Magenta/SkyBlue Line
- OCeaN Integrated Fabric
- Coherent System Bus

System Integration:
- Bus Controllers
- Timers
- DMA
- Arbiters
- Bridges
- Interrupt Controllers
- GPIO

Mixed Signal:
- PLLs/DLLs
- D/A, A/D
- Clock Data Recovery
- TIA, LDD

Memory Controllers:
- DDR SDRAM
- DDRII SDRAM
- SDRAM
- Flash, EPROM
- SRAM, DRAM

Future PQ

86xx Integrated Platform

PQ III (90nm)

PQ III

PQ II Pro

PQ II

Scalable Compatible Solutions

‘e’-based SoC Platform Processors
Available Today for Your Designs

e300

PowerQUICC II Pro

MPC8343E
MPC8347E
MPC8349E

MPC8358E
MPC8360E

e500

PowerQUICC III

MPC8540
MPC8560

MPC8541E
MPC8555E

MPC8543E
MPC8545E
MPC8547E
MPC8548E

e600

Integrated G4

MPC8641
MPC8641D

- **Integrated PowerPC Host Processors**
- **Integrated PowerPC Communications Processors** (Includes CPM or new QE)

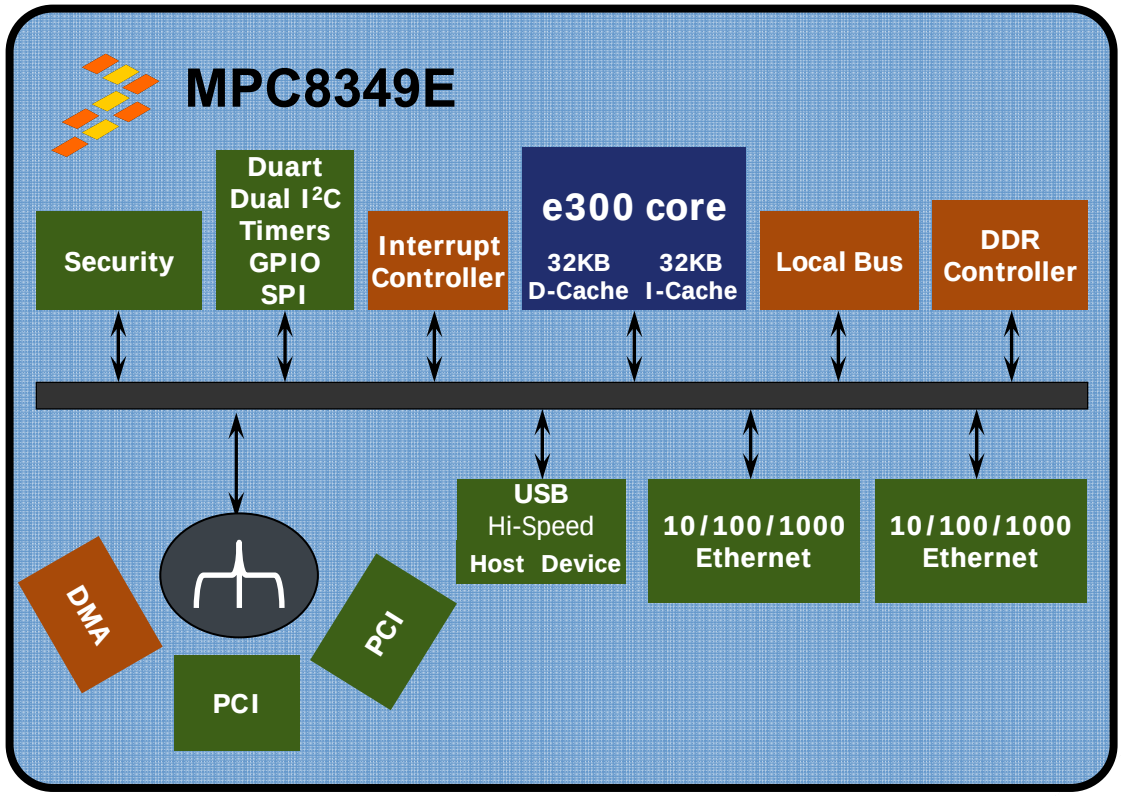
e300 SoC Platform
Focusing on the Low-End to Mid-Range

- e300 Platform Goals
  - Extend the PowerQUICC I and PowerQUICC II Product Families
  - Low-end Platform based on SoC Design Methodology
  - Focus on Low-Cost & Power-Sensitive applications

- Provides new high-performance functionality
  - DDR SDRAM
  - Hi-Speed USB
  - 10/100/1000 Ethernet
  - Dual PCI capability
  - QUICC Engine with enhanced communications functions

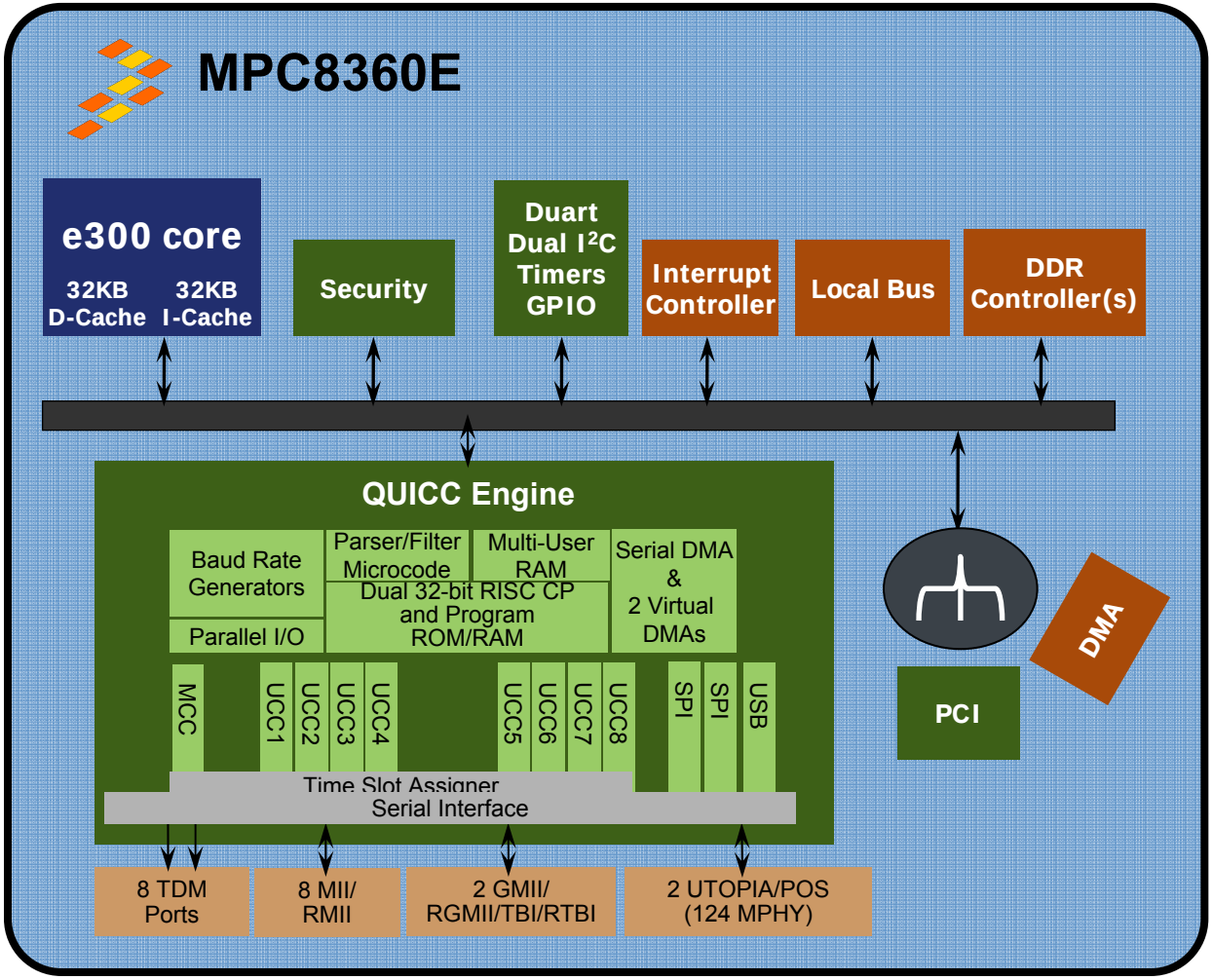
‘e’nside the e300 SoC Platform
MPC8349E Family – PowerQUICC II Pro

- **Features**
  - Integrated e300 core processor
    - > 266-667MHz
    - > 32K I/D cache
  - DDR Memory Controller
    - > 1 x 32/64-bit , 266/333MHz
  - Two 10/100/1000 Ethernet MACs
  - Integrated 2x32-bit or 1x64-bit PCI
    - > Up to 66 MHz PCI 2.2, PCI Arbiter
    - > Master & Agent mode support
  - Local Bus
  - Integrated Security
  - Two Hi-Speed USB ports
    - > 1 port Host, Device, or On-The-Go
    - > 1 port Host
  - Multi-channel DMA controller
  - DUART, Dual I²C, Interrupt, GPIO, SPI
- **Technology**
  - 0.13µm, 1.2V core, 3.3V I/O
  - 672 TBGA – 35x35 mm, 1mm pitch



‘e’nside the e300 SoC Platform
MPC8360E Family – PowerQUICC II Pro

- **Features**
  - Integrated e300 core processor
    - > 266-667MHz
    - > 32K I/D cache
  - DDR Memory Controller
    - > 1 x 32/64b or 2 x 32b, 266/333MHz
  - Integrated 1x32-bit PCI
    - > Up to 66 MHz PCI 2.2, PCI Arbiter
    - > Master & Agent mode support
  - Local Bus
  - Integrated Security
  - QUICC Engine
    - > 2 micro engines (300 - 500 MHz)
    - > 8 UCCs (Two UL2/POS, Two GMII, 8 MII, 4 port L2 switch, 8 TDMs)
    - > MCC (256 HDLC channels)
    - > Dual SPI
    - > USB Low/Full Speed
  - Multi-channel DMA controller
  - DUART, Dual I²C, Interrupt, GPIO
- **Technology**
  - 0.13µm, 1.2V core, 3.3V/2.5V I/O
  - 740 TBGA – 37.5x37.5 mm, 1mm pitch



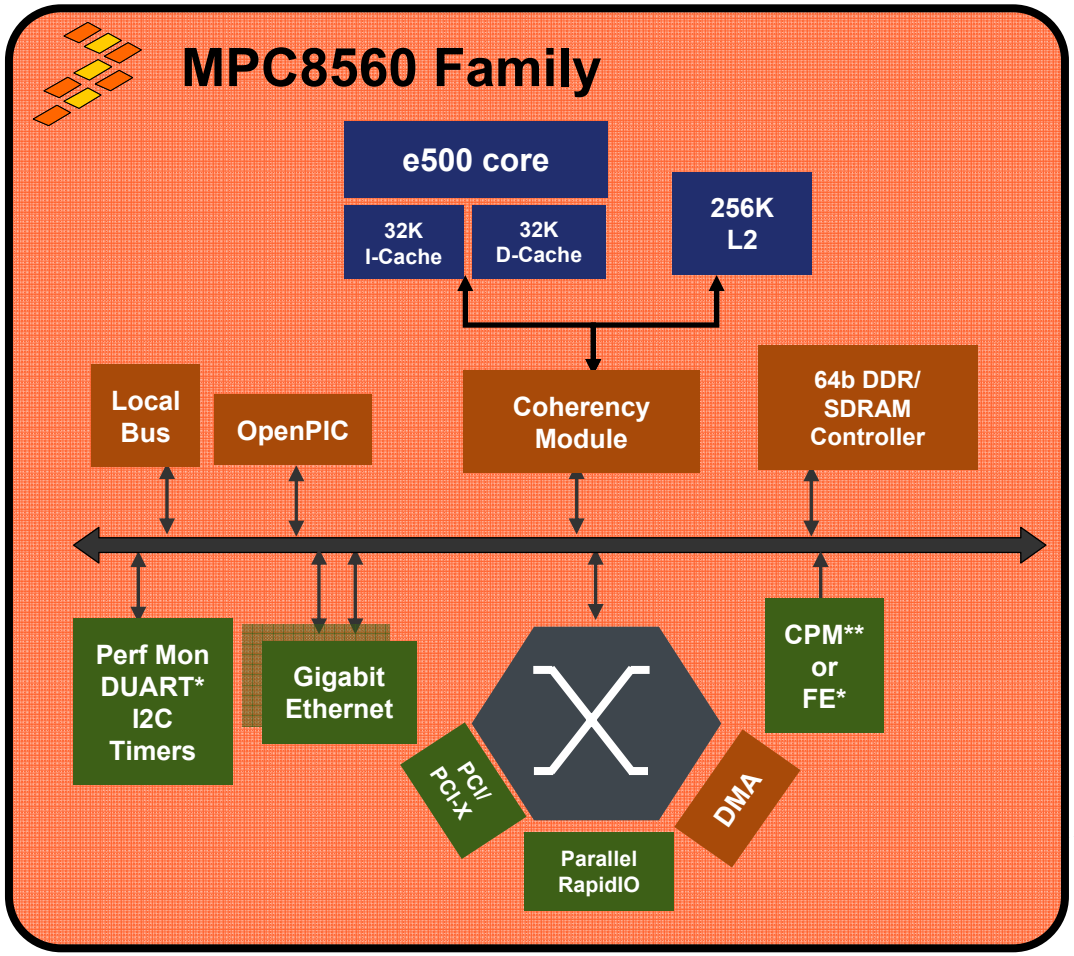
e500 SoC Platform
Focusing on the Mid-Range

- e500 Platform Goals
  - Address a Wide Variety of Market Needs
  - Exceptional Integration, High-Speed Connectivity, and HW Acceleration
  - Book E Architecture enabling Embedded Applications

- Provides Even Further High-Performance Functionality
  - 256KB-512KB L2 cache
  - DDR/DDR2/FCRAM1/FCRAM2 memory support
  - Enhanced Gigabit Ethernet controllers
  - RapidIO technology
  - PCI Express, PCI/PCI-X
  - Security enhancements
  - XOR acceleration
  - Communications Processor Module (CPM)

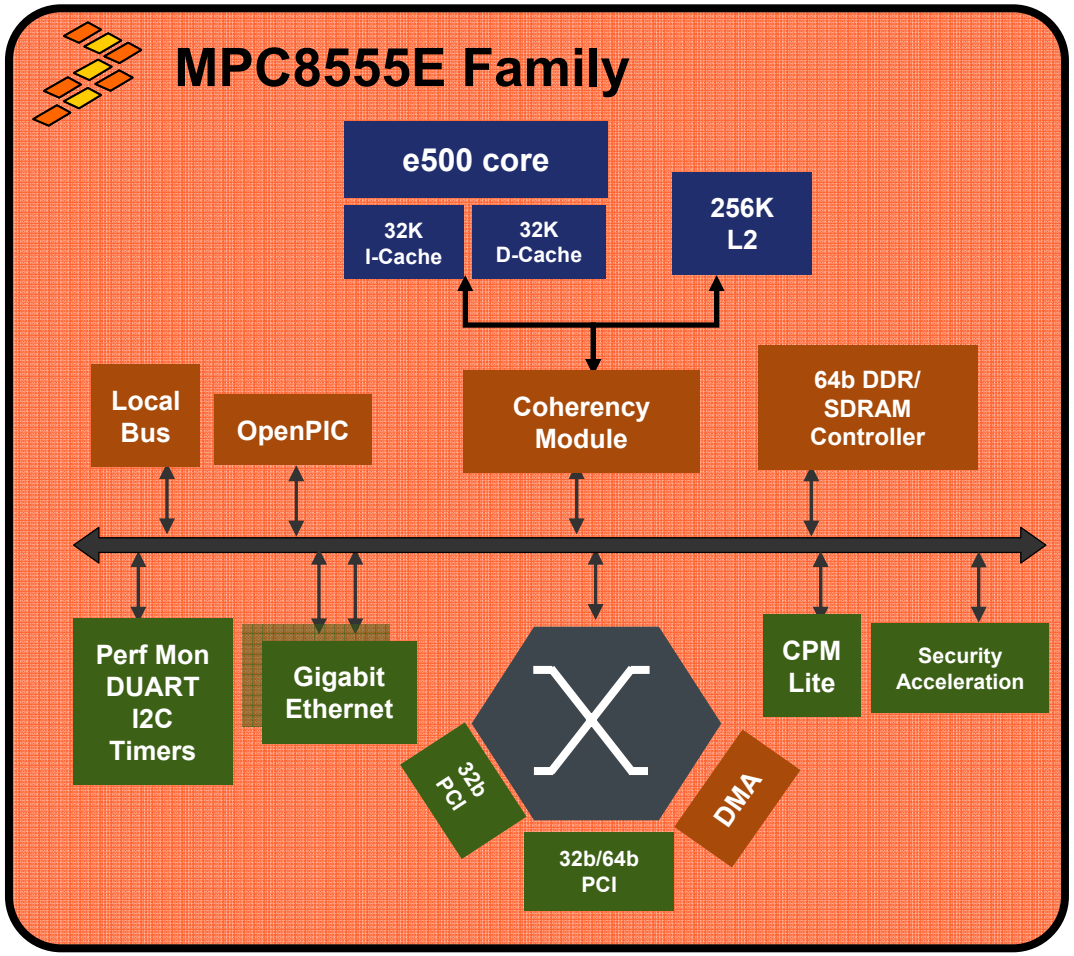
‘e’nside the e500 SoC Platform
MPC8560 Family – PowerQUICC III

- **Features**
  - Integrated e500 core processor
    - > 667-1000MHz
    - > 32K I/D cache
    - > 256KB L2 Cache
  - Features
    - > Up to 333MHz 64b DDR SDRAM
    - > 2x 10/100/1000 Ethernet Controllers
    - > 1x 10/100 Ethernet Controller (8540 only)*
    - > 32-/64-bit PCI/PCI-X
    - > 500MHz 8b RapidIO
    - > DUART(8540 only)*, I2C, Interrupt, GPIO
    - > Local Bus
    - > Multi-Channel DMA Controller
  - CPM (8560 only)**
    - > Specialized RISC 333 MHz
    - > 3 FCCs, 4 SCCs, 2 SMCs, 2 MCCs, SPI, I2C
    - > 8/16b UTOPIA L2 for DSL/OC-3
    - > 8 TDMs – Up to 256 HDLC Channels
    - > ATM TC Layer
- **Technology**
  - 0.13µm, 1.2V core, 3.3V/2.5V I/O
  - 783 FC-PBGA Package (Flip Chip on PBGA)



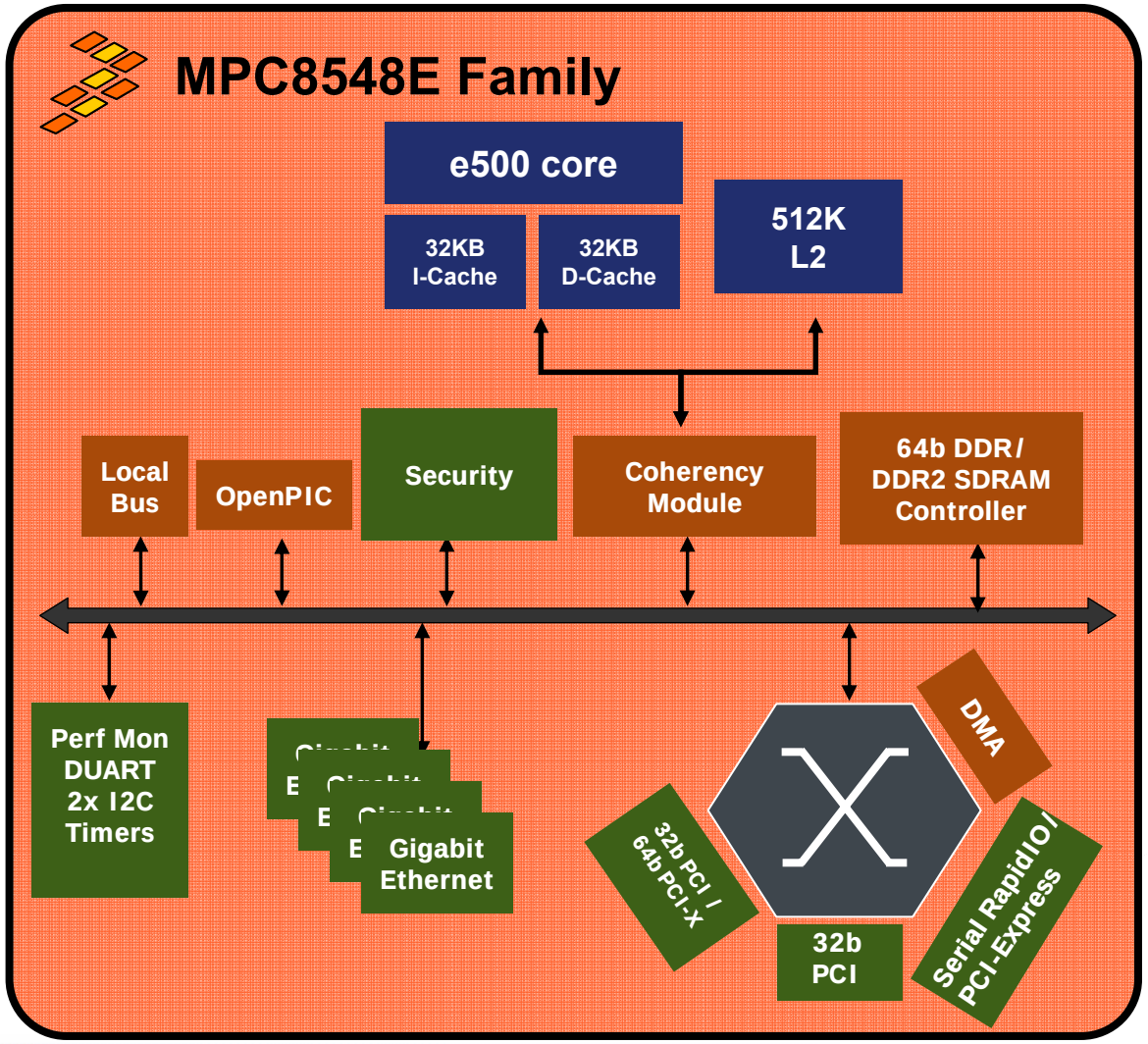
‘e’nside the e500 SoC Platform
MPC8555E Family – PowerQUICC III

- **Features**
  - Integrated e500 core processor
    - > 533-1000MHz
    - > 32K I/D cache
    - > 256KB L2 Cache
  - Features
    - > Up to 333MHz 64b DDR SDRAM
    - > 2x 10/100/1000 Ethernet Controllers
    - > 2x 32b or 1x 64b PCI
    - > DUART, I2C, Interrupt, GPIO
    - > Integrated Security
    - > Locus Bus
    - > Multi-Channel DMA Controller
  - CPM-Lite
    - > Specialized RISC 333 MHz
    - > 2 FCCs, 3 SCCs*, USB*, 2 SMCs*, SPI, I2C
    - > 8b UTOPIA L2 for DSL*
    - > 3 TDMs – Up to 64 HDLC Channels*
- **Technology**
  - 0.13µm, 1.2V core, 3.3V/2.5V I/O
  - 783 FC-PBGA Package (Flip Chip on PBGA)



‘e’nside the e500 SoC Platform
MPC8548E Family – PowerQUICC III (90nm)

- **Features**
  - Integrated e500 core processor
    - > Up to 1.5GHz
    - > 32K I/D cache
    - > 256-512KB L2 Cache
    - > 36bit physical addressing
  - Features
    - > 64b DDR/DDR2/FCRAM1/FCRAM2 SDRAM
      - – Up to 667MHz data rate with ECC
    - > Up to 4x 10/100/1000 Enhanced Ethernet Controllers
      - – Checksum Offload, QoS, Header Parsing, Packet Classification, and 8/16b FIFO mode (up to 3.2Gbps)
    - > 2x 32b-PCI or 1x 64b PCI(X)
    - > DUART, Dual I2C, Interrupt, GPIO
    - > Integrated Security
    - > Local Bus
    - > Multi-Channel DMA Controller
    - > High-Speed Interfaces:
      - – x4,x1 Serial RapidIO (20Gbps)
      - – Or x8,x4,x2,x1 PCI-Express (32Gbps)
      - – Or x4 Serial RapidIO and x4 PCI-Express (36Gbps)
- **Technology**
  - 90nm, 1.1V core, 3.3V/2.5V or 1.8V I/O
  - 783 FC-PBGA Package



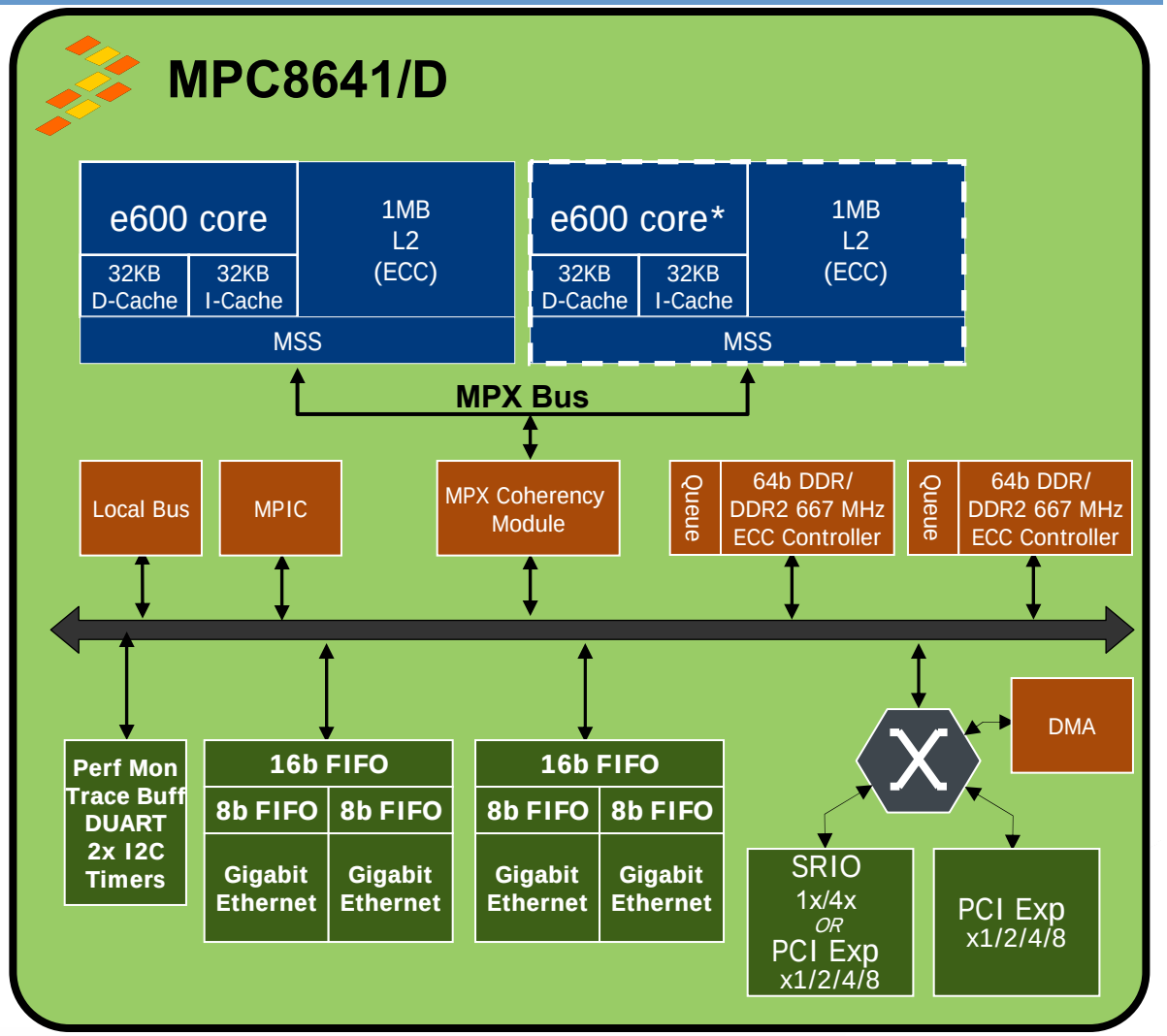
e600 SoC Platform
Focusing on High Performance

- e600 Platform Goals
  - Provide the Highest Compute Density/Performance for an Integrated Device in the Industry
    - > First Multi-PowerPC® Core Enabled Product Family from Freescale
    - > Achieve Higher Performance without Power Increases with AltiVec™
  - Low Power to enable the High Performance Embedded Market
  - Share Available SoC IP with e300 and e500 Platforms maximizing SW Reuse

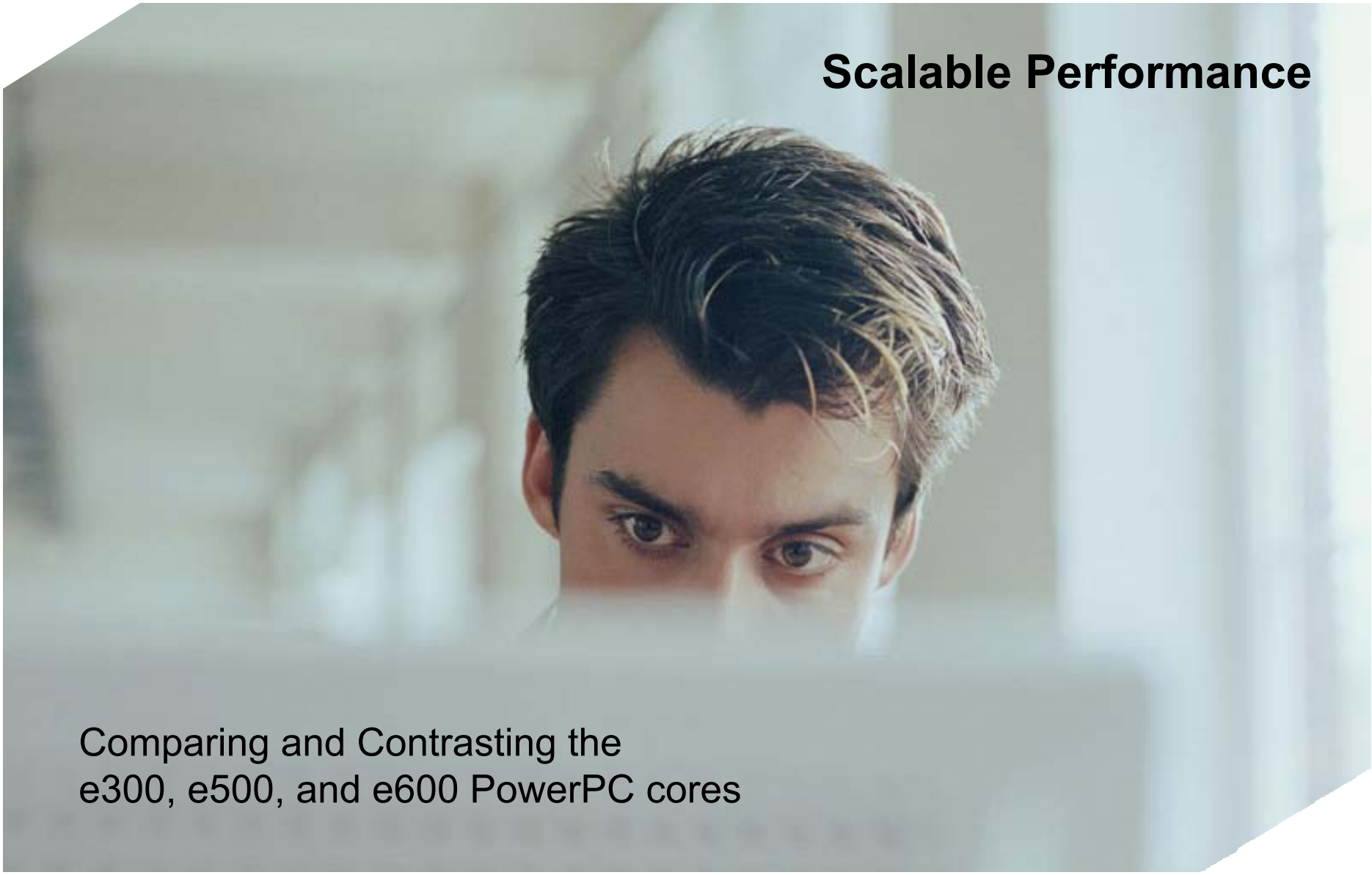
- Provides Highest-Performance
  - 1MB Backside L2 cache per e600 Core
  - Dual e600 PowerPC Cores
  - Dual 64b DDR/DDR2/FCRAM1/FCRAM2 memory support
  - Enhanced Gigabit Ethernet controllers
  - Serial RapidIO technology
  - Dual PCI Express

‘e’nside the e600 SoC Platform
MPC8641 Family – High Performance Single & Dual Core*

- **Features**
  - Integrated Single or Dual e600 Cores
    - > 1.2-1.8GHz
    - > 32K I/D cache
    - > 1MB Backside L2 Cache w/ECC per Core
    - > 36bit physical addressing
  - Features
    - > Dual 64b DDR/DDR2/FCRAM1/FCRAM2 SDRAM Controllers
      - – Up to 667MHz data rate with ECC
    - > Up to 4x 10/100/1000 Enhanced Ethernet Controllers
      - – Checksum Offload, QoS, Header Parsing, Packet Classification, and 8/16b FIFO mode
    - > DUART, Dual I2C, MP Interrupt, GPIO
    - > Integrated Security
    - > Local Bus
    - > Multi-Channel DMA Controller
    - > High-Speed Interfaces:
      - – x4,x1 Serial RapidIO (20Gbps) and x8,x4,x2,x1 PCI-Express (32Gbps)
      - – Or two x8/x4/x2/x1 PCI-Express (64Gbps)
- **Technology**
  - 90nm, 1.0-1.1V core, 3.3V/2.5V or 1.8V I/O
  - 783 FC-PBGA Package



Scalable Performance



Comparing and Contrasting the
e300, e500, and e600 PowerPC cores

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“Don't lower your expectations to meet your performance. Raise your level of performance to meet your expectations.”

Ralph Marston
The Daily Motivator

‘e’ – The Core of our SoC Platforms
Core Comparisons

	e300	e500	e600
Frequency (MHz)	266 – 667MHz	533MHz – 1.5GHz	1.2 – 1.8GHz
User Mode	PowerPC Classic	PowerPC Classic	PowerPC Classic
Supervisory	Classic	Book E	Classic
Instruction Issue	Dual-Issue	Dual-Issue	3 + 1 branch
Pipeline Stages	4	7	7
Vector Processing	–	64b SPE APU (uses GPRs)	128b Altivec (dedicated resources)
Block translation	8/8 I/DBAT, 128kB–256MB	16 SuperPages 4kB – 4GB	8/8 I/DBAT 128kB – 4GB
DMIPS/MHz	1.9	1.9 2.3 with SPE	2.3 no vectorization 2.8 with Altivec

‘e’ – The Core of our SoC Platforms
How is Book E different from Classic PowerPC?

- User mode is binary compatible across e300, e500, e600
  - Applies to the vast majority of code
  - Recompile improves performance
  - Some instructions have slightly stronger semantics (eieio→mbar, sync→msync) although the semantics should still ensure proper operation
  - Standard Floating point and string instructions are not implemented

- Supervisor mode is different – confined to kernel
  - MMU: BATs vs SuperPages
    - > Some TLB manipulation instructions have different semantics because MMU architecture is different
  - Exceptions: critical interrupt, real mode emulation
  - Reset vector at a different location
  - Debug: performance monitors

‘e’ – The Core of our SoC Platforms
MMU Architecture and Compatibility

- The e300 and e600’s block address translation (BAT) registers and segment registers (SRs) are not implemented in the e500 core.
  - Instructions, registers, and associated interrupts are removed
- e500 Platform Compatibility Methods
  - If MMU translations are static in a system (no dynamic mapping), equivalent translations can be set up at boot time.
  - Real mode can be emulated by creating a global TLB entry for address space 0 that maps all physical memory 1 to 1.
  - PID assignments could be used to replace segment register configuration for defining access to virtual address spaces.
  - New MMU Assist (MAS) registers are used to set up TLBs.
  - New TLB instructions need to be used.

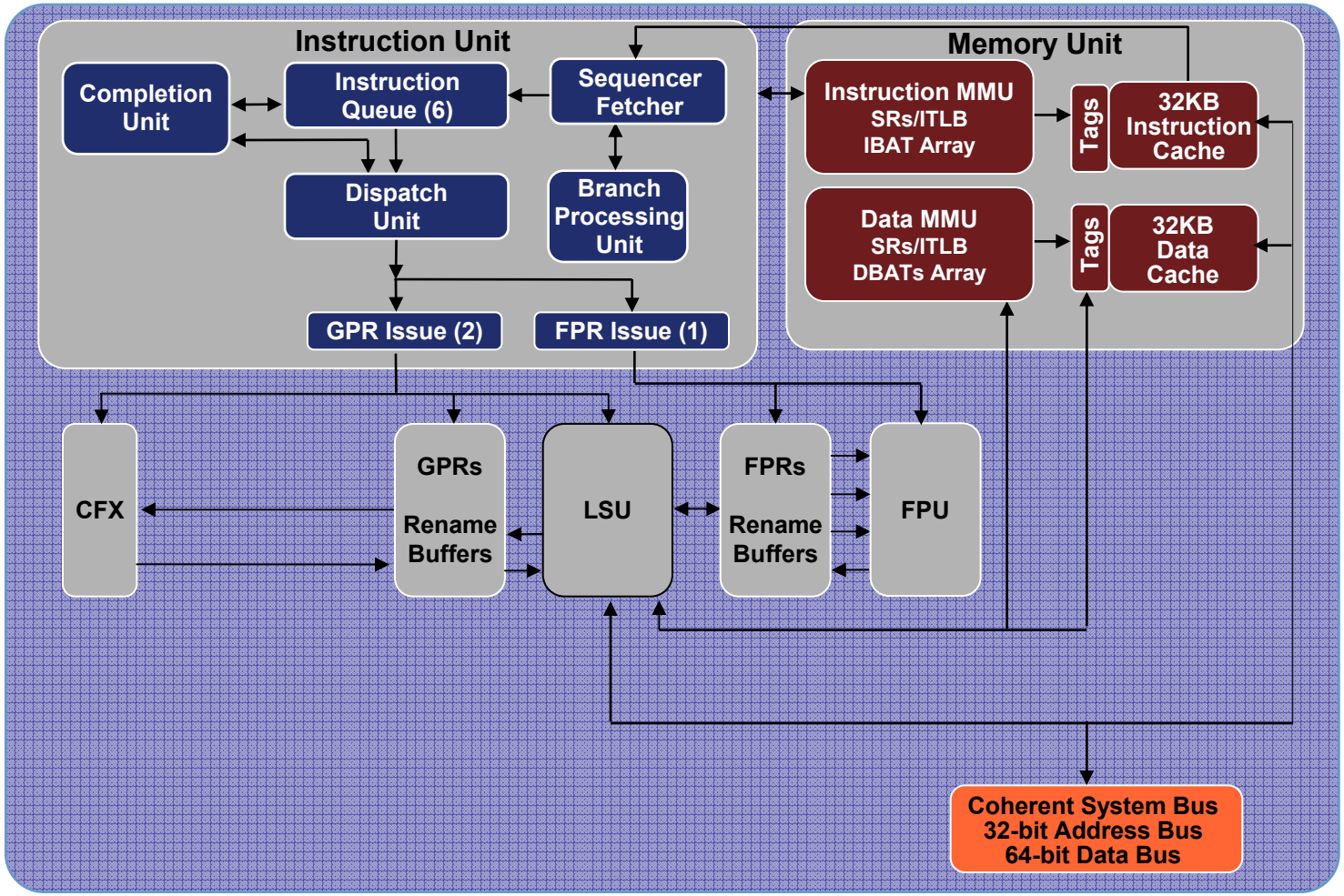
‘e’ – The Core of our SoC Platforms
Cache

	e300	e500	e600
L1 I/D-Cache:	32K/32K	32K/32K	32K/32K
L1/L2 Set Associativity:	8-way	8-way	8-way
L2 Type/Size	---	Unified Front Side	Unified Back Side
L1/L2 Error Detection	L1 Tag Parity	L1 Tag Parity L2 Tag Parity, ECC	L1 Tag Parity L2 Tag/Data Parity, ECC
Lockability	L1 Lockable per way (1 ... 7)	L1/L2 lockable per cache line	L1 Lockable per way (1 ... 7)
L2 Stashing	---	Yes	No
Mappable as SRAM	---	Yes	No
L2 Hit Latency	---	18 to 22 core clocks	11 or 12 core clocks

The Advantages of the Platform Caches

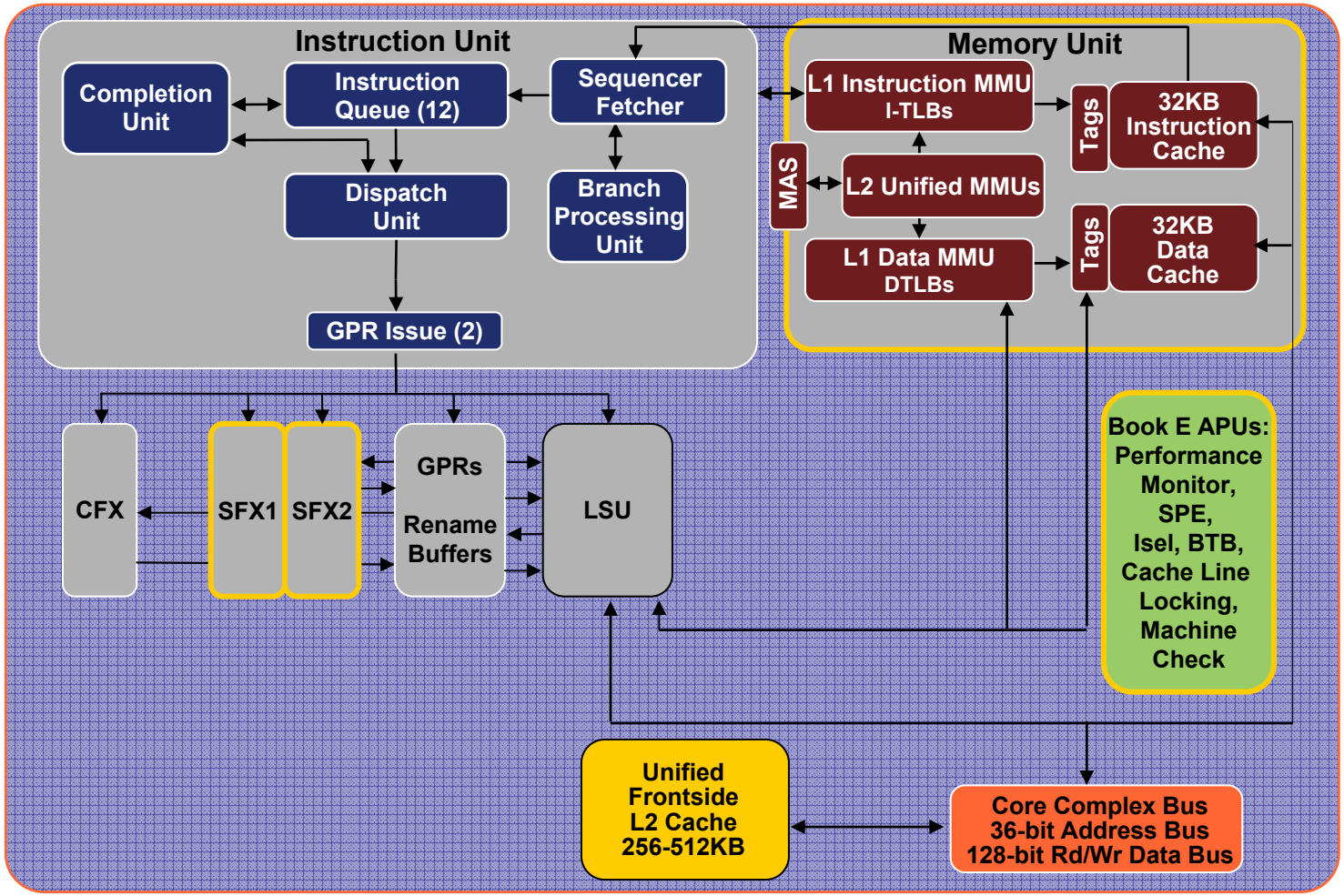
- e300 Platform includes only L1 I/D Caches
  - Provides a cost advantage for systems that require lower computing intensive tasks such as IP forwarding and protocol interworking.
- e500 Platform provides an additional 256k to 512k of Front Side L2 Cache
  - Provides for lower latency accesses to a data/instructions resulting in greater packet performance under heavy services on packet flows.
  - Allows for stashing of packet headers directly to memory.
- e600 Platform provides up to 1MB of Back Side L2 Cache per Core
  - For highly compute intensive applications, “Cache is King”.
  - Backside Cache means lower latency to data/instructions since the transaction does not have to transverse the Front Side bus.

e300 Core Architecture



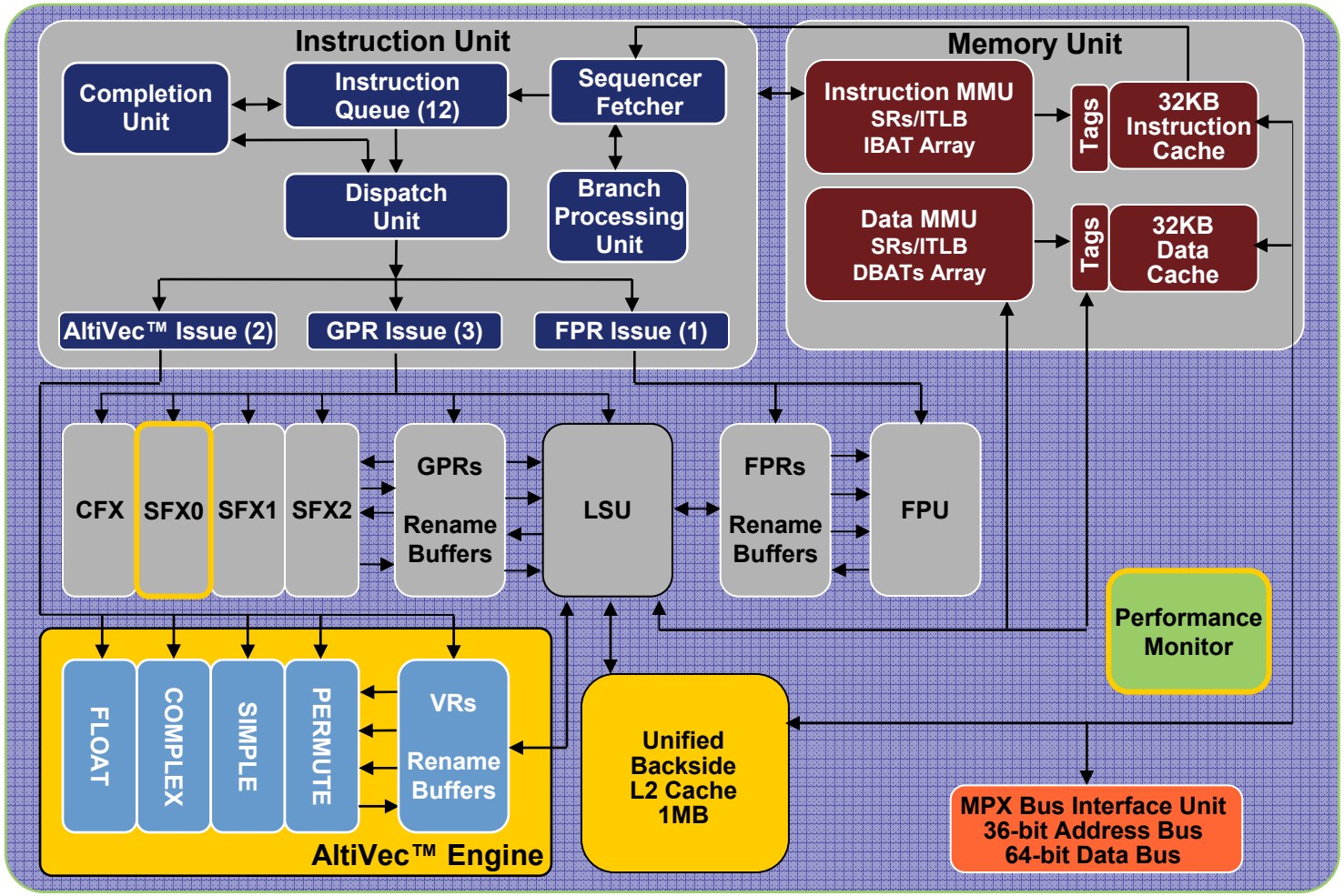
- 266-667MHz
- L1: 32KB, 8 way set associative, Parity
- Cache way locking supported
- MEI cache coherence and intervention
- Peak IPC 2 Instructions plus 1 branch
- Out of Order Execution
- FPU - 64-bit IEEE754-1985 single/double prec
- 8/8 I/D BATs
- 128-entry 4K pages
- 32-bit Physical Address

e500 Core Architecture



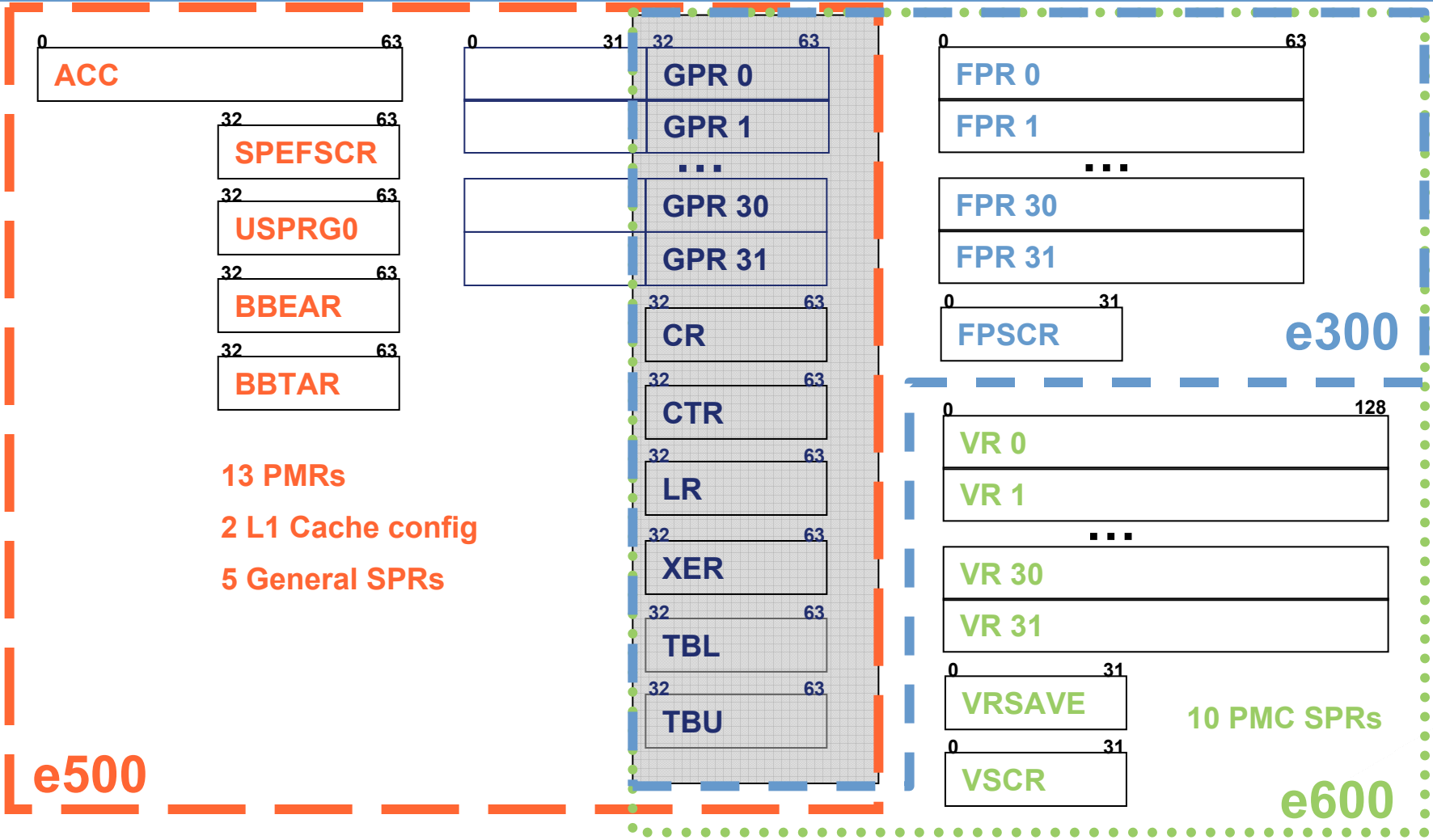
- 533MHz-1.5GHz
- L1: 32KB, 8 way set associative, Parity
- L2: Fronside 256-512KB, 8 way set associated, ECC
- Cache line locking supported
- MESI cache coherence and intervention
- Peak IPC 2 Instructions plus 1 branch
- Out of Order Execution
- Multiple Book E APUs
- 16 TLB SuperPages
- 512-entry 4K Pages
- 36-bit Physical Address

e600 Core Architecture

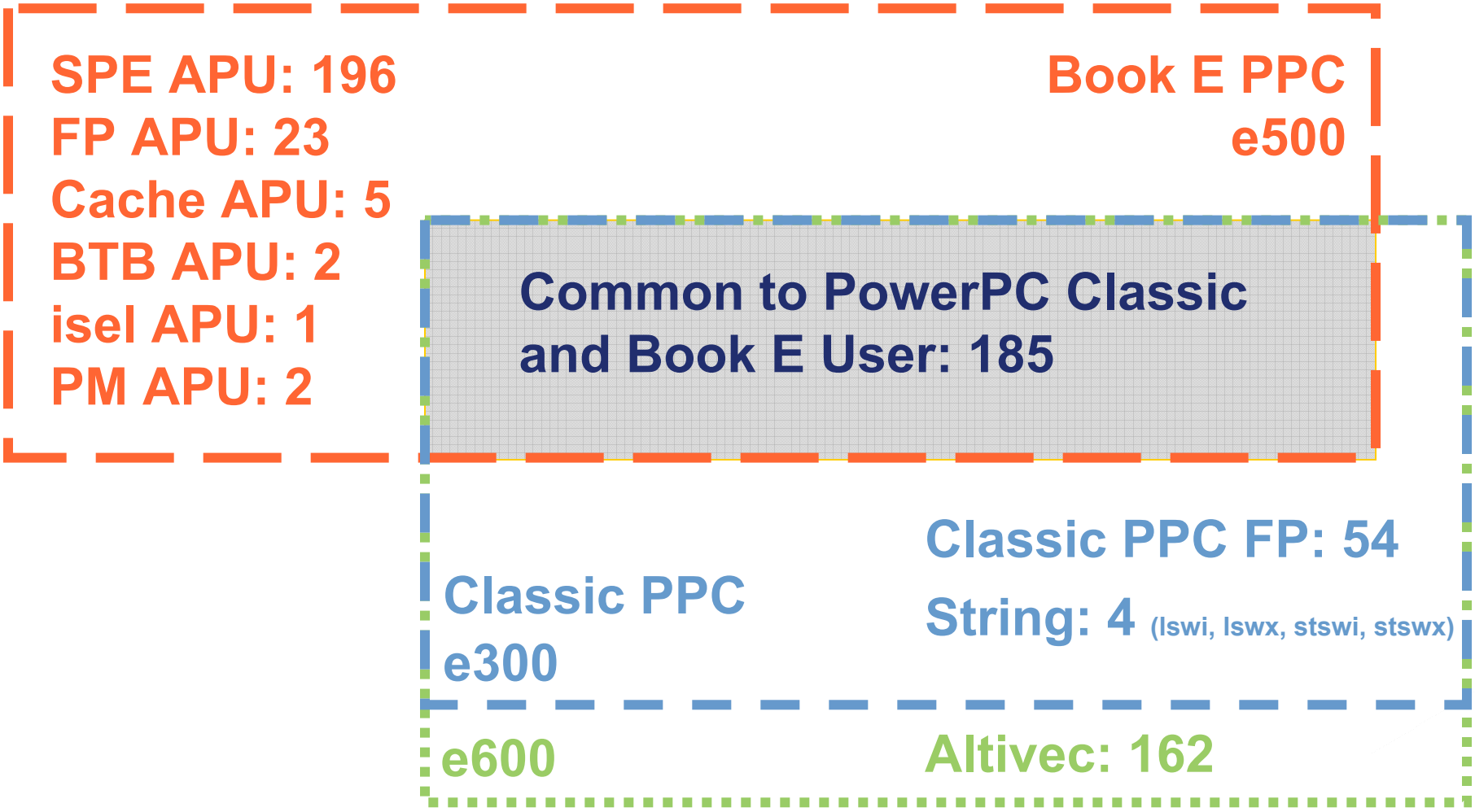


- 1.2GHz-1.8GHz
- L1: 32KB, 8 way set associative, Parity
- L2: Backside 1MB, 8 way set associated, ECC
- Cache line locking supported
- MESI cache coherence and intervention
- Full SMP Support
- Peak IPC 3 Instructions plus 1 branch
- Out of Order Execution
- AltiVec™ SIMD Engine
- 16 TLB SuperPages
- 256-entry 4K Pages
- 36-bit Physical Address

e300↔e500↔e600
Common Subset PowerPC User Registers



e300↔e500↔e600
Common Subset PowerPC Instructions



e300↔e500↔e600
Considerations for Cross-Platform Code Compatibility

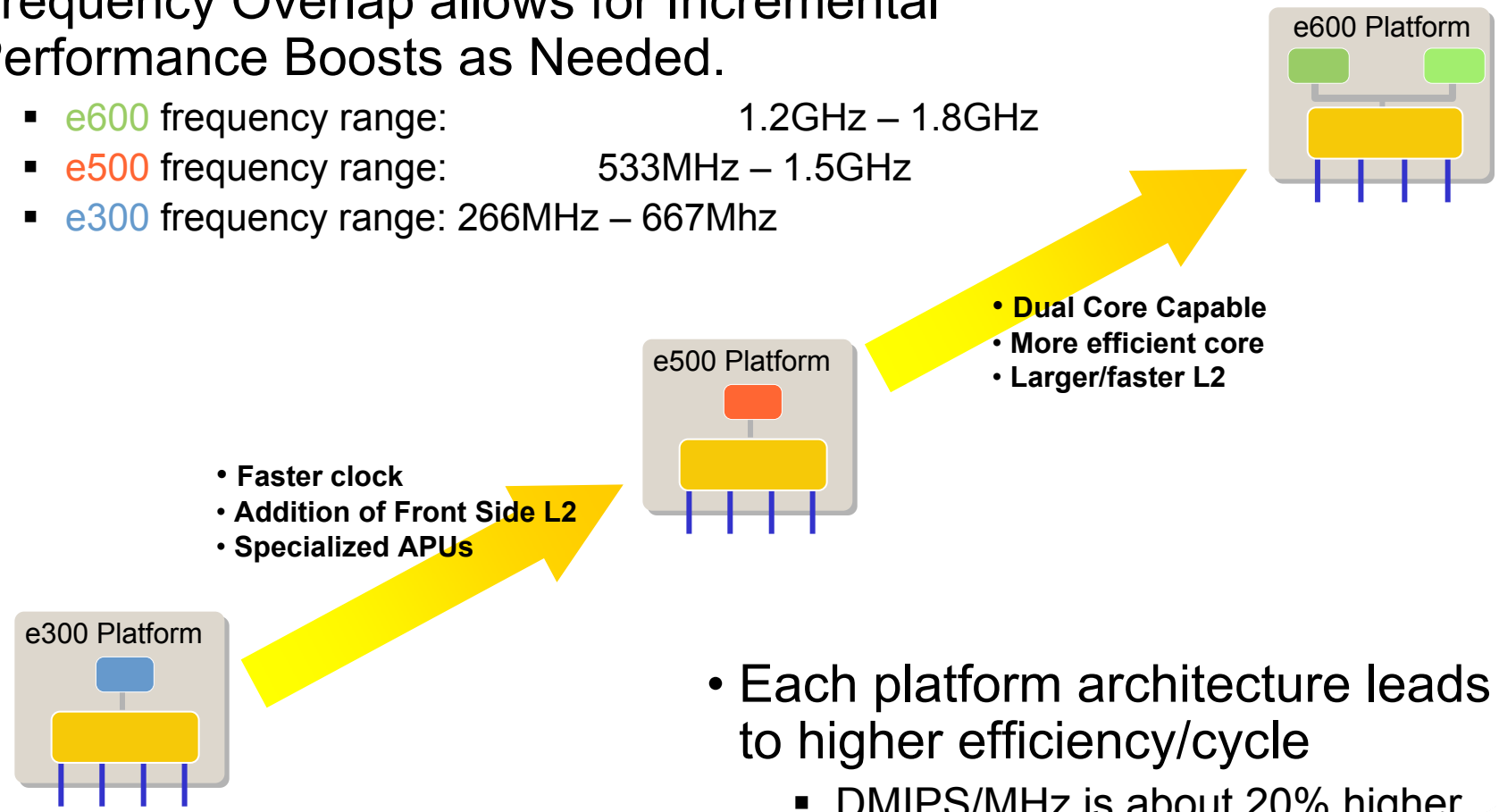
- Applications should only use features in the intersection of the user register space and instruction sets of e500 and e300/e600 Platforms
- Avoid use of:
  - Floating point (single or double precision)
  - String operations
  - Specialized Instructions
    - > Book E APUs (isel, SPE, etc.) or AltiVec

e300↔e500↔e600
Considerations for Optimized Platform Specific Code

- For optimized (pre-compiled) code-compatibility, do not ‘hand assemble’
- Recompile and optimize for each specific microarchitecture
  - e300, e500, e600-only binaries
  - For example, use options for e500: *-mcpu=8540 -mabi=spe*
- For the most optimized performance
  - Utilize special features that analyze and implement algorithms more efficiently (AltiVec, isel, FP, SPE, BTB, CL, PM)
    - > Automatic via compiler (isel, SP FP)
    - > Explicitly by using the AltiVec or SPE programming interface (PIM)
    - > Tuned assembly code (will not allow cross platform compatibility)
    - > Specialized libraries (libmotovec or libmoto_e500)
    - > Optimizing branch and cache behavior

e300↔e500↔e600
Relative Optimized Performance

- Frequency Overlap allows for Incremental Performance Boosts as Needed.
  - e600 frequency range: 1.2GHz – 1.8GHz
  - e500 frequency range: 533MHz – 1.5GHz
  - e300 frequency range: 266MHz – 667Mhz



- Each platform architecture leads to higher efficiency/cycle
  - DMIPS/MHz is about 20% higher between platforms

Scalable Connectivity

Comparing and Contrasting the MPC83xx, MPC85xx, MPC86xx Interconnect and Network Acceleration

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Scalable Connectivity
The Right Interface with the Right Performance

- Scalable System Connectivity to Match Platform Performance
  - HiP7 MPC83xx & MPC85xx: PCI, USB, TSECs, QE/CPM
  - HiP8 MPC85xx & MPC86xx: PCI-Express, Serial RapidIO, eTSECs
- Scalable Protocol Support to Meet Throughput Expectations
  - HiP7 MPC83xx and MPC85xx supply various IP and WAN options
    - > Complete Integrated Solution for WAN+LAN
    - > Flexible QE/CPM for Multi-Protocol and Interworking Support
  - HiP8 MPC8548E and MPC8641x Target IP Applications
    - > Focus on Line-Rate Capability through the use of TCP/IP Offload, QoS, FIFO mode, VLAN insertion/extraction.
    - > WAN Interfaces would normally be supported via Line Card Interfaces
- Standard Low Speed Interfaces across all Platforms

Scalable Connectivity
Interface and Peripheral Summary

	8349	8548	8641
Serial IO:	None	X8 PCI Express OR (x4 PCI Express + x4 SRIO)	X8 PCI Express AND (x8 PCI Express OR x4 SRIO)
PCI	2x 32b PCI OR 64b PCI	2x 32b PCI OR 64b PCI-X	With low cost bridge chip
GE /FIFO	2x GE	4x GE OR (16b FIFO + 8b FIFO)	4x GE OR (16b FIFO + 16b FIFO)
IP/Enet Features	---	TOE/QoS/Stashing	TOE/QoS
Security	Hardware Block	Hardware Block	SW with AltiVec
USB	High Speed (Dual)	---	---
Low-speed IO	DUART, 2x I2C	DUART, 2x I2C	DUART, 2x I2C

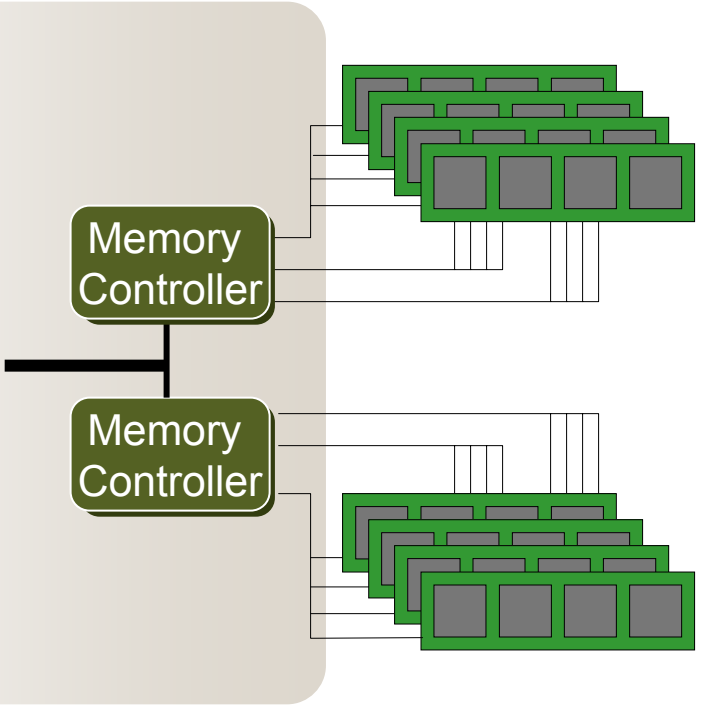
Scalable Integration

Comparing and Contrasting the MPC83xx, MPC85xx, MPC86xx
Pulling it all Together

freescale semiconductor

Scalable Integration
Sustaining Expected Packet Performance

- Scalable Memory Interfaces to Sustain Packet Performance
  - MPC83xx supplies a single 333MHz 32/64b DDR I Memory Controller
    - > Note: MPC8360E can support either single 32/64b or dual 32b DDR I
  - MPC85xx supplies a single 667MHz 64b DDR II Memory Controller
  - MPC86xx supplies dual 667MHz 64b DDR II Memory Controllers



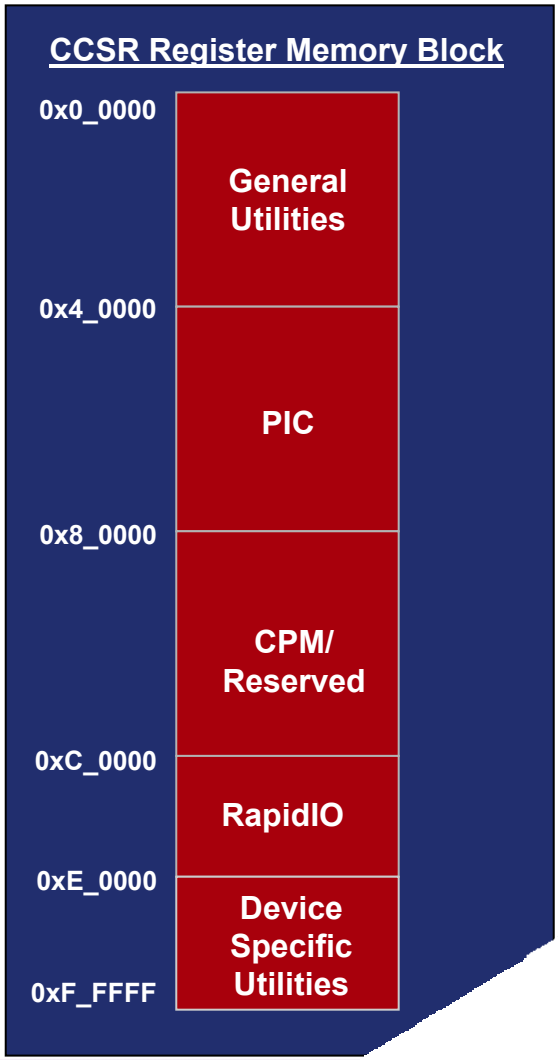
Scalable System Performance

- Memory Controllers Peak Bandwidth
  - 8349: 64b @ 333MHz = 2.7GB/s
  - 8548: 64b @ 667MHz = 5.3GB/s
  - 8641D: dual 64b @ 667MHz = 10.6GB/s
- System Bus Bandwidth
  - 8349: 64b CSB @ 333MHz = 2.7 GB/s,
  - 8548: 64b CCB read at 667MHz = 5.3GB/s, simultaneous with 128b write bus at 667MHz: 10.6GB/s (also for L2 rd/wr)
  - 8641D: 64b MPX @ 667MHz: 5.3GB/s

> Note: All Bandwidth Numbers are provided in GigaBYTES per Second

Software Reuse – How it's Done!
Configuration, Control, & Status Registers (CCSR)

- Software Driver Reuse is Enabled through CCSR.
- The CCSR is a 1MByte memory mapped region that contains all the configuration, control, and status registers for the processor
- All Platforms use the same offsets in the CCSR for a particular IP Block
  - *Example*: DUART Code for the MPC8540 can be reused on both the MPC8349E and MPC8641D since all registers and offsets stay the same.



Scalable Integration
Bus and Controller Summary

	8349	8548	8641
Core Bus	64b CSB	128b CCB	64b MPX
DDR Memory Controller	32/64b DDR I to 333MHz with ECC	64b DDR II to 667MHz with ECC	Dual 64b DDR II to 667MHz with ECC
Maximum DDR Memory Bandwidth	2.7 GB/s	5.3 GB/s	10.6 GB/s
Local Bus	32b to 133MHz	32b to 167MHz	32b to 167MHz
LB Controllers	GPCM/UPM/SDRAM	GPCM/UPM/SDRAM	GPCM/UPM/SDRAM
DMA	4-channel	4-channel	4-channel
Interrupt Controller	PIC	PIC	Multi-Processor Superset of PIC
CCSR-Based	Yes	Yes	Yes

The Power of ‘e’ from Freescale
Meeting Your Low-End, Mid-Range, & High-End Requirements

- e300, e500, & e600 PowerPC cores enable software compatible designs that span the full range of computing requirements

- Freescale's SoC-based standard products provide optimized connectivity and integration allowing the right power-price-performance point for a wide range of applications.
  - I/O models and on-chip system logic are shared across product families allowing you to maximize your software re-use (OS and Drivers)

Platform Specific FTF Sessions
Don’t miss out on these related in-depth presentations

- **e300 Platform**
  - NWL443 Overview of PowerQUICC II Pro MPC8349E Family
  - NAR497 The QUICC Engine™ and the PowerQUICC™ II Pro MPC8360 Family
  - NAR500 System Design and Initialization with the MPC834x PowerQUICC™ II Pro Family
  - NAR526 Hands-On Workshop: MPC8349 Board Hands-On Training and Demonstration

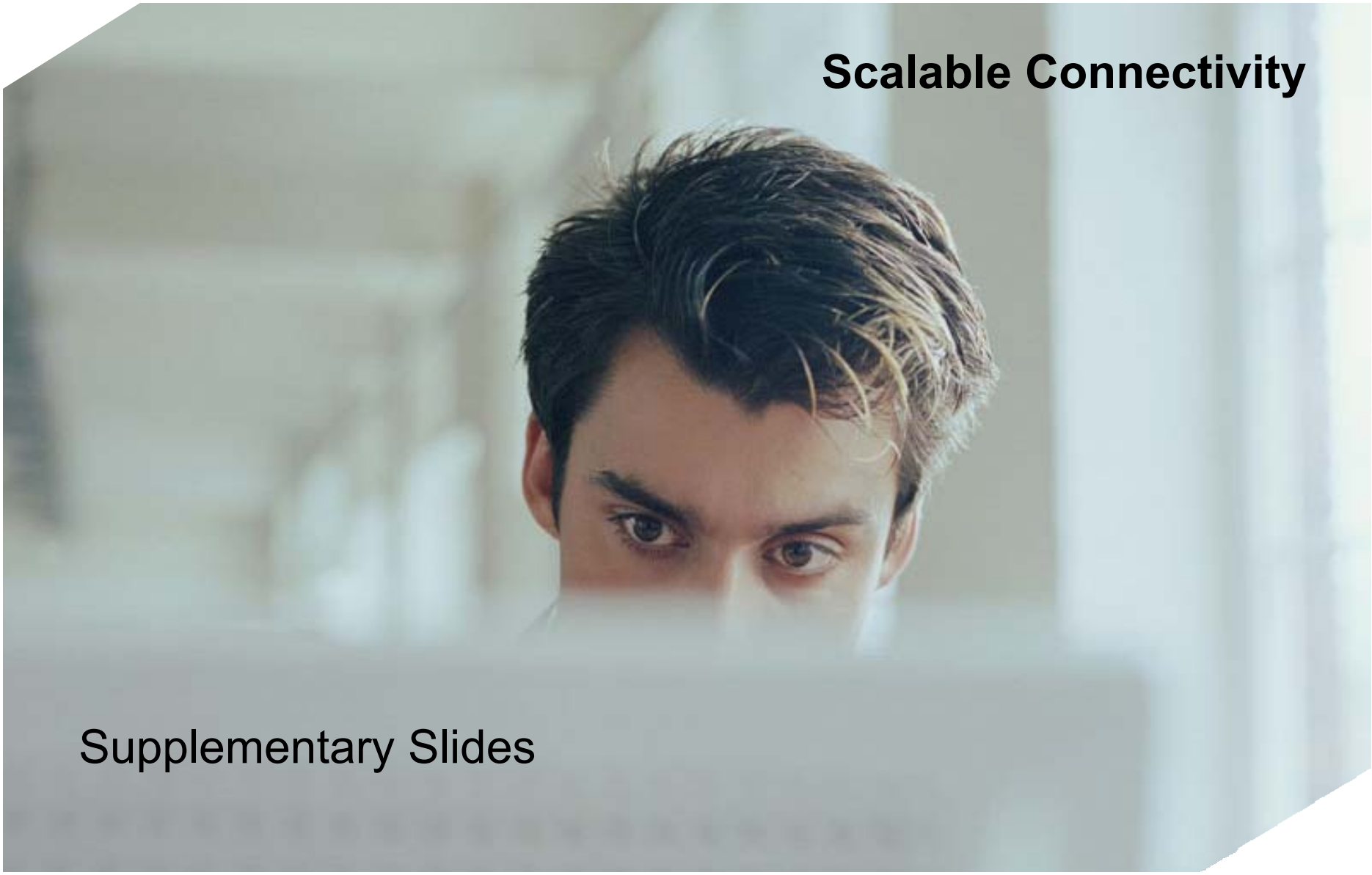
- **e500 Platform**
  - NAR490 Overview of the PowerPC® e500 core on the MPC8548
  - NAR489 MPC8548 Architecture Overview
  - NAR492 Tips and techniques in debugging design using PowerQUICC™ III.
  - NAR479 PowerQUICC™ III: Meeting the Needs of Next-Generation Systems

- **e600 Platform**
  - NAR464 Inside the MPC8641D Dual-Core PowerPC Processor
  - SDT838 Introduction to AltiVec™ Technology—Ten Easy Ways to Vectorize Your Code
  - NEN410 Flexible and Scalable Multi-Layer Switch Design Using the Dual-Core MPC8641D

- **Related Sessions:**
  - NPV427 PowerPC® Architecture Primer
  - NAR405 PowerQUICC™ II Pro and PowerQUICC III: Scalability and Flexibility
  - NAR474 PowerQUICC™ Software Drivers
  - NAR473 Enhanced Triple Speed Etherent Controller Features
  - NAR513 Overview of the PCI Express I/F on the MPC8548 and MPC8641/D
  - NAR457 Pros and Cons of Using RapidIO®, PCI Express, & Gigabit Ethernet for Embedded System Connectivity
  - NHS512 Overview of the DDR2 I/F on the MPC8548 and MPC8641D

Questions?

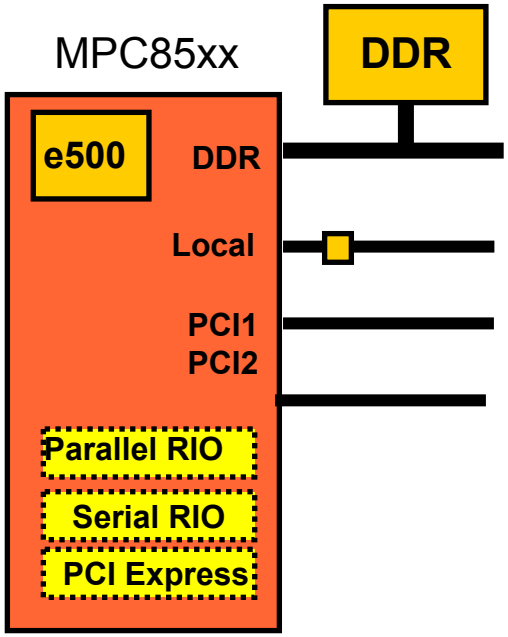
- **Introduction to Freescale's SoC Platforms**
  - History and Evolution of SoC at Freescale
  - MPC83xx, 85xx, 86xx Platforms and Available Standard Products
- **Scalable Performance**
  - Core Comparisons and Advantages: e300, e500, e600
  - Application Software Compatibility
- **Scalable Connectivity**
  - Peripherals and Interfaces
- **Scalable Integration**
  - Buses and Controllers
  - Driver Software Compatibility
- **Session Summary**
- **Questions**

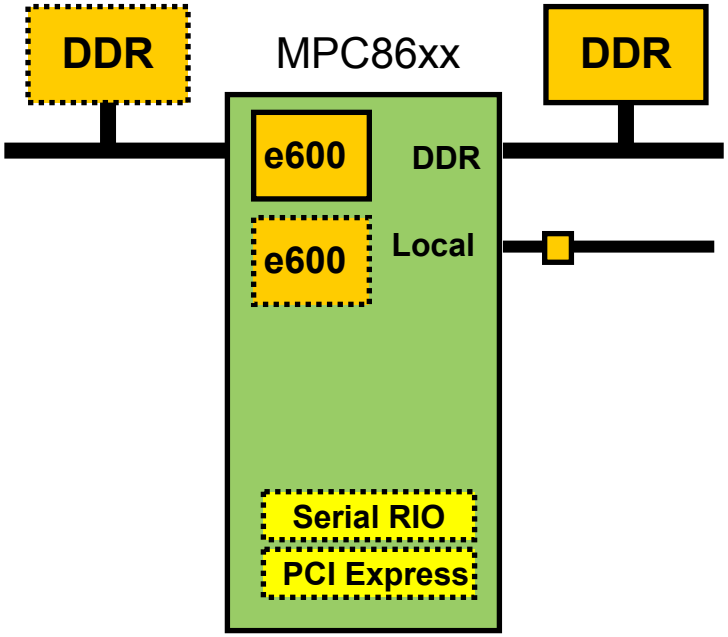


Scalable Connectivity

Supplementary Slides

Serial Interconnects



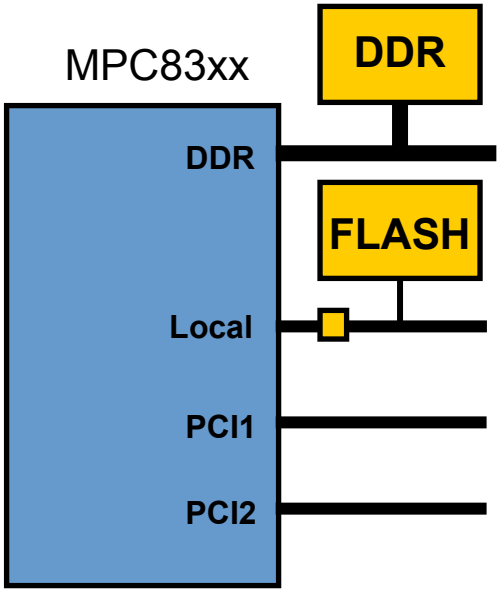


(#lanes)	P-RIO	S-RIO	PCI-Ex
8540	P-RIO(8)		
8541/E			
8555/E			
8560	P-RIO(8)		
8543/E			PCI-Ex(4)
8545/E			PCI-Ex(4)
8547/E			PCI-Ex(8)
8548/E		S-RIO(4)	PCI-Ex(8)

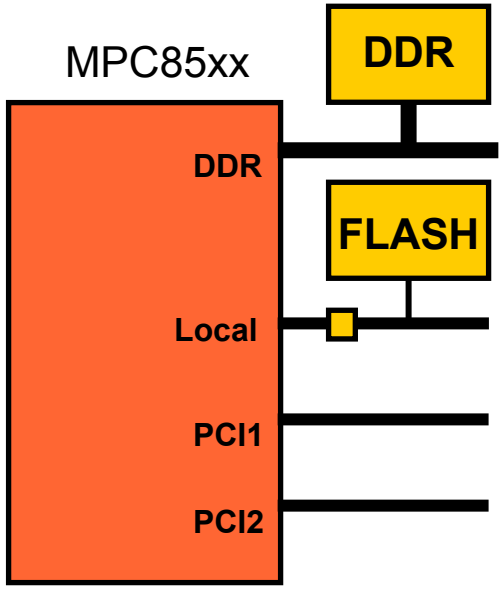
(#lanes)	S-RIO	PCI-Ex1	PCI-Ex2
8641D	S-RIO(1/4)	PCI-Ex (1/2/4/8)	
		PCI-Ex (1/2/4/8)	PCI-Ex (1/2/4/8)
8641	S-RIO(1/4)	PCI-Ex (1/2/4/8)	
		PCI-Ex (1/2/4/8)	PCI-Ex (1/2/4/8)

P-RIO Parallel Rapid IO
S-RIO Serial Rapid IO
PCI-Ex PCI Express

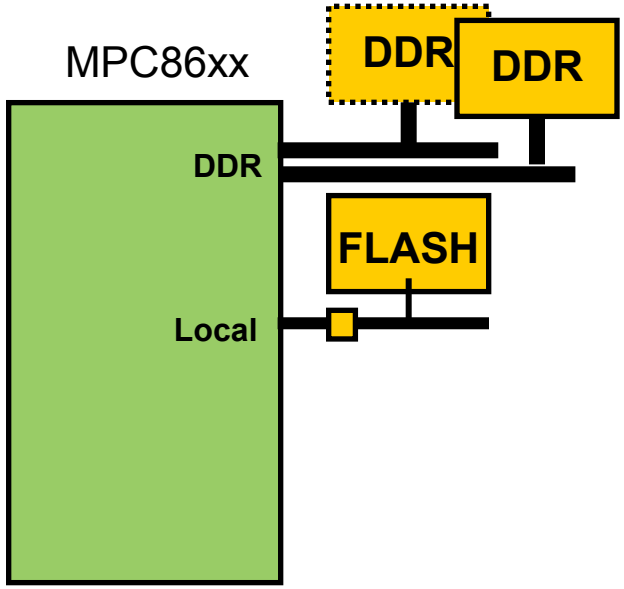
PCI Bus Options



8343/E	PCI1-32b	
8347/E	PCI1-32b	
8349/E	PCI1-64b	
	PCI1-32b	PCI2-32b
8360/E	PCI1-32b	



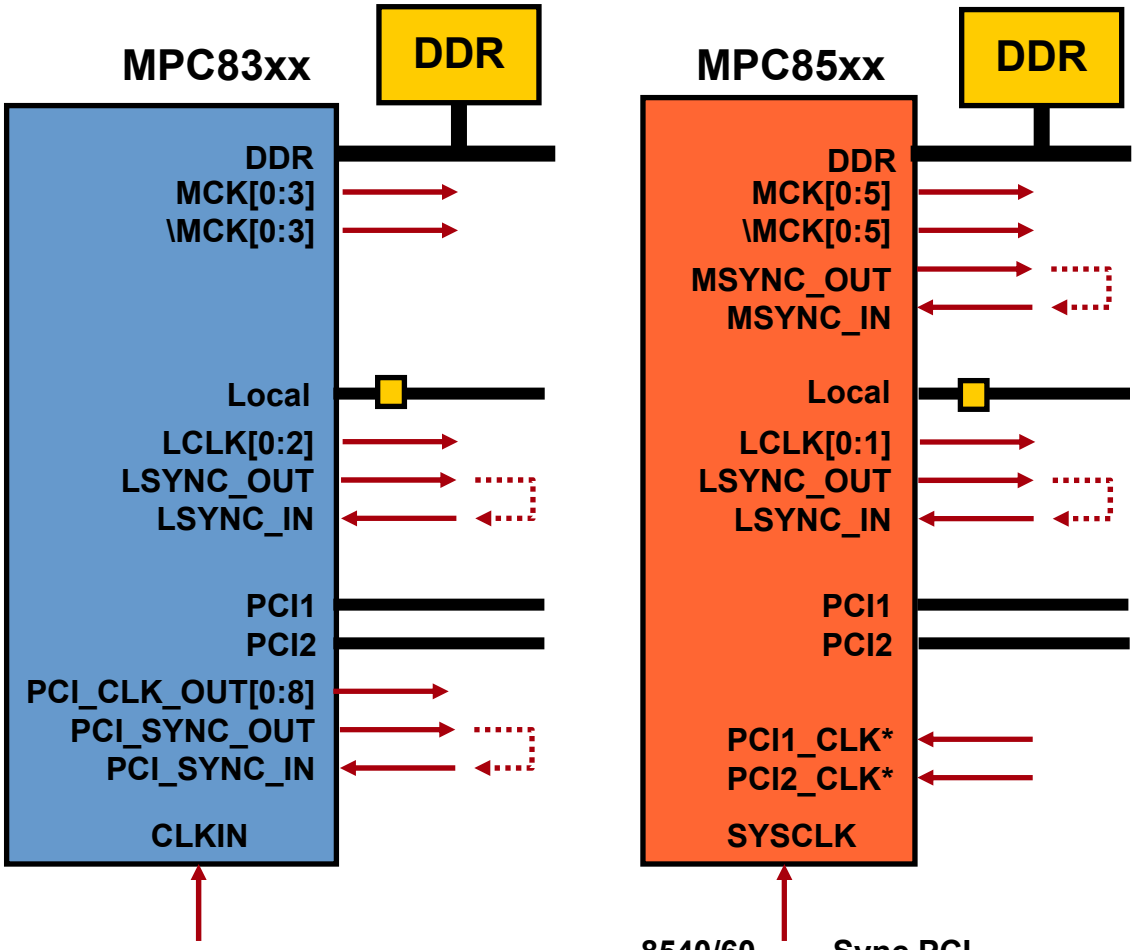
8540/60	PCI1/X-64b	
	PCI1-32b	
8541/55/E	PCI1-64b	
	PCI1-32b	PCI2-32b
8543/E	PCI1-32b	
8545/E	PCI1-64b	
	PCI1-32b	PCI2-32b
8547/E	PCI1/X-64b	
8548/E	PCI1/X-64b	
	PCI1-32b	PCI2-32b



8641	-
8641D	-

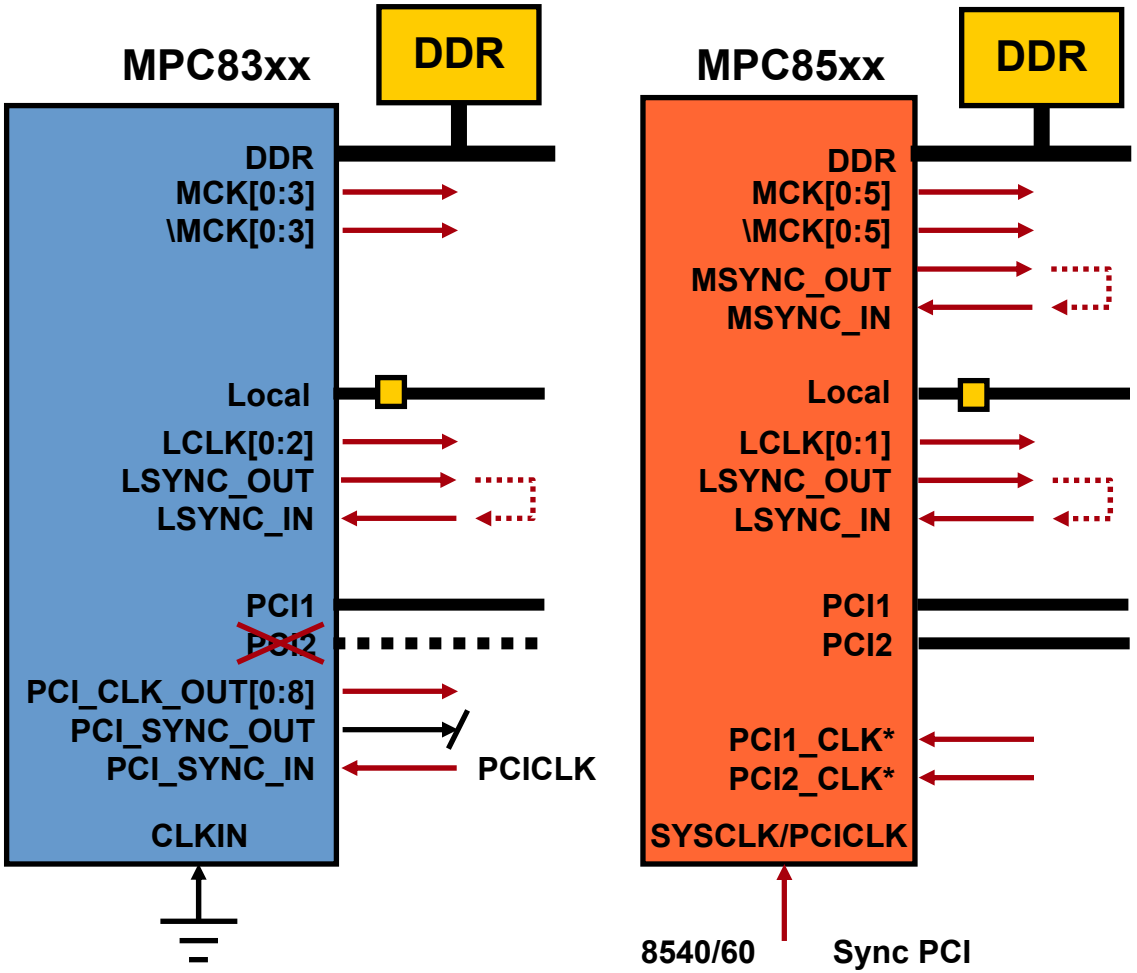
* PCI Functionality can be added by using a low cost PCI-Express to PCI Bridge Chip

Clocking (PCI Host)

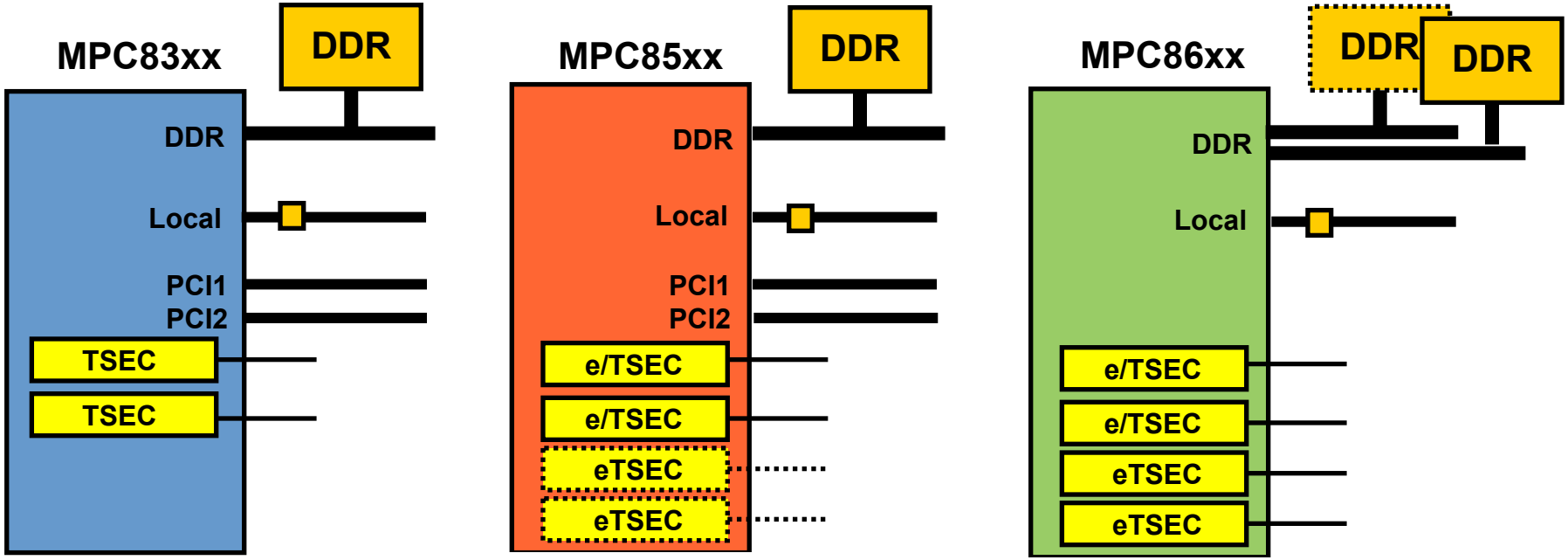


8540/60	Sync PCI SYSCLK=PCICLK
8541/55/E*	Sync/ASync PCI

Clocking (PCI Agent)



Ethernet



	10/100/1000	10/100
8343/E	2 (TSEC)	
8347/E	2 (TSEC)	
8349/E	2 (TSEC)	
8358/E	2 (UCC)	4 (UCC)
8360/E	2 (UCC)	6 (UCC)

	10/100/1000	10/100
8540	2 (TSEC)	1 (FEC)
8541/E	2 (TSEC)	2 (FCC)
8555/E	2 (TSEC)	2 (FCC)
8560	2 (TSEC)	3 (FCC)
8543/E	2 (eTSEC)	
8545/E	2 (eTSEC)	
8547/E	4 (eTSEC)	
8548/E	4 (eTSEC)	

	10/100/1000
8641	4 (eTSEC)
8641D	4 (eTSEC)

FCC	Fast Communications Controller (10/100)
UCC	Universal Communications Controller (up to 2 GigE)
TSEC	Triple Speed Ethernet Controller (10/100/1000)
eTSEC	Enhanced TSEC with FIFO mode, TCP/IP Checksum, QoS

‘e’nhanced Triple Speed Ethernet Controller - eTSEC

Feature of the MPC8548E and MPC8641D Families

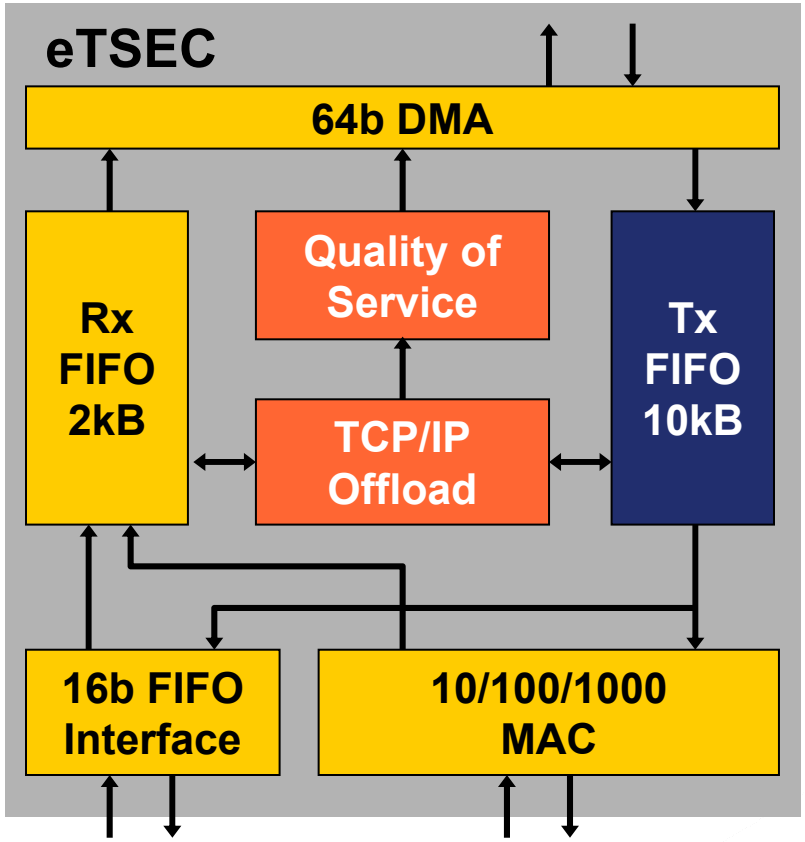
Optimizes CPU performance on TCP/IP
- TCP/IP checksum offload Rx + Tx
- IPv6 support in H/W

QoS support for 16 H/W queues (8 Rx + 8 Tx)
- Customizable per-packet filtering/filing to 64 logical receive queues
- 802.1p, IP TOS, Diffserv classification
- Support for weighted fair queuing
- TCP/UDP port-based flows
- Assist firewall through IP/TCP/UDP reject
- Ethernet preamble sorting and insertion

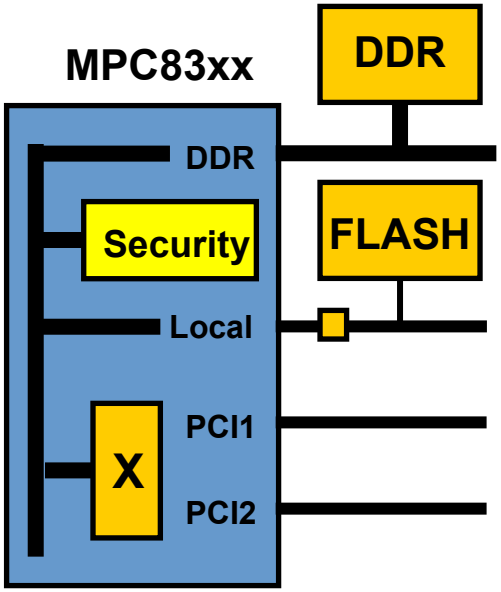
FIFO I/F to ASICs + (R)GMII/(R)MII/(R)TBI
- 8/16-bits @ OC-48 rates and above

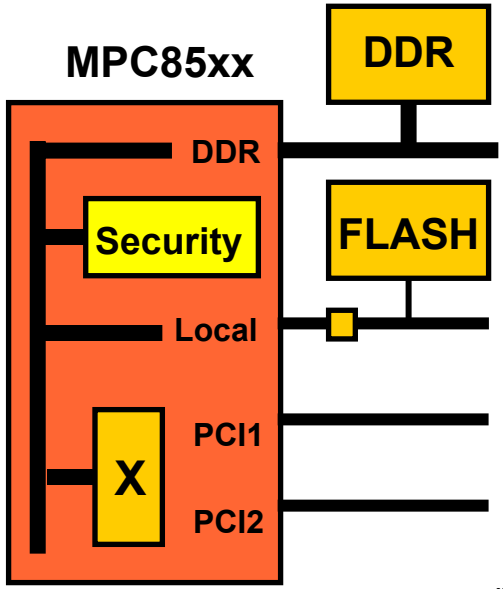
Layer 2 features
- VLAN insertion and deletion per frame
- 16 exact-match MAC addresses

Code compatible by default with standard TSEC
- MPC8349E, MPC8560, MPC8555E Families



Security Engine





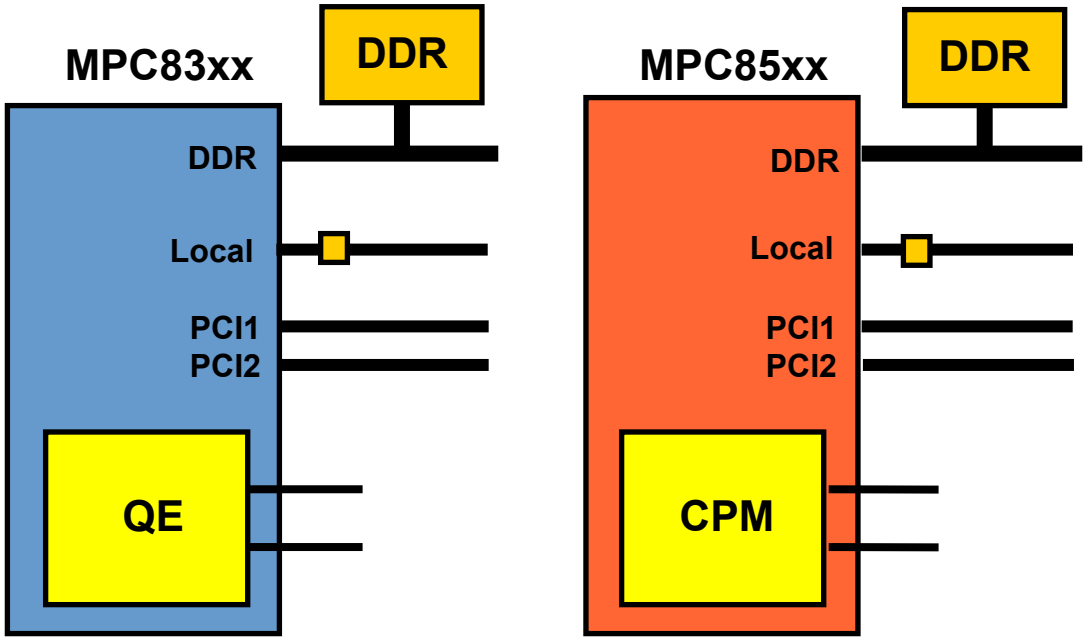
8343E	166MHz	
8347E	166MHz	
8349E	166MHz	
8360E	166MHz	

8541E	166MHz	SEC2.0
8555E	166MHz	SEC2.0
8543E*	333MHz	SEC2.1
8545E*	333MHz	SEC2.1
8547E*	333MHz	SEC2.1
8548E*	333MHz	SEC2.1

Common Features
- 4 Crypto Channels
- PKEU, AESU, DEU, AFEU, MDEU, RNG
- 256byte Tx + 256byte Rx FIFOs per Unit
- Single Pass IPSEC

***Special Features**
- KEU Kasumi Engine for 3G
- Single Pass SSL

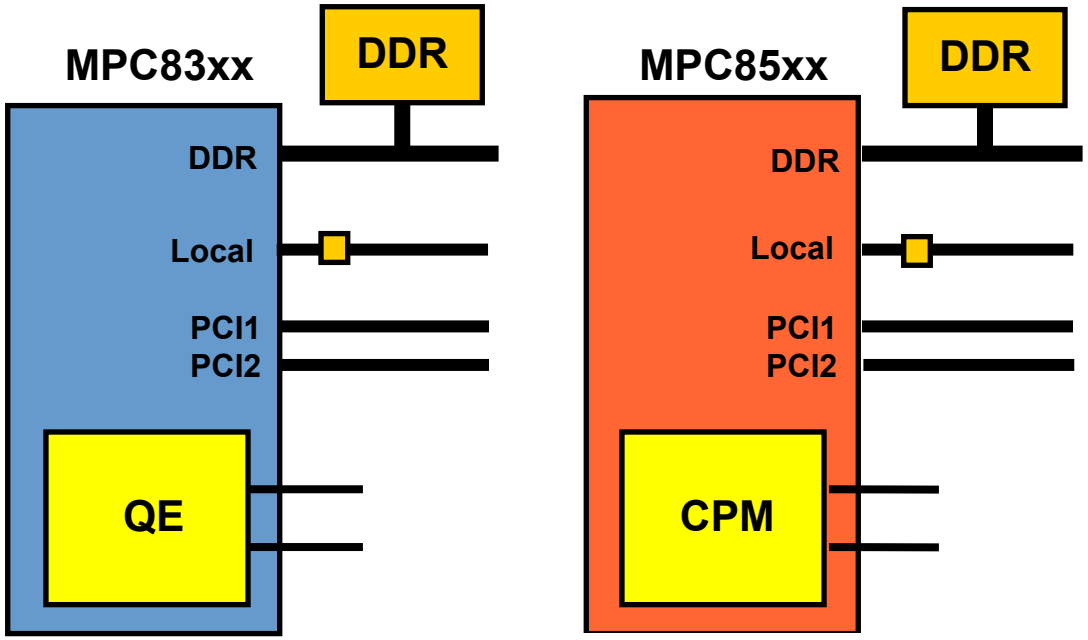
Communications Processor



8360/E	2x500MHz	8UCC, MCC	8555/E	333MHz	2FCC, 3SCC, USB
8358/E		6UCC	8560	333MHz	3FCC, 4SCC, 2MCC

CPM	Communications Engine
QE	QUICC Engine
FCC	Fast Communications Controller
SCC	Serial Communications Controller
MCC	Multi-Channal Controller
UCC	Universal Communications Controller

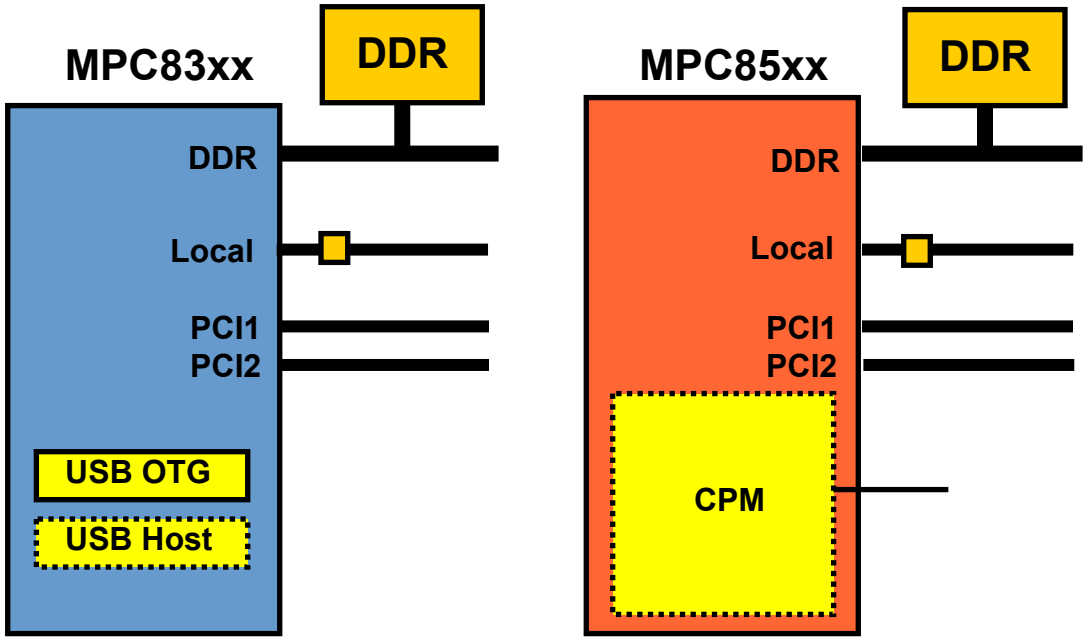
ATM



	UTOPIA (MPHY)	IMA		UTOPIA (MPHY)	IMA
8358E	1 UL2/POS (31-124)	-	8555/E	1 UL2 (31)	-
8360/E	2 UL2/POS (124)	8 T1/E1	8560	2 UL2 (31)	8 T1/E1

FCC	Fast Communications Controller (ATM AAL0/1/2/5)
UCC	Universal Communications Controller (ATM AAL0/1/2/5)
UL2	8/16-bit UTOPIA Level 2

USB



	USB
8343/E	HS (OTG)
8347/E	HS (Host) + HS (OTG)
8349/E	HS (Host) + HS (OTG)
8358/E	FS (Host/Dev)
8360/E	FS (Host/Dev)

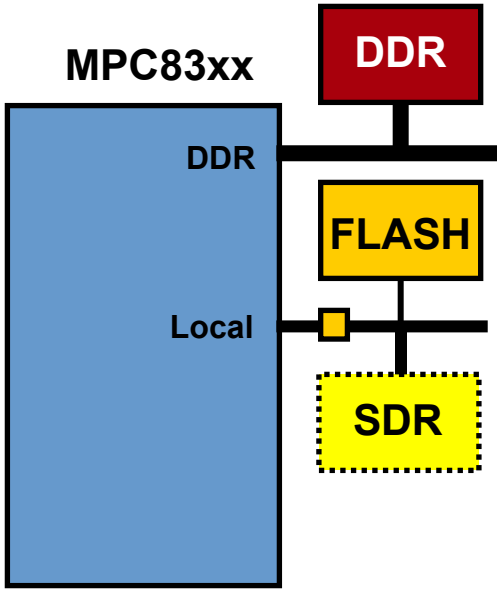
	USB
8540	-
8541/E	FS (Host/Dev)
8555/E	FS (Host/Dev)
8560	-
8543/E	-
8545/E	-
8547/E	-
8548/E	-

FS	Full Seed (12 Mbps)
HS	High Speed (480 Mbps)
OTG	On The Go (Configurable Host/Device)

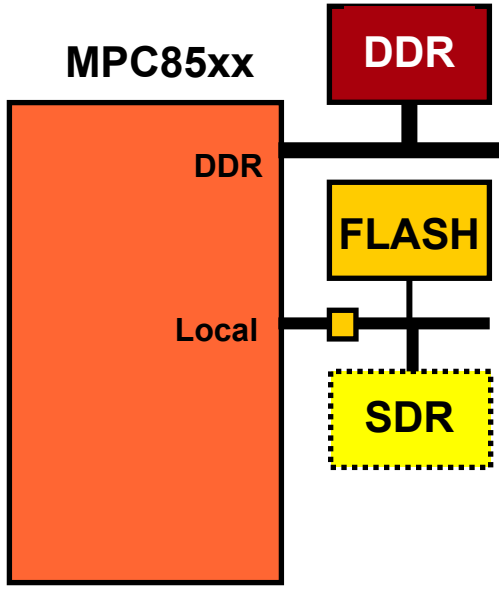
Scalable Integration

Supplementary Slides

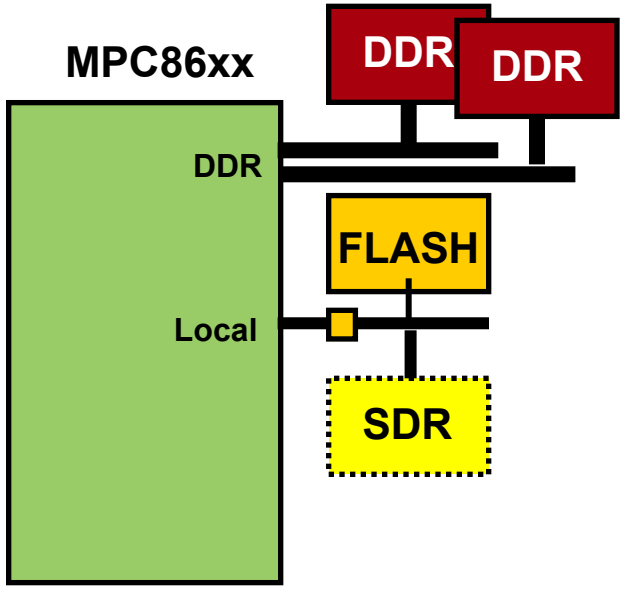
DDR SRAM – Packet Memory Options



DataRate	DDR1	
8343/E	333MHz	Parity
8347/E	333MHz	Parity
8349/E	333MHz	Parity
8358/E	333MHz	Parity
8360/E	333MHz	Parity

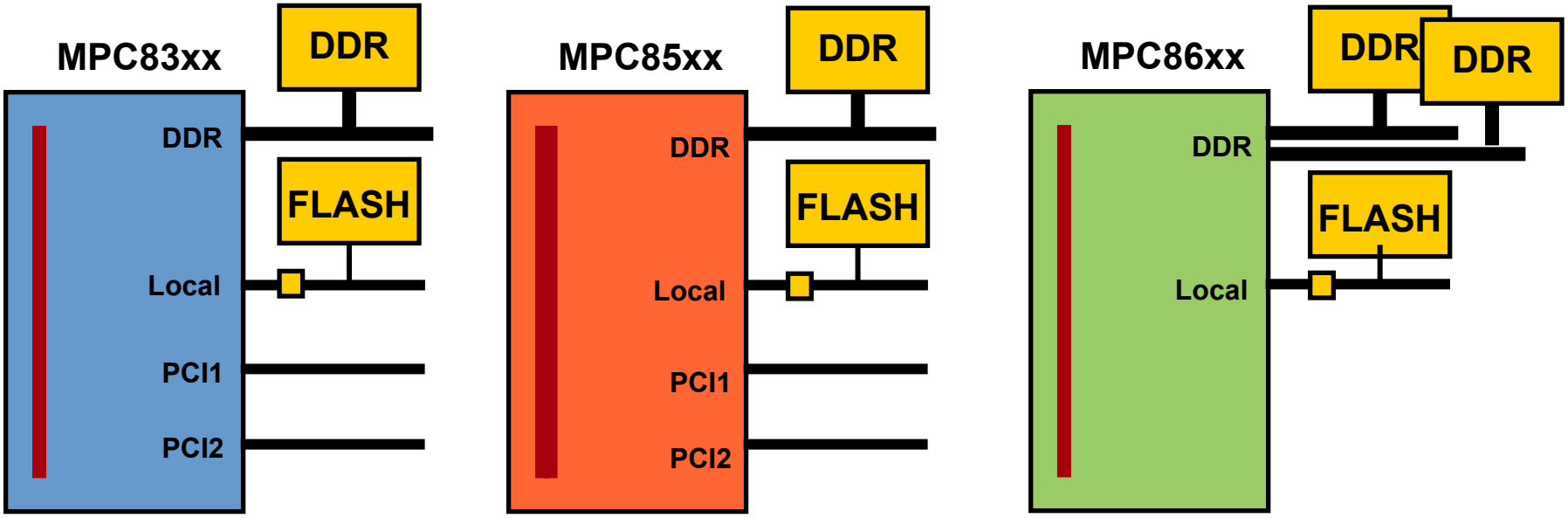


Data Rate	DDR1	DDR2	
8540/60	333 MHz	-	ECC
8541/55/E	333 MHz	-	ECC
8543/E	400 MHz	400 MHz	ECC
8545/E	400 MHz	400 MHz	ECC
8547/E	400 MHz	533 MHz	ECC
8548/E	400 MHz	667 MHz	ECC



Data Rate	DDR2	DDR2	
8641	333MHz x2	667MHz x2	ECC
8641D	333MHz x2	667MHz x2	ECC

Core Bus



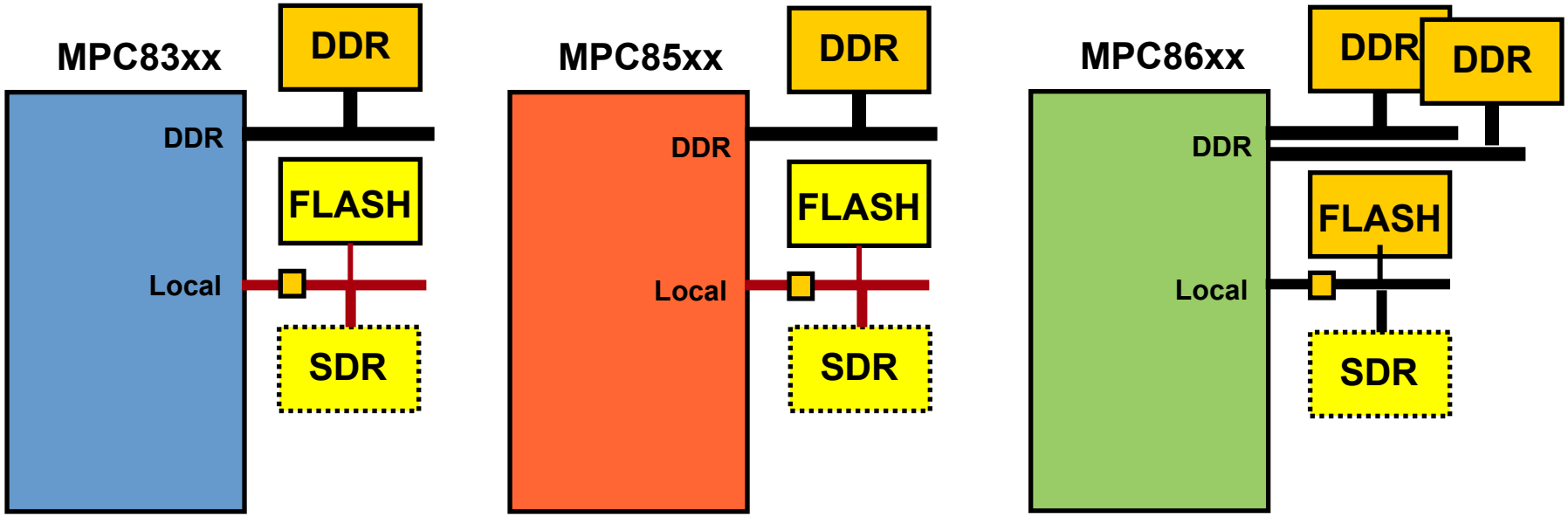
8343/E	CSB : 64-bit, 333MHz
8347/E	CSB : 64-bit, 333MHz
8349/E	CSB : 64-bit, 333MHz
8358/E	CSB : 64-bit, 333MHz
8360/E	CSB : 64-bit, 333MHz

8540/60	CCB : 128-bit, 333MHz
8541/55/E	CCB : 128-bit, 333MHz
8543/E	CCB : 128-bit, 400MHz
8545/E	CCB : 128-bit, 667MHz
8547/E	CCB : 128-bit, 667MHz
8548/E	CCB : 128-bit, 667MHz

8641	MPX : 64-bit, 667MHz
8641D	MPX : 64-bit, 667MHz

CSB	Coherent System Bus (60x)
CCB	Core Complex Bus
MPX	Enhanced 60x Bus

Local Bus



	Local Bus	
8343/E	AD32, 133MHz	Parity
8347/E	AD32, 133MHz	Parity
8349/E	AD32, 133MHz	Parity
8358/E	AD32, 133MHz	Parity
8360/E	AD32, 133MHz	Parity

	Local Bus	
8540/60	AD32, 167 MHz	Parity
8541/55/E	AD32, 167 MHz	Parity
8543/E	AD32, 133 MHz	Parity
8545/E	AD32, 133 MHz	Parity
8547/E	AD32, 133 MHz	Parity
8548/E	AD32, 133 MHz	Parity

	Local Bus	
8641	AD32, 167 MHz	Parity
8641D	AD32, 167 MHz	Parity

- All Platforms utilize the same GPCM, 3 UPM, SDRAM Controllers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