

## AN1058

## Reducing A/D Errors in Microcontroller Applications

### Introduction

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Many significant benefits can be realized in an electronic product by converting analog signals into the digital domain. From drift-free signal filtering to extremely reliable signal detection, the digital domain offers a level of performance many times only approximated by its analog circuit-based counterpart. Once cost prohibitive, converting analog signals into the digital domain has become more cost effective. These decreasing costs, increasing digital semiconductor speeds, and the benefits of digital processing have contributed significantly to the increasing popularity of digital systems and to the rise of the digital system with built-in analog interfaces.

One such popular system on silicon is the single-chip microcontroller unit (MCU). Now available from many manufacturers and in many forms, MCUs with resident analog interfaces like analog-to-digital converters (ADC) and other on-chip peripherals can provide unsurpassed cost effectiveness to a product's design. The MCU with integral ADC may easily be used to convert analog signals in the digital domain with the convenience of an already defined on-chip ADC-to-CPU interface. In addition, the MCU offers the flexibility afforded to all software-based systems.

MCUs have liberated many board-level designers from selecting, designing, and debugging microprocessor peripherals in multichip assemblies. This type of highly integrated solution is becoming more

popular than the multichip solution. Consequently, it is reasonable to expect that the practicing design engineer will eventually work with an MCU-based system. Yet despite the advantages of the MCU system, some integrated peripherals such as the ADC offer new challenges to the designer. By incorporating a wide bandwidth linear system, such as an ADC, on the same die with a high-speed digital central processor unit (CPU), ADC performance can be adversely affected. Noisy ADC readings functionally manifest themselves in a range from merely annoying and relatively benign glitches to more catastrophic hard failures.

In any case, an MCU-based system does not have to be at the mercy of poor MCU/ADC performance. Fortunately, by following some fairly rudimentary systems-level guidelines in the design phase of the MCU-based product, potential ADC performance problems can be avoided.

To resolve ADC performance issues, it is necessary to understand a little about the nature of the MCU and the various areas of susceptibility of several ADC types. Although much information presented in this application note assumes that the ADC is resident on-chip with the CPU, other converter types not typically found on-chip with MCUs are discussed for those instances in which a multichip combination is encountered. The following paragraphs also apply to these less frequent hardware combinations.

## ADC Types

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Even when the ADC is available on-chip with an MCU where the unpleasant task of interfacing and debugging the ADC-to-CPU interface is done, obtaining maximum performance from the ADC requires attention to application details of the given MCU/ADC combination. The type of design precautions and applications details needed to avoid problems varies as a function of the type of ADC used. Understanding the mechanics of the given ADC is crucial to improving performance.

ADCs may be categorized into five main categories. Although each type has unique capabilities and traits, each has surprisingly similar points of vulnerability.

The categories are:

- Integrating
- Servo
- FLASH
- Successive-approximation converter (SAC)
- Hybrid

The integrating converter has appeal for applications requiring high resolution (16-bit or higher) and low cost. Because the basic converter is simply implemented (see **Figure 1(a)**), hardware is minimized while high resolution is obtained. In addition, the integrating ADC may provide some noise immunity that is not feasible with higher speed designs. Although it is possible to build the integrating converter onto MCU chips (there is nothing technologically impeding such a construct), its lower speed has apparently been discouraged by MCU designers since it is currently not offered on an MCU by a major manufacturer.

Whereas the integrating converter tends to be the slowest of ADC types, the servo converter tends to have the highest resolution and fastest conversion times in its most recent advancement — the sigma-delta converter. The more traditional servo converter tries to balance the charge or voltage on an input comparator by using a feedback configuration (see **Figure 1(b)**) to force slewing from a previous charge or voltage to the current input signal level applied to the other input of the same comparator. This process is followed by appropriately changing a digital counter up or down (in this form, the converter is often called a tracking converter). Before the sigma-delta variation, the servo converter was less popular than other converter types primarily due to its slew rate limitation. Nothing about the servo converter would prevent its inclusion onto an MCU die; once BiCMOS processes improve, this converter type will probably become a popular feature of future MCUs (particularly the sigma-delta variation, most of which is linear circuitry).

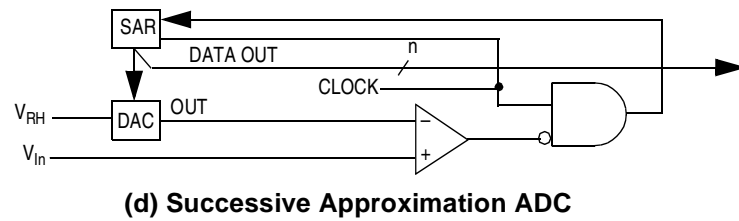
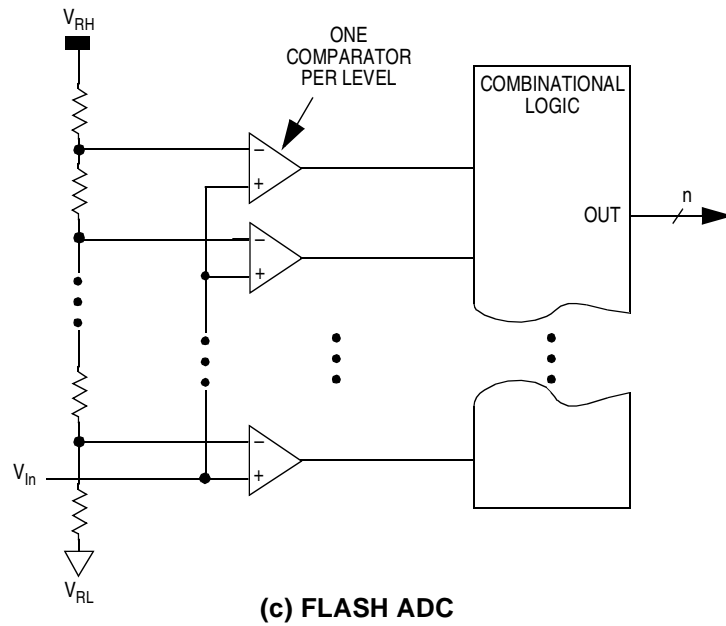
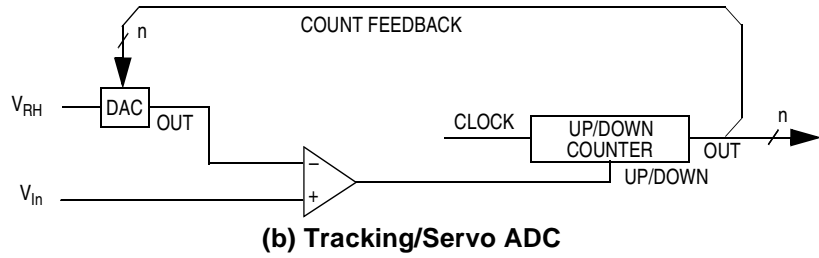
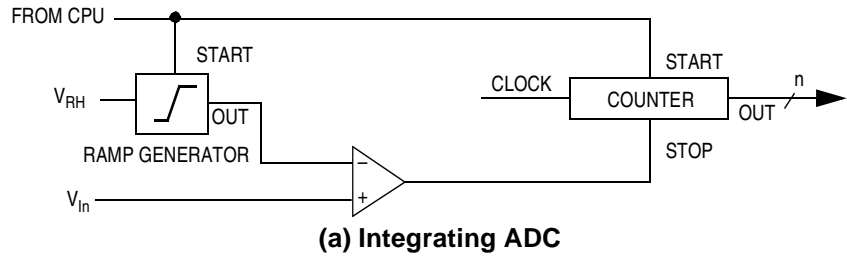


Figure 1. ADC Types

Although the sigma-delta variation of the servo converter provides high-resolution conversions and maintains a relatively high throughput rate, the fastest type is the FLASH converter. By stringing together several voltage comparators (one per desired level to be detected), conversion bandwidths in excess of 100 MHz are now quite commonplace (see [Figure 1\(c\)](#)), albeit at lower resolutions (four to six bits are common). As the input voltage is applied to one input of all the comparators, a set of reference voltages is applied to the other comparator inputs. After a period of time has elapsed, determined primarily by the propagation delays through the comparators, the discrete-level representation of the input voltage is available at the comparator outputs. FLASH conversion, although incredibly fast, requires a tremendous number of devices to implement even modest-resolution converters. In addition to the number of transistors necessary to implement each comparator, the outputs of each comparator are typically input to a combinational logic array to form a desired output code. Consequently, this converter, which consumes much silicon area when compared to other converter types, has not been widely accepted by MCU designers and users.

The fourth ADC type is the successive-approximation converter (SAC). Of all current converter types, the SAC is the most popular. (See [Figure 1\(d\)](#)). This popularity is primarily due to its applicability to smaller circuit requirements, medium-to-fast conversion speeds, and the medium- to high-resolution applications (8 to 16 bits). Like other converter types, the SAC uses a differential voltage comparator to compare the input signal with a reference voltage. By performing a binary search, conversion rates of one bit per clock are possible. Because only one comparator is typically required and the output code is inherent in the conversion process, circuitry and silicon surface area are reduced when compared with other conversion methods. Although the exact implementation varies from silicon-chromium-based to charge-redistribution, this ADC is currently the most prevalent type found on MCUs.

The fifth ADC category is the hybrid converter. In this case, the term hybrid is not used to reference a specific implementation approach, but rather implies combining one or more ADC types to form an ADC with different performance characteristics.

For example, some of the faster and higher resolution ADCs now employ a hybridized technique which utilizes FLASH conversion prescaling followed by an SAC. In this case, almost instantaneous prescaling is accomplished and easily interfaced to an existing SAC design. Hybrid converters are a very viable alternative as an MCU peripheral and may find eventual popularity in MCU designs when higher resolution converters are needed.

## ADC Noise Susceptibility

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The comparator is the cornerstone of the A/D conversion process. The ability of the comparator to announce the presence of small voltage/current differentials with large changes in its output voltage make the comparator invaluable to the A/D conversion process. Yet, this same feature also accounts for the largest potential source of ADC malfunction. Of course, degradation of the comparator's desired action, and hence the ADC, is most usually caused by unwanted noise.

Two basic characteristics of the comparator affect noise susceptibility:

- Bandwidth
- Power supply connections

Wide bandwidth comparators easily respond to noise as well as to signals. Even in the low-speed integrating converter, the accuracy of measurement is heavily contingent upon the comparator's speed of operation. To illustrate, imagine that a very slowly varying input signal has been applied to an input of such a comparator. For a single-slope integrating converter, the other comparator input will have a linearly increasing voltage (or other convenient shape) applied to it. As this voltage ramp increases, an independent digital counter (started at the same time the voltage ramp began) will count clock pulses provided by some timebase. When the voltage ramp finally exceeds the input voltage, the comparator will change state. If the comparator fails to respond to the voltage ramp in a timely fashion, the digital counter will register an incorrect count when compared to the results obtained by a

perfectly fast comparator, implying that the response time (characterized by bandwidth) must be reasonably fast even in the slowest ADC types.

Consequently, a wide bandwidth comparator will appropriately respond not only to input/reference signals but also to any other signal present at the comparator input terminals (including noise components superimposed upon the signals of interest).

The typical comparator uses some form of differential front end. The operation of the differential front end is dependent upon biasing networks that are ultimately connected to the supply terminals of the comparator. Therefore, the comparator should be considered as a 5-terminal device — two differential inputs, one output, and two inputs to the biasing networks — for the purposes of designing with the ADC. The implication is that signals present at the supply terminals of an ADC, particularly the high-frequency signals typically superimposed on the power supply in digital systems, can affect comparator and ADC operation.

Due to the high bandwidth of the comparator found in ADCs, the designer of a given system should be extremely careful about the type and amount of signals allowed to reach the comparator stage of the ADC, particularly the power supply terminals. For this reason, some of the more mundane and overlooked aspects of electrical product design, such as printed circuit design and circuit interconnection, become increasingly critical to the success of the MCU/ADC system.

## Appropriate Design Techniques

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Most of the MCU is digital. As seen in [Figure 2](#), a major portion of the MC68HC11E9, a representative MCU, is digital circuitry. Thus, it is reasonable to assume that digital design practices will generally be employed when designing with the MCU.

With an analog-based subsystem, such as the M68HC11 ADC, normally accepted digital design practices may not be sufficient to ensure satisfactory performance of the converter.

As an illustration, consider noise levels normally found on the power supply of a typical high-speed HCMOS digital system. It is not unusual to find 100 mV<sub>PP</sub> broadband noise riding on top of the positive voltage rail. With a nominal 5-volt HCMOS system, the resulting voltage drop, down to 4.9 volts, is above the V<sub>OH</sub> for HCMOS. Thus, the 100-mV signal will probably not upset circuit operation. When present in such a robust digital system (HCMOS), this 100-mV noise signal is a mere visual nuisance on the oscilloscope. Because of the theoretically infinite signal-to-noise ratio of digital gates, the presence of the 100-mV noise poses no practical threat.

However, when such a noise signal is inserted into an ADC system, the results can be much more dramatic. In an 8-bit ADC system with a nominal 5-volt reference, this same 100-mV noise can result in a greater than 5-bit error in the ADC reading. Thus, an MCU system utilizing an ADC assumes a different electrical character that requires application of design practices not traditionally used in the design of digital systems.

What design practices should be used?

To correct or avoid a noisy ADC/MCU design, separate the noisy signals from the sensitive ones. The challenge is to design a system in which this separation is practically realized. The closer to the ideal of completely separating the noisy signals from the sensitive ones, the better. For situations where the noisy and sensitive circuits cannot be completely separated, reduce the noise coupling as much as possible. Since it is difficult to axiomatically specify how to implement both concepts in all cases, an illustration will aid understanding and provide an analogy by which individual situations may be gauged.

Freescale tests 100 percent of the ADCs found on its MCUs. Before any M68HC11 ADCs leave the factory, they have been tested and verified for specified ADC performance. Even so, it is possible to operate the M68HC11 in an environment that causes the M68HC11 ADC to subsequently malfunction. These two scenarios in the life of such an MCU indicate not, strictly speaking, a parts-related anomaly, but rather a significant interaction of the part's characteristics with the electrical environment.



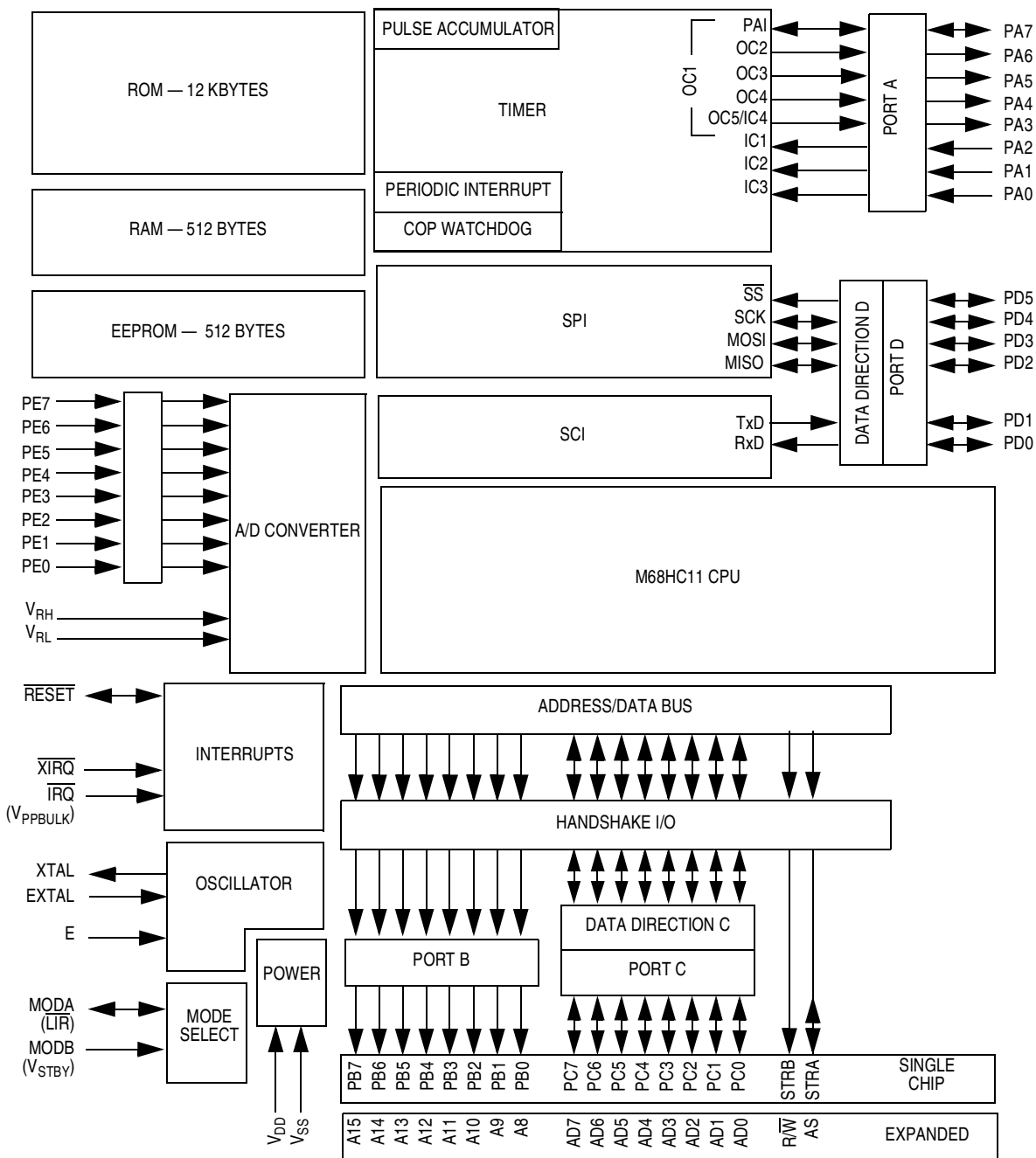


Figure 2. MC68HC11E9 Block Diagram

Typically, a large contributor to malfunction is the printed circuit board (PCB) layout. Since the PCB can influence many of the circuit parametrics (reactance, voltage, etc.), the PCB layout can help or hinder ADC performance. Yet, the PCB layout is not typically done by the circuit's designer. More importantly, laying out the PCB artwork, up to and including the width and placement of traces, is often performed by people without a detailed knowledge of correct electrical circuit design practices. Many PCB designers are only concerned with ensuring that they have connected all the points connected in the schematic. Although this has its economic advantages, this can be a dangerous proposition with regard to ADC performance.

**Figure 3** shows an example of such a PCB layout which, although it manages to distribute the power to all of the devices, provides several potential sources of ADC/MCU performance problems.

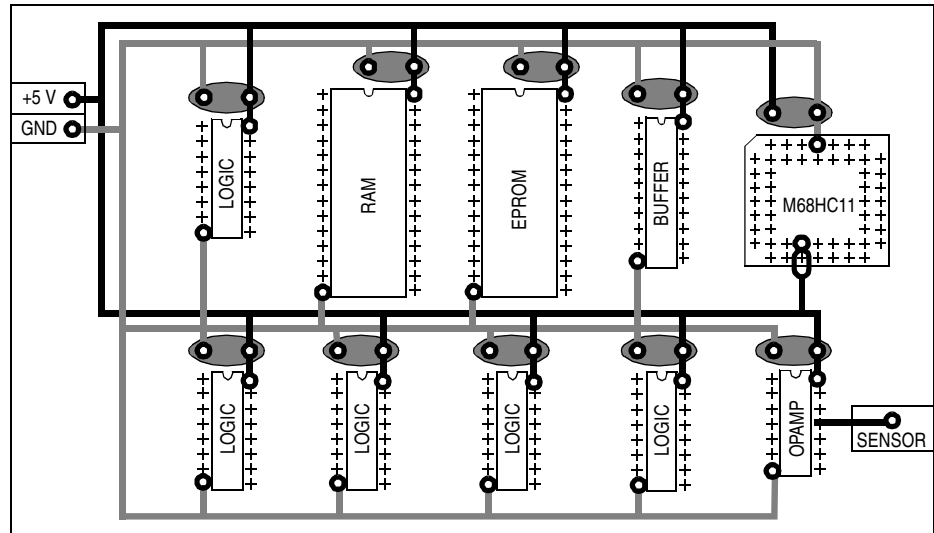
First, the MCU/ADC is placed farthest from the power terminal, meaning that the MCU return currents will be mixed with the digital circuit currents between the MCU and the power terminal. Although the MCU may not produce large return currents in the power return, high-speed digital circuits typically do. The inductance of PCB traces at high frequencies can be significant enough to produce large noise spikes when measured between the ground pin of the MCU and the ground terminal of the board.

Second, the opamp, which buffers the signals to the ADC inputs on the MCU, is physically located close to the MCU but is electrically located in a very poor place. As with the MCU, the opamp power supply return will be corrupted with high-frequency spikes. However, the voltage drops measured between the opamp and the MCU will be even worse than those measured between the MCU and the power terminal. When deciding which parts are to be jointly located on the PCB, the electrical impact of conductor distance and tolerance to any induced noise must be considered.

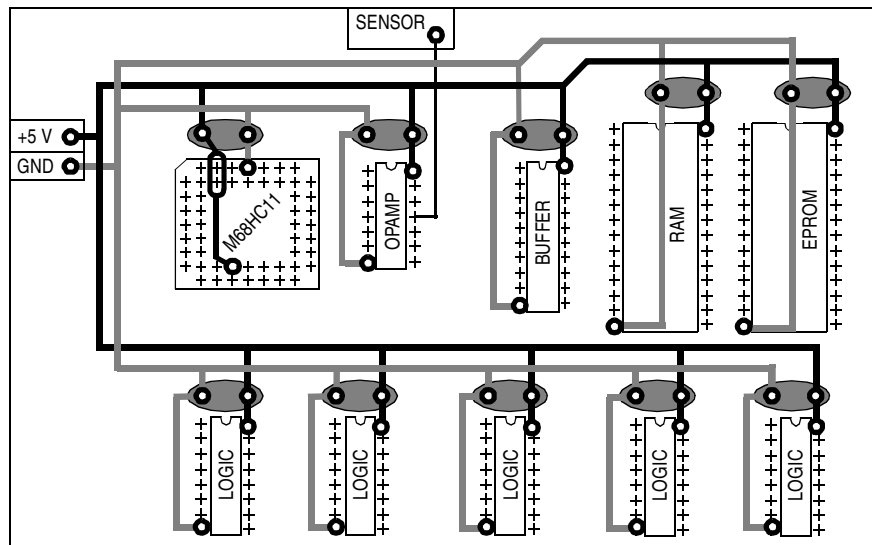
Third, the bypass capacitors, as shown, are ineffectual in reducing high-frequency noises on  $V_{DD}$ . To perform the decoupling function properly, bypass capacitors should be attached as close as possible to the IC power pins they are intended to bypass. In addition, PCB trace

inductance should be minimized between the leads of the capacitor and the power pins.

**Figure 3** illustrates a few of the PCB-related errors that can degrade ADC performance. Specific PCB designs involving MCU/ADCs should be carefully engineered. A better PCB layout is depicted in **Figure 4**, which connects the defects shown in **Figure 3**.



**Figure 3. Poor Layout Design**



**Figure 4. Improved Layout Design**

## A Specific MCU with ADC

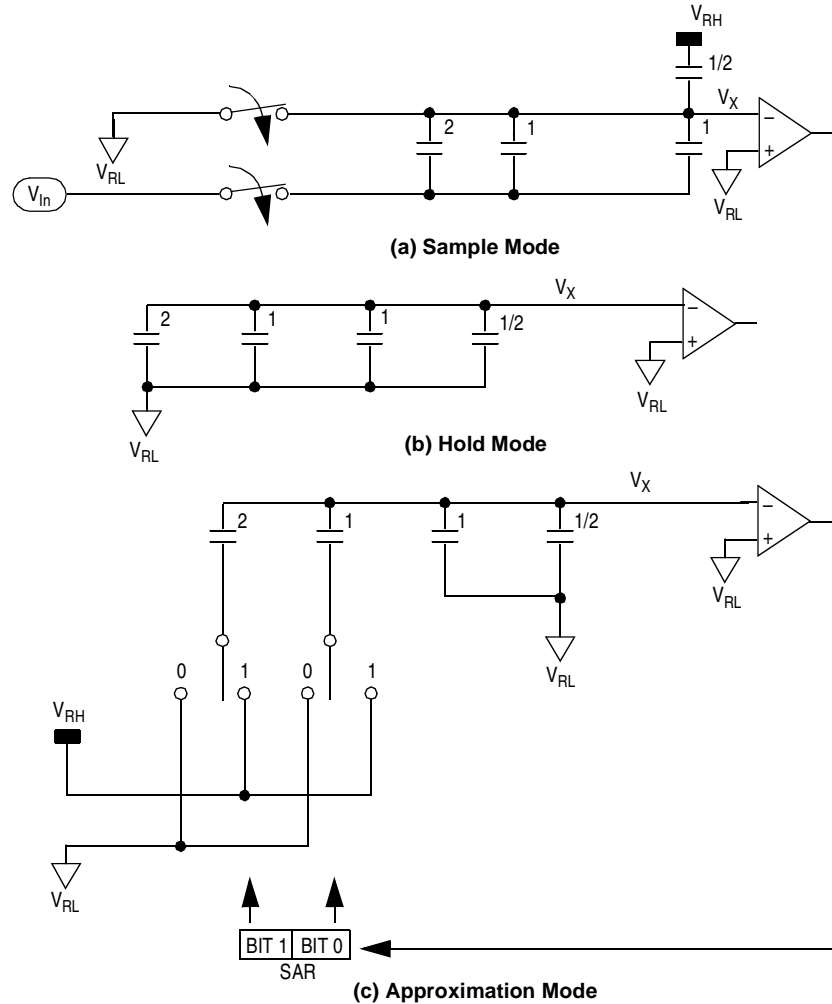
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Other factors involving a more specific ADC system contribute to reduced ADC performance. Thus, this discussion will focus on the ADC system found on the Freescale M68HC11 Family of MCUs.

A unique implementation of an SAC, the standard M68HC11 (2-MHz bus) ADC provides a 16- $\mu$ s 8-bit A/D conversion with the convenience of an on-chip MCU peripheral. The ADC is a charge-redistribution SAC. The digital-to-analog converter (DAC) is implemented with capacitors rather than the usual R-2R silicon-chromium (SiCr) thin-film resistors. Although the SiCr resistor has the advantage over the commonly used diffused resistor in improved temperature stability and tracking, laser trimming is necessary to obtain ADC accuracies compatible with even medium-resolution converters. Processing this R-2R ladder presents a challenge since trimming one resistor in the network will change the current in the previously trimmed bit, requiring an iterative trimming process. Furthermore, the R-2R ladder requires careful control of the ON resistance in the MOS switches because the switches also determine the current flow through the R-2R network. The M68HC11 capacitive DAC avoids these shortcomings. The charge-redistribution method is easily fabricated using poly-poly capacitors. No trimming of the poly capacitors or MOS switches is required to obtain medium-resolution accuracies. As an added benefit, a sample-hold function, which extends the effective conversion bandwidth of the ADC, is an inherent by-product of the redistribution technique.

The internal operatives of the M68HC11 converter are relevant to preventing or reducing ADC errors. For converters using SiCr R-2R ladders, the impact of parametric phenomena may be different than for the M68HC11. It is necessary to understand the nature and implementation of the ADC to realize the highest performance from it. To understand the M68HC11 conversion process, a 2-bit example is presented (see [Figure 5](#)). A conversion is accomplished by a sequence of three operations. In the sample mode (see [Figure 5\(a\)](#)), the top plate is connected to  $V_L$  (0 volts), and the bottom plates are connected to the input voltage,  $V_X$ , resulting in a stored charge on the top plate that is proportional to the input voltage. In the hold mode (see [Figure 5\(b\)](#)), the

top switch is then opened, and the bottom plates are connected to  $V_L$ . Since the charge on the top plate is conserved, its potential goes to  $-V_X$ , which is the initial voltage at the input of the comparator. The approximation mode (see **Figure 5(c)**) begins by testing the value of the most significant bit by raising the bottom plate of the largest capacitor to the reference voltage,  $V_H$ . The equivalent circuit is now actually a voltage divider between two equal capacitances. The output of the comparator, after each capacitor is switched, determines whether the bottom plate of that capacitor will remain at  $V_H$  or be returned to  $V_L$  before the next capacitor is switched. Conversion proceeds in this manner until all bits have been determined and the result is stored in the successive-approximation register (SAR).



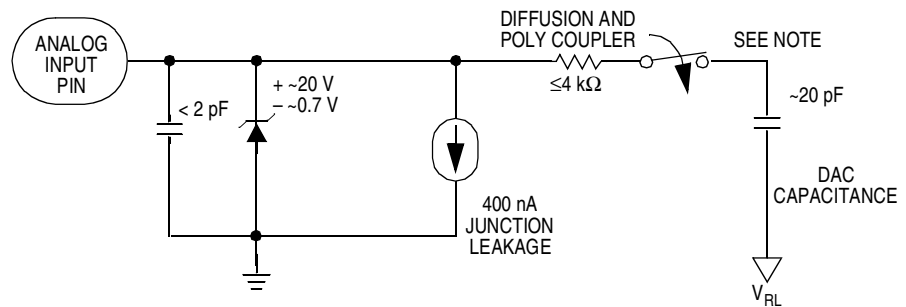
**Figure 5. ADC Conversion Modes**

Major sources of M68HC11 ADC errors controlled by external circuit parameters are discussed in the following paragraphs.

**Leakage Current on ADC Input Pin**

The electrical model of an M68HC11 ADC input pin is shown in **Figure 6**. The problem is caused by n-channel device junction leakages at this node (no p-channel devices are used here), which are worse at high temperatures.

Consequently, the leakage current is 1) unidirectional and 2) bound by the maximum specification of 400 nA. This leakage-induced error would tend to only cause a static lowering of ADC results. This leakage-induced error would tend to only cause a static lowering of ADC results. To avoid leakage effects, the external circuit network feeding the ADC pin(s) should maintain impedances, which in the presence of maximum leakage, would guarantee a maximum desired error. For example, if the maximum error (due to leakage) is desired to be  $\leq 1$  LSB with a 5-volt reference voltage, then the maximum source impedance (resistance) feeding this pin should be  $50\text{ k}\Omega = (\approx 19.5\text{ mV}/400\text{ nA})$ .



Note: This analog switch is closed only during the 12-cycle sample time.

**Figure 6. Electrical Model of an M68HC11 ADC Input Pin**

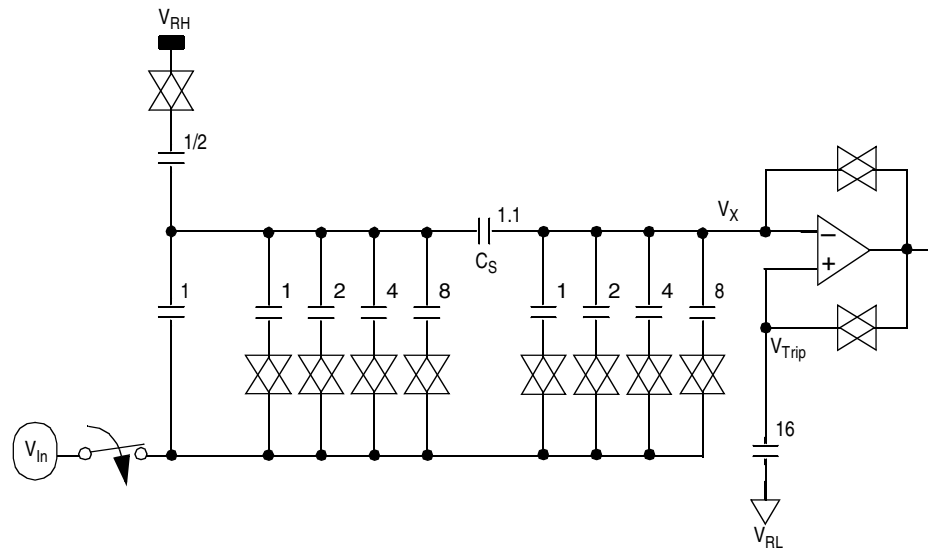
**Charge Time on Sample Capacitor**

By lengthening the resistance-capacitance (RC) time constant, comprised of the source resistance feeding the ADC pin and the DAC capacitance evidenced at the pin during the sample mode, errors may result. However, given the size of the DAC input capacitance, the size of the source resistance necessary to induce these RC time-constant errors will probably be inundated by the effects of the pin leakage described previously.

**$V_{DD}/V_{SS}$  and Input Terminal Noise**

The differential comparator used in the M68HC11 ADC derives its power from  $V_{DD}$  and  $V_{SS}$ , the power pins that supply the rest of the M68HC11 (see [Figure 7](#)). The M68HC11, when considered with respect to ADC performance, is a source of noise, partially due to the wave shape and harmonics associated with square waves. In addition, the complex relationship between the primary M68HC11 clock and related noise voltages are further complicated by dependence of the M68HC11 upon many software combinations, each sufficiently changing the noise characteristics emanating from the M68HC11. Therefore, ADC performance degradation, which is linked to noise generated on  $V_{DD}/V_{SS}$  by the M68HC11, can often appear related to execution of specific software combinations. As established earlier, this is due to the ADC wide bandwidth comparator.

**NOTE:** *Because the M68HC11 ADC uses a very wide bandwidth comparator capable of responding to noise components in excess of 20 MHz, it must be guarded against unwanted noise at its input terminals and  $V_{DD}/V_{SS}$  pins.*



**Figure 7. M68HC11 ADC in Sample Mode**

The reference to input terminal noise must be distinguished between noise externally superimposed on the input signal lines that is measured between a system reference and a given input signal (occurs from capacitive coupling between high-impedance ADC inputs and noisy signal sources or electro-magnetic interference) and voltage differentials experienced by different comparator inputs when referenced to each other. The importance of input terminal noise in this context is the presence of non-common-mode differential noise between the biasing networks in the comparator and the input lines. If, under noisy conditions, the same noise is presented to an input to the comparator and one of the supply (or other input) terminals, the common-mode rejection ratio (CMRR) capabilities of the comparator may prevent performance perturbations; whereas, noise presented to either terminal, with respect to system ground, may cause havoc (see [Wide Bandwidth Input Signals](#)). Efforts should be made to ensure that noise, if it cannot be reduced further, is also seen by the other comparator inputs to take advantage of the CMRR. Of the ADC error sources, this is one of the most challenging to control in a practical and effective manner.

### Wide Bandwidth Input Signals

A certain way to disrupt ADC function is to give the wide bandwidth comparator something to respond to other than the input signal of interest. By designing the electronics feeding the ADC inputs to pass input signals having frequencies that range from dc to purple, ADC problems are usually guaranteed. Thus, this fourth area is a common source of ADC malfunction.

### Other Error Sources

Although occurring less frequently and more subtly, other error sources can also impact ADC performance: rate of conversion requests to a particular channel and interchannel charge-sharing. These sources and an estimate of the impact on a given M68HC11 system are presented in detail in the *M68HC11 Reference Manual*, Freescale document order number M68HC11RM/AD.



## Real-World Example

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When discussing the mechanics of noise phenomena in MCU/ADC systems, it is very difficult to understand how large the noise problem is, how well it is expected to respond to corrective action, and how closely the analysis matches the real world. To help resolve these problems, an actual troubleshooting session involving an M68HC11-based assembly is presented.

The subject assembly, an industrial controller, is a typical MCU/CPU installation utilizing the M68HC11 in expanded multiplexed (CPU) mode. The customer designed the program memory to expand to 32 K x 8, RAM to 2 K x 8, an external address decoder, some additional digital I/O lines, and analog buffers feeding the ADC inputs. Built on a 6-layer PCB, the assembly had the benefit of separate ground and voltage planes and was designed to be placed in a Faraday shield providing electromagnetic compatibility. This assembly was designed without the aid of any of the concepts presented in this application note. Understandably, the customer was having difficulty with ADC performance.

### The Problem

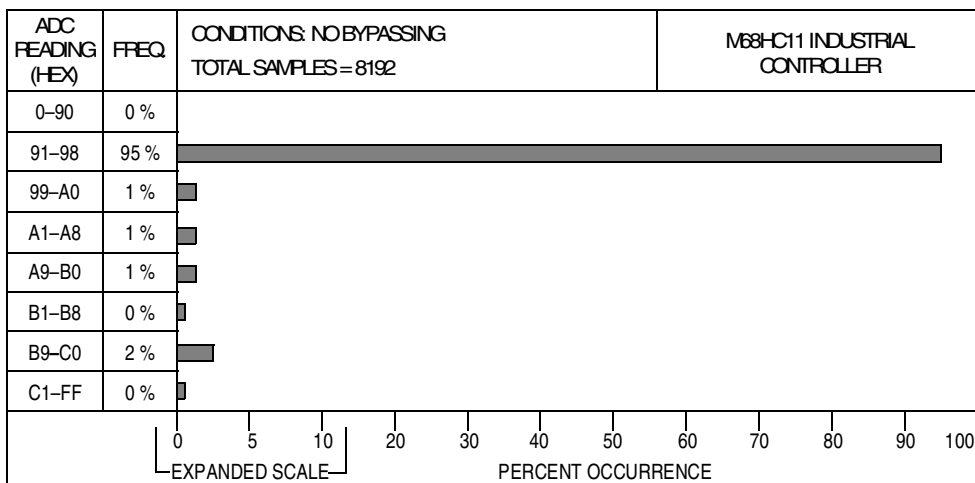
Functionally, the ADC noise problem manifested itself as an extreme shutdown condition in the final product. Since this assembly provides control to industrial equipment, conditions sensed by this controller could indicate dangerous conditions, which must be dealt with by severe and swift action, including functional shutdown of the controlled equipment. To achieve the safest response times and largest safety margins to such stimuli, the software designers of this system required 64  $\mu$ s continuous conversions ( $> 15$ -kHz sampling frequency). Once they were run through part of the designer's algorithm, the conversion results could not deviate more than  $\pm 2$  counts from the actual system ADC measurements. The M68HC11 was selected for this application because of its high level of integration as well as the  $\pm 1$  least significant bit (LSB) 8-bit ADC performance.

Errors many times this specification were encountered in the application. Unfortunately, evaluation of the extent of the ADC errors concerned only functional operation of the assembly and manual inspection of ADC values read with an in-circuit emulator, making the problem more serious. An attempt by the hardware engineers to reduce the noise by changing the bypassing scheme yielded no apparent change in the pattern of product shutdown. In this case, the lack of quantitative data convinced the engineers that they had no control over the problem, diverting attention from the actual cause.

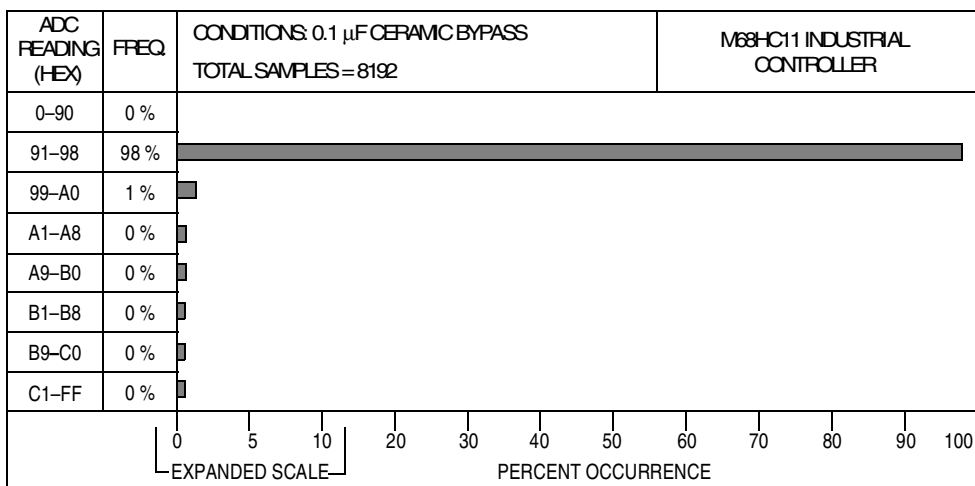
When dealing with these types of problems, always instrument the problem correctly — that is, ensure measuring techniques used to observe the malfunction by following these guidelines:

1. Quantify the A/D conversion process with regard to frequency of occurrence and magnitude of error.
2. Ensure that the measurements are with sufficient resolution so that minute improvements or degradations in performance may be monitored and evaluated.
3. Ensure that the number of observed conversions is similar to product usage or is statistically significant to allow inference from the measured sample to actual product operation.

Had the assembly been properly monitored, an improvement in ADC performance with the different bypassing scheme would have been evident (see **Figure 8**). These two histograms display ranges of A/D conversion values on the vertical axis and the hit rate (percent of total readings landing within the boundaries of the selected ADC reading range) on the horizontal axis. As shown, there was approximately a 3 percent improvement in the number of correct A/D conversions with new bypassing. To detect these changes, the EPROM on the controller PCB was probed with a fairly simple logic analyzer. The logic analyzer was then configured to trigger on accesses to a location in memory containing the results of A/D conversions. By utilizing the simple statistics options given by the analyzer, each quantitative improvement in ADC performance was observed.



**(a) No Bypassing**



**(b) Improved Bypassing**

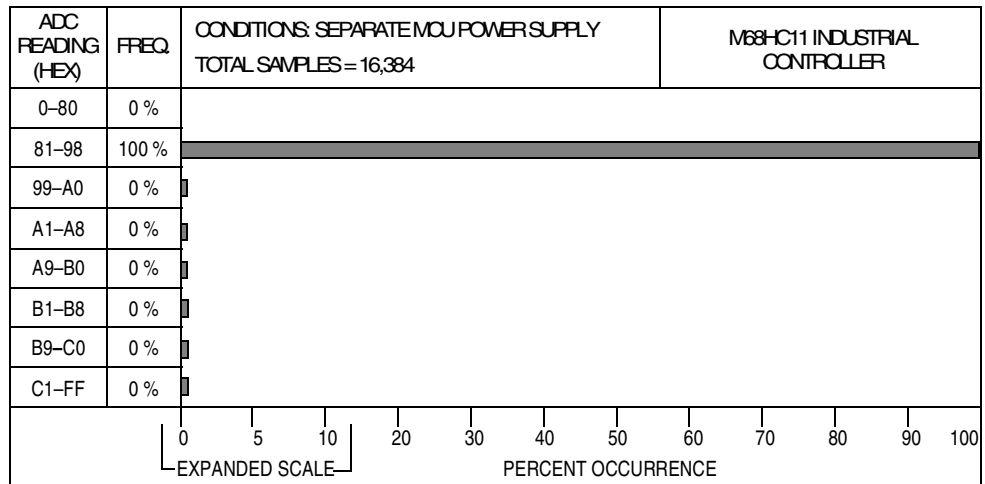
Note: Readings are rounded to nearest 1% value. Columns with 0% and a grey bar imply >0% and <0.5%.

**Figure 8. Effect of Bypassing Only**

## The Perfect Circuit

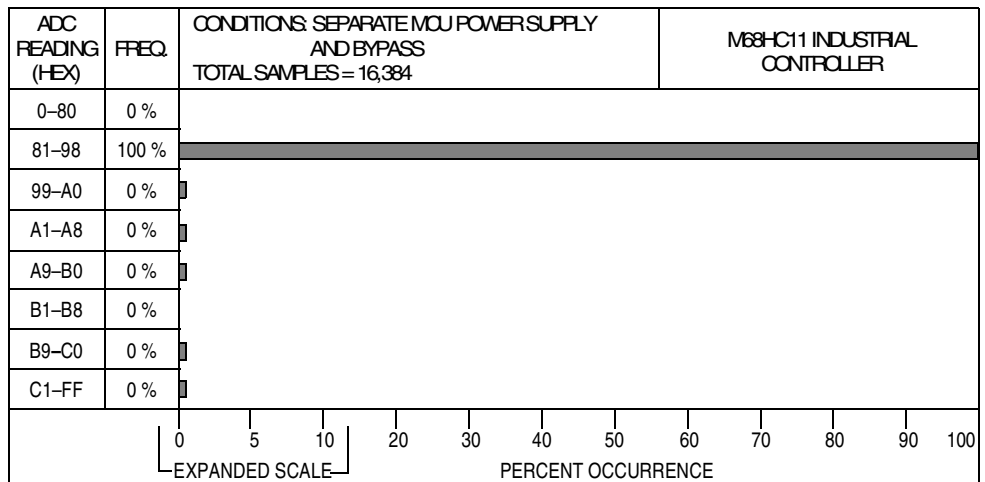
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After sufficiently instrumenting the offending assembly, the next step is to attempt to duplicate ideal operating conditions for the MCU/ADC. Since every M68HC11 is 100 percent tested for ADC performance before leaving the factory, in the absence of externally induced failure, the M68HC11 should maintain factory performance given identical operating conditions. By operating the M68HC11 in near perfect conditions, the engineer learns if the failure is or is not parts related. The motivating factor for this case, however, concerned  $1 V_{PP}$  noise (spaced in time at approximately the E-clock rate of the M68HC11) found when measuring  $V_{DD}$  at the pins of the M68HC11. Given what is known about the ADC comparator, it was best for system performance to reduce this  $V_{DD}$  noise as much as possible. The noise was reduced by isolating the power busing to the M68HC11 only. The PCB foil was cut to  $V_{DD}$ ,  $V_{SS}$ ,  $V_{RL}$ , and  $V_{RH}$  leading to the M68HC11. Discrete wires were then run directly to an external laboratory-grade power supply. With this configuration, measurements were taken as before. The results of these measurements are shown in **Figure 9**. As the graph shows, an improvement was made over the non-bypassed assembly. Instead of a 5 percent error in the ADC readings, less than 0.5 percent of the readings were outside of the expected range. Also evident in **Figure 9** is the presence of full-scale errors as before. At this point, a bypass capacitor was soldered between the M68HC11  $V_{DD}$  and  $V_{SS}$  pins. The resulting measurements, shown in **Figure 10**, are an apparent improvement over the previous non-bypassed assembly. However, due to the granularity of the measurement reported by the logic analyzer, it cannot be stated quantitatively how much the bypassing improved the condition. Further manipulation of the bypassing network failed to improve the readings in a discernible manner.



Note: Readings are rounded to nearest 1% value. Columns with 0% and a grey bar imply >0% and <0.5%.

**Figure 9. Separate MCU Power Supply**

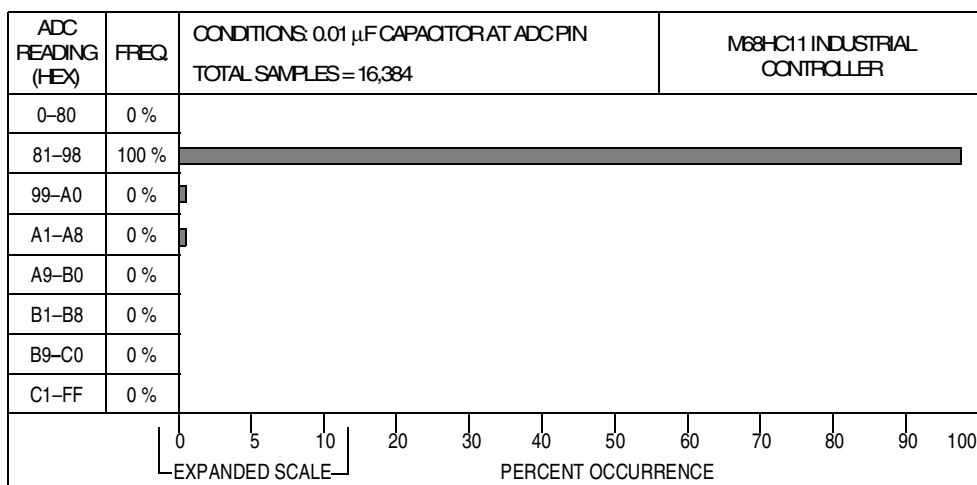


Note: Readings are rounded to nearest 1% value. Columns with 0% and a grey bar imply >0% and <0.5%.

**Figure 10. Separate MCU Power Supply with 0.1  $\mu$ F Bypass**

At this point, only power distribution buses had been manipulated to reduce ADC errors. Another part of the ADC circuit manipulated to yield some improvement was the linear portion interfacing the MCU to the various input signals. Consisting of 324-type opamps operated at unity gain, this linear buffer provided a low-impedance source for the ADC input multiplexer. Although not usually considered a wideband opamp, it proved too wideband for this system. Most data coming from the devices

feeding the 324 buffers were slowly varying dc or signals with frequencies below 500 Hz. Yet, the full bandwidth of signals allowed by the buffer passed unaltered to the ADC inputs. This manipulation violated a design guideline that urges the designer to tailor the bandwidth of each ADC channel to the bandwidth of the input signal. By properly filtering the input to the ADC, frequencies that may prove troublesome if left unfiltered will not be allowed to pass to the ADC input. To test the effect of this guideline on this specific industrial controller, 0.01  $\mu$ F capacitors were soldered to the ADC input pins at the M68HC11. The measurements taken with this configuration (see **Figure 11**) showed significant improvements. As shown in **Figure 11**, there were still occasional occurrences of out-of-spec ADC readings.

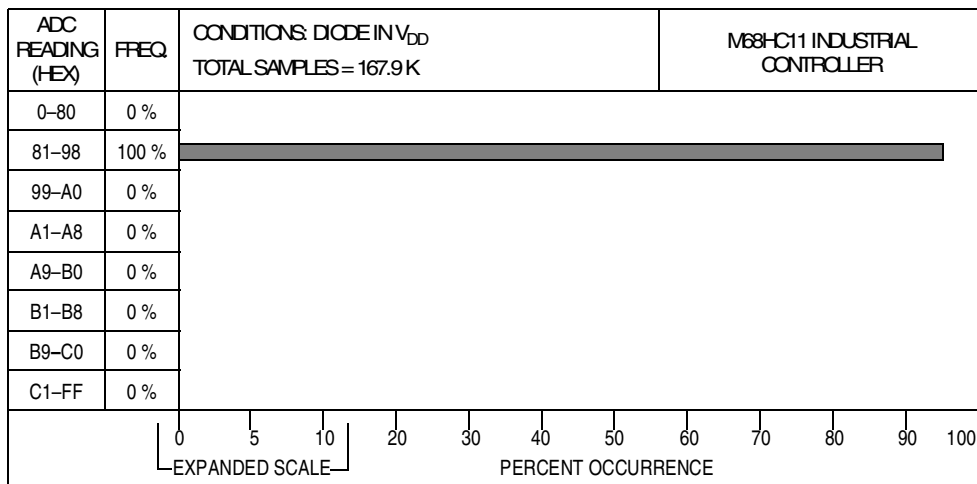


Note: Readings are rounded to nearest 1% value. Columns with 0% and a grey bar imply >0% and <0.5%.

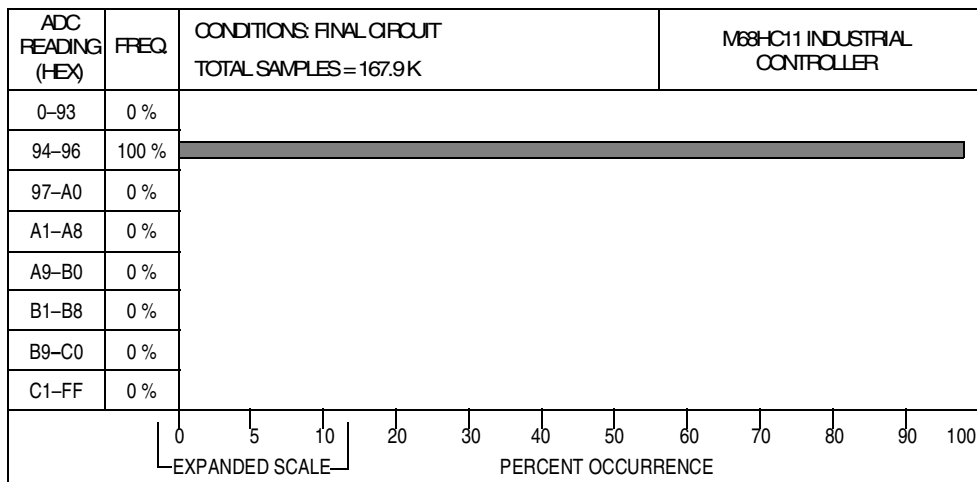
**Figure 11. Capacitor on ADC Pin**

In the absence of other guidelines, the only choice left to achieve specified ADC performance was to refine the implementation of the existing guidelines. The second guideline, duplicate ideal operating conditions, is usually the most likely candidate for improvement. One of the corollaries to duplicating ideal operating conditions is reducing unwanted interaction between adjacent circuit segments. In this case,  $V_{DD}$  noise had not been completely eradicated. Rather than inserting a local IC regulator for just the M68HC11, an alternative method of  $V_{DD}$  isolation was attempted: a series diode with  $V_{DD}$  forming a peak detector

with the bypass cap. Out-of-spec ADC errors were totally eliminated (see **Figure 12(a)**). To check the thoroughness of this last circuit fix, the range of sensitivity for the ADC result range of interest was changed on the logic analyzer. By changing the range to show values between  $(94)_{16}$  and  $(96)_{16}$ , inclusively, the  $\pm 1$  LSB spec could be observed directly. The results of this measurement run are shown in **Figure 12(b)**.



**(a) Diode in  $V_{DD}$**



**(b) Tightened ADC Range**

Note: Readings are rounded to nearest 1% value.

**Figure 12.  $V_{DD}$  Diode and Tightened ADC Range**

## Application Note

### Summary

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The highly integrated MCU can be a cost-effective design tool. With the breadth of MCU choices available to the circuit designer these days, analog circuit functions may now often be implemented by MCUs with integral ADCs. By following the practical guidelines presented in this application note during the design phase, the MCU-based product design using the on-chip ADC can achieve its full cost-effective potential.

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Tokyo 153-0064  
Japan  
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