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Application Note

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MPC5744P Startup STCU Overview

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1. Introduction

The purpose of this document is to give the user an overview of the default configuration of the Self-Test Control Unit (STCU) when running the Startup Built-In Self-Test (BIST) and the memory and logic partitions testing during a BIST. Details on how to enable/disable the Startup BIST are included as well as the default fault handling configuration.

Contents

2. Memory Partitions

Table below shows the different memory partitions that are tested during the MBISTs.

Table 1. MBIST mapping

Partition Number	Memory Partition
0	BAM ROM
1	DMA RAM
2	System RAM 1
3	System RAM 0
4	System RAM 3
5	System RAM 2
6	System RAM 5
7	System RAM 4
8	DLMEM 1
9	DLMEM 0
10	iCache Data Memory 3
11	iCache Data Memory 2
12	iCache Data Memory 1
13	iCache Data Memory 0
14	iCache Tag Memory
15	dCache Data Memory 3
16	dCache Data Memory 2
17	dCache Data Memory 1
18	dCache Data Memory 0
19	dCache Tag Memory
20	FlexCAN RAM 2
21	FlexCAN RAM 1
22	FlexCAN RAM 0
23	FlexRay LRAM 1
24	FlexRay LRAM 0
25	FlexRay DRAM
26	ENET Memory

3. Logic Partitions

Table below shows the different logic partitions that are tested during the LBISTs. This table only shows the central, definable logic blocks. The LBIST also tests glue logic.

Table 2. LBIST mapping.

LBIST number	Device partition	Logic Partition
0	**C0**	z4 Main Core_0, PFLASHC, Flash memory, NPC, NXMC0, NXMC1, MEMU
1	**C1**	z4 Checker Core_0s, RCCU, CMU1
2	**P0**	DMA_CH_MUX0, FlexRay, WKPU, MC_ME, MC_PCU, SIUL2 IO-muxing logic, CRC, PIT, DSPI0, DSPI1, LIN1, FlexPWM1, eTimer1, CTU1, SENT0, SIPI, LFAST, BAM, FlexCAN0, FlexCAN1, FlexCAN2, ADC1, ADC3, ENET
3	**P1**	DMA_CH_MUX1, FCCU, FOSU, CMU0, CMU2, CMU3, CMU4, DSPI2, DSPI3, SGEN, LIN0, FlexPWM0, eTimer0, eTimer2, CTU0, SENT1, ADC0, ADC2

4. Startup BIST Configuration

The BIST will test both memory and logic partitions, and when executed, the test will finish execution within a specific time frame shown below. By default, the startup BIST is enable and will execute. It is not possible to disable the BIST engine which is running during startup but there is possibility to disable MBIST and LBIST tests (patterns), a single Device Configuration Format (DCF) record should be written to the UTEST area. When the BIST is enabled, the BIST will execute after a Power On Reset (POR), a destructive reset, or an external reset (if triggered as long-functional reset). The default configuration meets the ASIL D requirements.

4.1. Clock Settings

The BIST for MPC5744P assumes the device is using a 16 MHz IRC to source the Phase-Locked-Loop (PLL). The clock divider (MC_CGM.SC_DC0.R = 0x80030000) sets the STCU frequency to 50 MHz.

STCU Clock Source and Frequency : 50 MHz (derived from PLL @ 200 MHz)

PLL Source : IRC 16 MHz

4.2. Memory Built-In Self-Test (MBIST)

MBIST is implemented for each of the memories on the MCU listed in Table 1, including memory contained in the peripheral modules. For MBIST testing purposes, each of the memories is segmented into individual MBIST partitions. The MPC5744P implements 27 memory partitions, and each partition has an individual MBIST controller. The STCU controls the MBIST execution of all partitions.

The MIBST uses one of three test modes, Diagnostic, Long self-test, and Normal self-test. The Diagnostic Mode tests all memories with the full RAM and ROM algorithm. The Long self-test Mode tests all memories with the reduced RAM and ROM algorithm. The Normal self-test mode tests all memories with a checkerboard/inverted checkerboard algorithm.

It is only possible to use Normal Self-Test Mode for the MPC5744P in startup mode. The other modes can be used only in shutdown mode.

Algorithm Used	:	Auto test MBIST algorithm (normal mode)
Partitions Tested	:	MBIST 0-27 concurrently

4.3. Logic Built-In Self-Test (LBIST)

The LBIST tests operate on the digital logic of the device and uses scan test techniques to provide high coverage defect detection. The logic is divided up into multiple partitions, with each partition containing multiple user recognizable logic modules. The MPC5744P implements 4 logic partitions where in first step run concurrently C0 and P1 and in next step run concurrently C1 and P0 to minimize execution time and current consumption. All LBIST partitions are tested when BIST is enabled.

Partitions Tested:

- Step: LBIST 0 (partition C0), and LBIST 3 (partition P1) concurrently
- Step: LBIST 1 (partition C1), and LBIST 2 (partition P0) concurrently

Stuck-at coverage: 90%

4.4. Worst Case Execution Time

LBIST	:	10.5 ms
MBIST	:	4 ms
Overall	:	15.545 ms

4.5. Disable MBIST and LBIST tests during startup BIST

To disable MBIST and LBIST tests during startup BIST, the user must write 0x7F0000000008000C to the first open UTEST memory address. If no other DCF records have been written to the UTEST area, the first open UTEST memory address should be 0x0040_0218.

DCF records:

Enable Startup BIST	:	0x0000_0301_0008_0000 //By default – enable STCU module 0x1210_0008_0008_000C //Enable all BIST test
Disable Startup BIST	:	0x7F00_0000_0008_000C //Disable all BIST tests

CAUTION

The UTEST flash memory is one time programmable (OTP) memory on MPC5744P. It means that what is one time programmed It is not possible to change.

5. Fault Handling

Any faults that occur during the startup BIST are set as non-critical faults. After the execution of the startup BIST, the user can check the STCU2 error register (STCU2_ERR_STAT) for any errors that might have occurred. The Non-Critical Faults Status Flag (STCU2_ERR_STAT [NCFSF]) will indicate if a non-critical fault did occur. If a fault did occur, the user can check the STCU2 status registers to determine where the fault occurred; STCU2 Startup LBIST Status Register (STCU2_LBS), and STCU2 Startup MIBST Status Low Register (STCU2_MBSL).

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