Document Number: FXAS21002CER
Rev. 0.1, 5/2015

Errata for FXAS21002C

This errata sheet describes the functional problems known at the release date of this document.

Revision History

Rev	Date	Description
0	2/3/2015	Added E1: SPI Multipoint Communication
0.1	5/1/2015	E1 Fix Plan, Changed the date from WW19'2015 to WW32'2015 (2 places)

Contents

1 Part Identification

The following errata affect the behavior of all production FXAS21002C devices.

2 Errata

2.1 E1: SPI Multipoint Communication

Problem

FXAS21002C does not support *multi-point* 4-wire SPI communication protocol (multiple slave devices on the bus).

FXAS21002C, when connected for a 4-wire SPI communication with the master, does not tri-state the MISO line when the SPI_CS_B (SPI chip select, Active low) pin is deasserted (logic high). This leads to a bus conflict if there are multiple devices on the same SPI bus. As the part pulls MISO down to GND, instead of tri-stating, this part blocks the other slave devices on the bus from sending data to the master by means of 4-wire SPI communication.

Workarounds

Three possible workarounds are associated with the erratum.

Workaround 1

Add a tri-state buffer with the MISO line and the SPI_CS_B line as inputs to the buffer (see Figure 1).

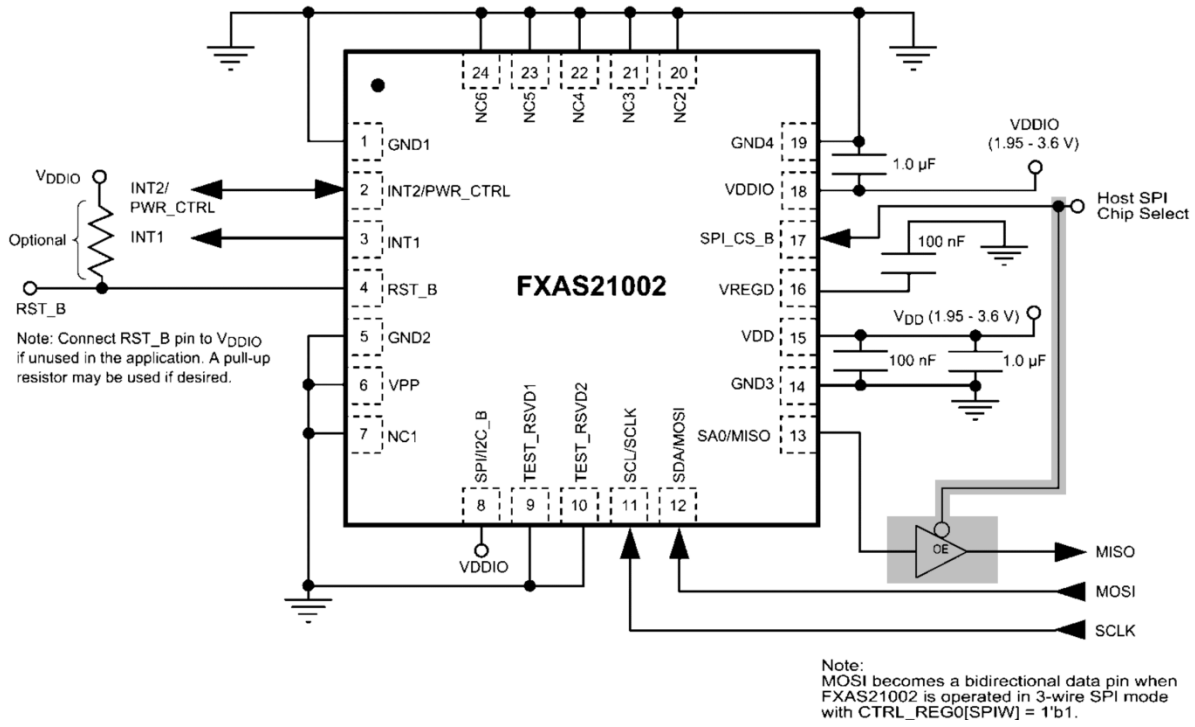

Figure 1. Typical application circuit with addition of tri-state buffer

Workaround 2

Use I^2C communication instead of SPI 4-wire communication as the part's I^2C communication works as expected with multiple slave devices on the bus.

Workaround 3

Use 3-wire SPI communication with FXAS21002C and all other slave devices on the SPI bus.

If the device is connected and configured to operate in 3-wire SPI mode, it works as expected with multiple slave devices on the bus with the only condition that all slave devices on the bus must be connected for a 3-wire SPI communication with the master. In this configuration, FXAS21002C's SA0/MISO pin must be left unconnected.

Fix Plan

A fix for *E1: SPI Multipoint Communication* is planned.

An ASIC revision is planned for the first half of 2015. Parts not subject to this errata will be identifiable by means of a clean date code currently targeted for WW32'2015. All material manufactured WW32'2015 and later will not be subject to this errata.

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