NXP Semiconductors
Design Reference Manual

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Power-Line Communication Module for CENELEC Band

1. Introduction

The Power-Line Communication (PLC) is becoming more and more popular. The distribution network serves not only to supply electric energy, but also as a communication channel. The growth of green-energy sources' deployment creates a need to measure and control the distribution network dynamically. This drives a constant push to the PLC development.

There are several different protocols that compete in the CENELEC band (9 kHz to 95 kHz) in Europe, mainly Prime and G3. They have several versions and are being improved continuously. On one hand, the protocols are quite similar as they use the OFDM modulation for physical layer, but, on the other hand, they differ in the number of subcarriers, sample rates, and the forward error-correction calculation.

The G3 physical-layer sampling frequency is 400 kHz, and uses 256 samples for the FFT calculation.
The subcarriers used for the communication are the numbers from 23 to 58, in the frequency range of 35.9 kHz to 90.6 kHz. The data is encoded by the DBPSK or DQPSK modulations, and protected by the convolutional and the Reed Solomon codes.

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The PRIME protocol uses a sampling rate of 250 kHz with 512 samples for FFT calculation. The subcarriers used for the communication are the numbers from 86 to 182, in the frequency range from 42 kHz to 89 kHz. The data is encoded by the DBPSK, DQPSK, and D8PSK modulations, and can be protected by the convolutional code.

Although these protocols seem to be similar, there is a difference in the CPU time needed to process the PHY and MAC layers, mainly in the FEC and RS calculation. Both protocols can be demodulated on the ARM® Cortex®-M4 core, while G3 requires more CPU time to do so than PRIME.

There are many variants of higher layers above the PHY and MAC layers, such as IPv4, IPv6, or DLMS COSEM. Each protocol has a different memory footprint for both the RAM and FLASH sizes.

Due to the above-mentioned facts, it is clear that customers need a flexible approach to PLC to easily adapt their products to their actual tenders. It is ideal to use the software-defined communication and choose the right product from the broad NXP portfolio of Cortex-M4 MCUs. The NXP portfolio offers a broad scale of Cortex-M4 MCUs with regards to performance and memory size that are pin-to-pin compatible.

The MK26FN2M0VLQ18-based PLC module is designed to enable you to develop, tweak, test, and certify your products before you finish the hardware. NXP partners with the PLC stack developers where the module is ideal piece of hardware to be used for development.

The MK26FN2M0VLQ18 MCU is powerful enough to handle both mentioned protocols and offers 2 MB memory, which fulfills the higher layers' needs. It is then simple to migrate to lower-performance MPUs that are pin-to-pin compatible. The module uses the NCS5651 line driver from ON Semiconductor with whom NXP partnered in the development of the board.

The module is intended to be used for PLC in the CENELEC band (30 kHz to 95 kHz) and for low-voltage systems (120/230 V AC). The module uses a transformer for galvanic isolation from the mains to make the development easier.

The following figure shows the top and bottom views of the module.

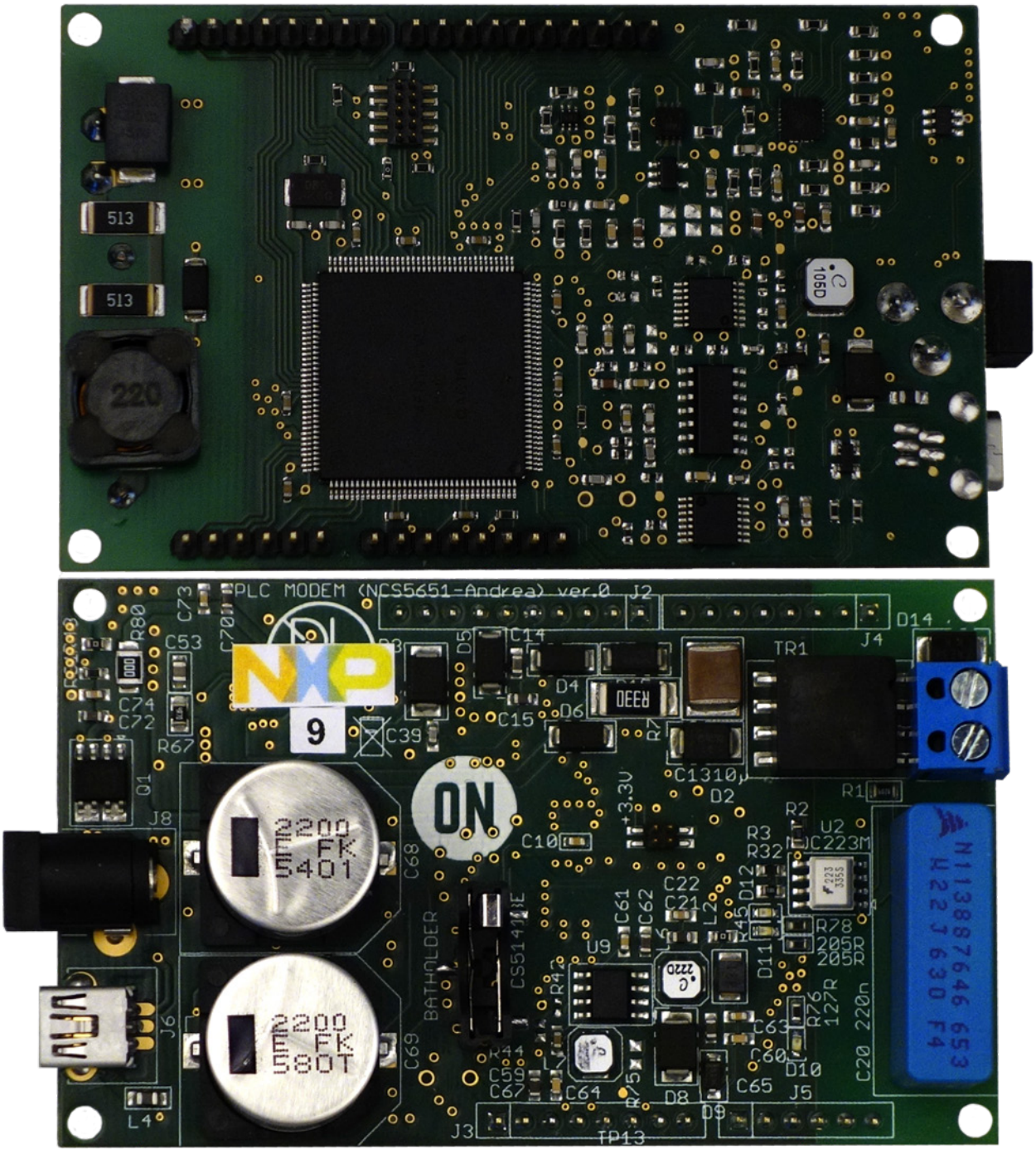

Figure 1. PLC module (top and bottom views)

2. MCU

The module uses a high-performance Kinetis K family ARM Cortex-M4 MCU. The MCU has these features:

- The CPU runs at 180 MHz, and contains the ARM Cortex-M4 core with DSP instructions and a single-precision floating-point unit.
- The MCU contains up to 2 MB program flash memory with 256 KB RAM.
- The MCU contains two 16-bit SAR ADCs with sampling speeds of up to 1 Msps.
- The MCU contains two 12-bit DACs.
- The voltage reference is 1.2 V.
- The MCU contains four analog comparators (CMPs), together with a 6-bit DAC.

3. PLC Module Topology

The module adopts the Arduino shield form factor. The side connectors follow the Arduino pinout, and contain the power-supply input, analog inputs, GPIOs, UART, Timer, I^2C, and SPI. Moreover, there is a jack connector for a 12 V @ 3 A DC power supply, a power-line connector to communicate over the mains (230 V AC maximum), and a USB connector.

The hardware is galvanically isolated from the mains by a transformer to lower the risk of high-voltage injury or damage of development tools (such as JTAG or a notebook). Follow the safety rules when connecting the device to the mains.

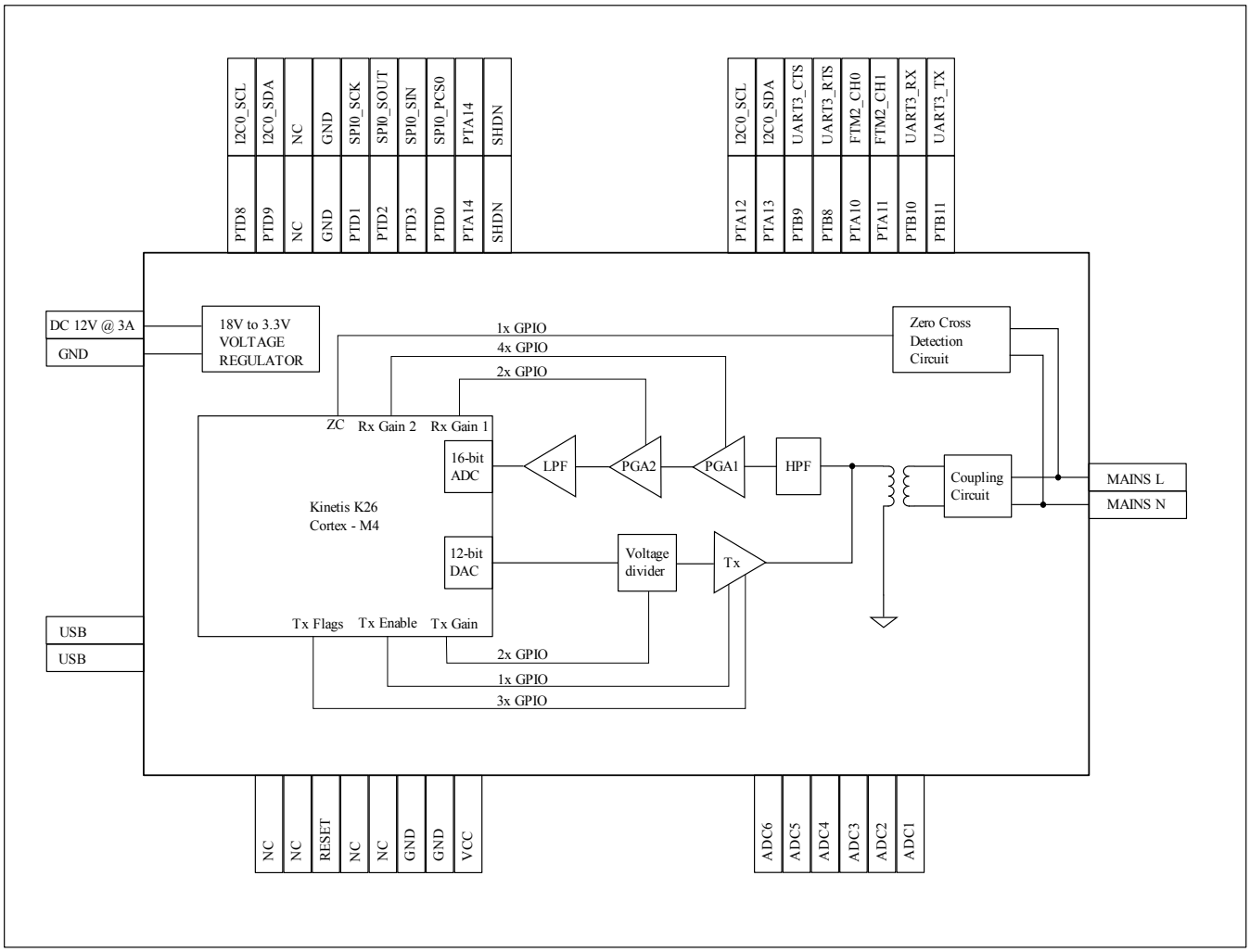

Figure 2. PLC module topology

In the module, there are complete transmit/receive circuits, based on a standard operational amplifier for the receiver path, and the NCS5651 line driver for the transmitter path. There are filters tuned for the CENELEC 50065 band (35 kHz to 95 kHz) in both paths.

The receiver also contains two PGA modules to adjust the received signal to the AD converter voltage level. The module uses the DA and AD converters integrated in the Kinetis K26 MCU; the remaining modules are of pure analog design. Due to a high ADC and DAC accuracy, you do not need to use any external converters.

In the transmitter signal path, there is a voltage divider for decreasing the output voltage without compromising the DAC output signal quality.

The coupling circuit filters out the 230 V AC, and contains many protection components to remove the spurious over-voltage.

The buck voltage regulates 12 V to 3.3 V to power the MCU and transmitter logic circuits.

4. MCU

The MCU uses the JTAG debug interface to load and debug code. There is a J7 connector assembled on the board, and has the TCLK, TDI, TDO, TMS, and RESET signals. The 8-MHz crystal oscillator provides a clock source that can be multiplied by the internal PLL up to 180 MHz.

There are two LED diodes that are directly controlled by the PTB0 and PTB1 GPIO pins.

Table 1. LED diodes

Pin number	Name	LED
81	PTB0	D11
82	PTB1	D12

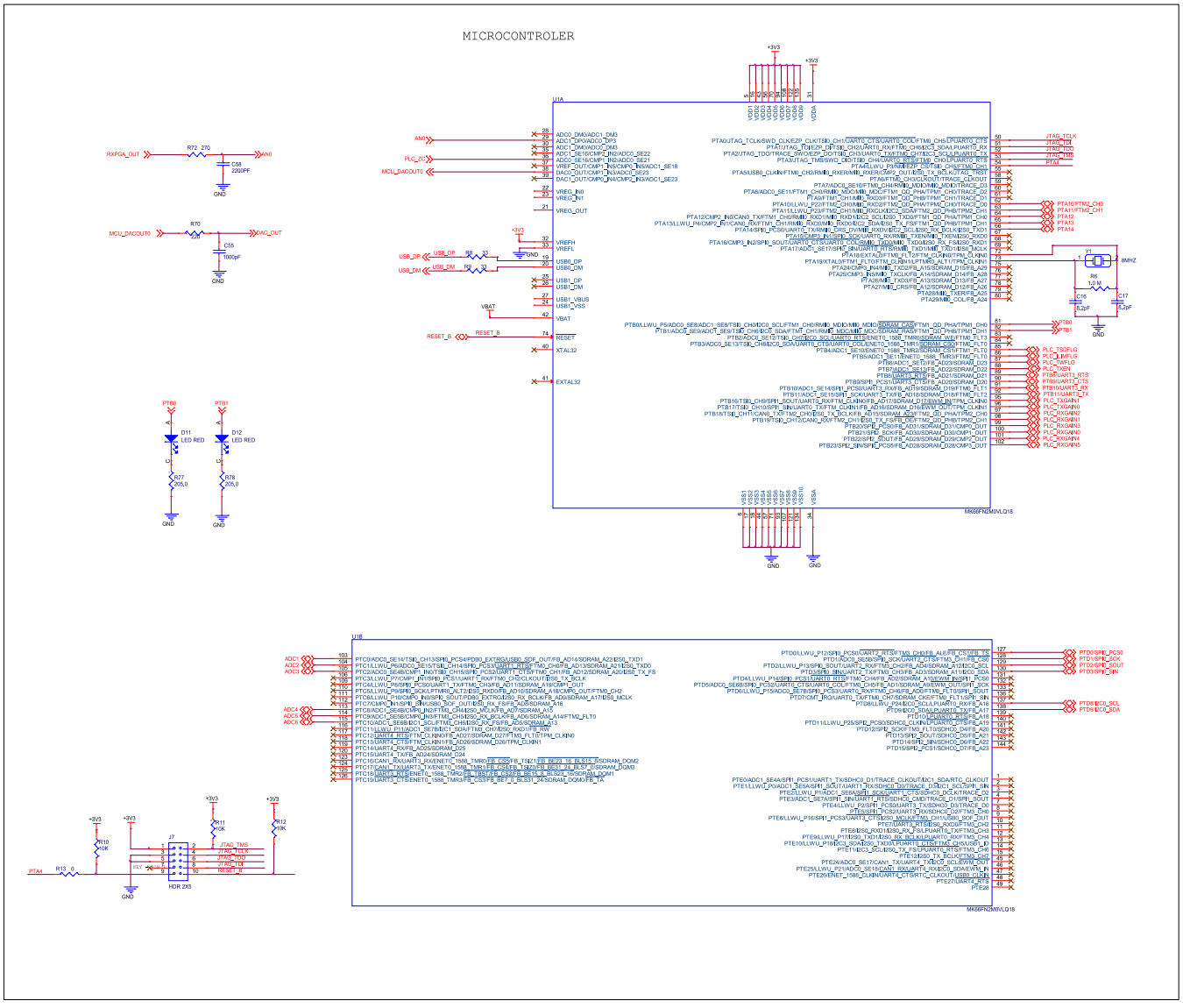

Figure 3. MCU digital part schematic

5. Transmitter

The purpose of the transmitter is to amplify the transmit signal generated by the MCU DA converter. The transmitter must have a good current-feeding capability to transmit to the low-impedance line. A good signal harmonic distortion is essential to achieve the purity of the communication channel. NCS5651 is a high-efficiency, Class A/B, low-distortion power-line driver. The device consists of two operational amplifiers (OpAmps), with one acting as a pre-amplifier, and the other as a line driver. NCS5651 has a power-supply voltage ranging from 6 V to 12 V.

The output OpAmp is designed to drive a peak of up to 2 A into an isolation transformer, or a simple L-C coupling to the mains. At the output current of 1.5 A, the output voltage has only 1-V drop from the positive/negative rails.

In addition to the output amplifier, a small-signal OpAmp is provided. This OpAmp can be configured as a unity-gain follower buffer, or to provide the first stage of a 4-pole low-pass filter.

Both OpAmps have the Gain Bandwidth Product (GBP) high enough to work as filters. In the design, each amplifier forms multiple second-order feedback filters tuned to a cut-off frequency of 95 kHz.

Regarding the additional features, NCS5651 contains a current-limit circuit programmable with a single resistor, RLIM, and a current limit flag for signaling to the host processor.

The device provides two independent thermal flags with a hysteresis:

- A thermal warning flag to indicate that the internal junction temperature has reached a user-programmable thermal warning threshold.
- A thermal error flag to indicate that the internal junction temperature has exceeded 150 °C.

All the digital warning flag signals are connected to the host MCU GPIO, which has the interrupt capability to catch the event immediately.

The amplifier also provides the enable/shutdown functionality to control the line driver output and set the output to the Hi-Z mode during reception.

Kinetis K26 generates the transmit signal using the 12-bit DAC. It can run at 1 MHz, which fulfills both the PRIME and G3 protocol sampling rates. It provides high accuracy and low harmonics, and is compliant with the CENELEC 50065 disturbance limits. Together with a powerful core and the DMA channel, it forms an ideal base for a modem transmitter.

The electrical parameters are designed in such way that the output signal fulfills the CENELEC 50065 standard, and works on the low-level network (230 V @ 50 Hz or 120 V @ 60 Hz).

The transmitter analog path consists of these sub-blocks:

- Attenuator
- Amplifier
- Protection circuit

5.1. Attenuator

The mains lines may have a very low impedance in the CENELEC band. Therefore, at the full signal voltage, the line driver may not be able to feed enough current to the line. In this case, the signal voltage must be lowered to limit the corresponding current. The attenuator decreases the transmitter output voltage level without compromising the DAC resolution. The attenuator uses a resistor divider and the IC1SW switch to decrease the output signal from the MCU DAC. The attenuator has four steps of attenuation: 0, 9, 15, and 17 dB. To avoid changes in the DC path, the voltage is divided to the 6 V bias rail (the same bias level the transmitter has). The DAC must keep a stabile DC bias as well (VDDA/2).

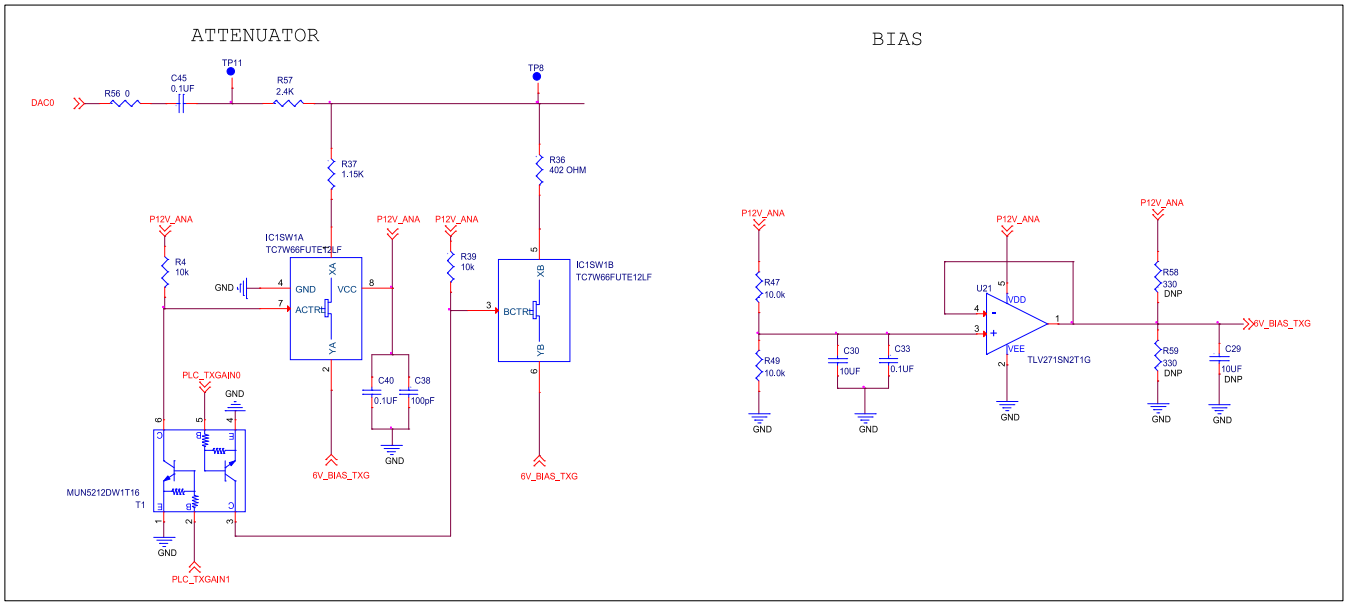

Figure 4. Transmitter attenuator schematic

The PLC_TXGAINx signals control the attenuator. The bias voltage is created by the R47/R49 voltage divider, and buffered by the U21 operational amplifier.

The attenuator is controlled by two digital signals (PLC_TXGAIN0 and PLC_TXGAIN1), connected to the IC1SW switch through the level shifter T1. See these two tables for the signal levels and the corresponding attenuation:

Table 2. Transmitter—PLC_TXGAINx attenuation control signals and corresponding attenuation

MK26FN2M0VLQ18 pins	PLC signal name	Signal logic state			
PTB17	PLC_TXGAIN0	0	0	1	1
PTB16	PLC_TXGAIN1	0	1	0	1
Attenuation	[dB]	0	7	13	15

The digital input electrical parameters are:

Table 3. Voltage levels of PLC_TXGAINx digital control signals

Digital VCC3V3 = 3.3 V	Input Low max [V]	Input High min [V]
PLC_TXGAINx	1.5	1.9

To limit crosstalk among amplifiers, the attenuator uses its own bias voltage (Vdd/2), built around the U21 OpAmp and the R47/R49 voltage divider.

The switching happens immediately. This figure shows the switching of attenuation from 15 dB to 0 dB:

Figure 5. Transmitter attenuation switching from 15 dB to 0 dB

5.2. Amplifier

The transmit amplifier is built around the NCS5651 PLC line driver (component U6). The line driver is capable of driving a peak current of up to 2 A into the isolation transformer TR1, with an output swing of 12 Vpp. The fourth-order low-pass Butterworth filter (multi-feedback topology) is formed around the amplifiers, and the cut-off frequency is set to 95 kHz.

Each gain stage has a gain of 9 dB, so the total gain is 18 dB. The maximum output voltage swing is 11 Vpp (on the output pins 8 and 9), provided that the power supply voltage P12V_ANA is 12 V. The input signal from the MCU is decreased by the filter input loss, and the loss on the attenuator (joined together by resistors R56/R36, R37, and R35). The input filter loss and the attenuation give a maximum input signal voltage from the MCU of around 1.8 Vpp. Therefore, the DAC must use the 3.3 V reference voltage to get a full-swing TX signal.

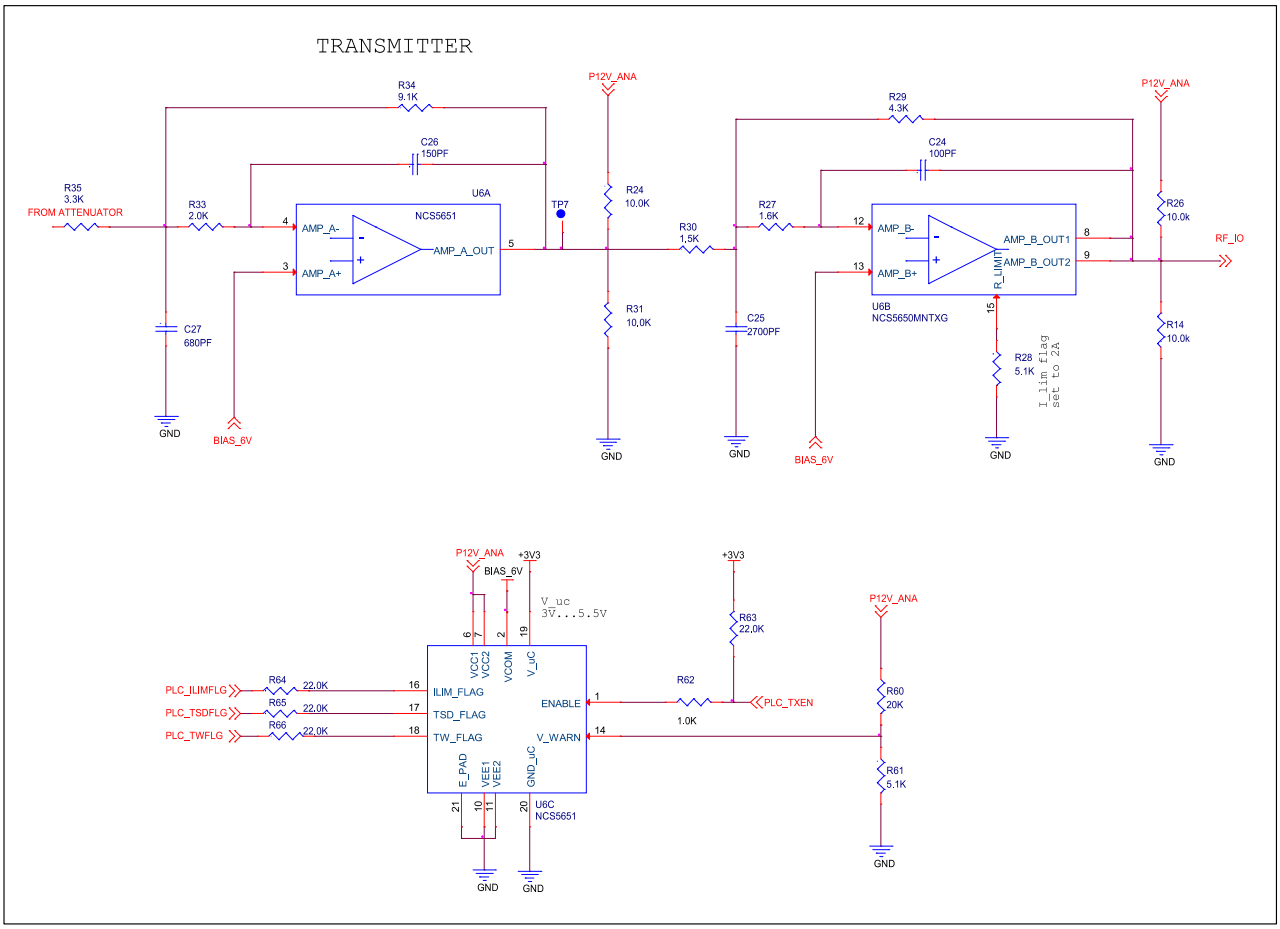

Figure 6. Transmit path amplifier composed of pre-amplifier U6A and line driver U6B

See the following table for the voltages on the amplifier stages. The R35 voltage corresponds to the attenuated DAC output, while the RF_IO voltage is the amplified signal after the last gain stage (output not loaded). The values in the table are valid for a 50-kHz signal.

Table 4. Transmitter voltage levels

Attenuation [dB]	R35 [Vpp]	TP7 [Vpp]	RF_IO [Vpp]
0	2.1	4.9	13 (limited)
7	0.9	2.1	6.88
13	0.48	1.1	3.4
15	0.38	0.9	2.6

The transfer function of the transmit path for four different attenuations is shown in the following figure. The input signal is 1.1 Vpp, generated from the signal generator Keysight 33600A. The output is measured at the artificial mains network L2-16, as described in the CELENCE EN50065 standard.

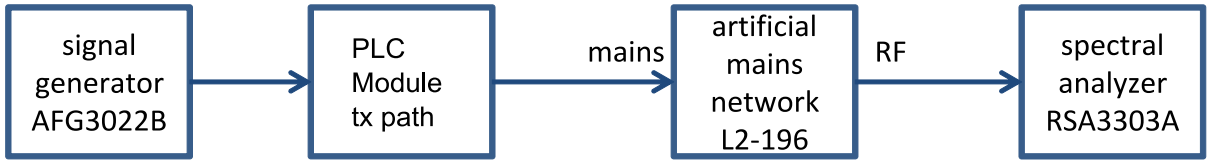

Figure 7. Measurement of transmit path and frequency response of PLC module

The Tx amplifier/filter transfer function is shown in the following figure. The signal generator output voltage is 1.1 V.

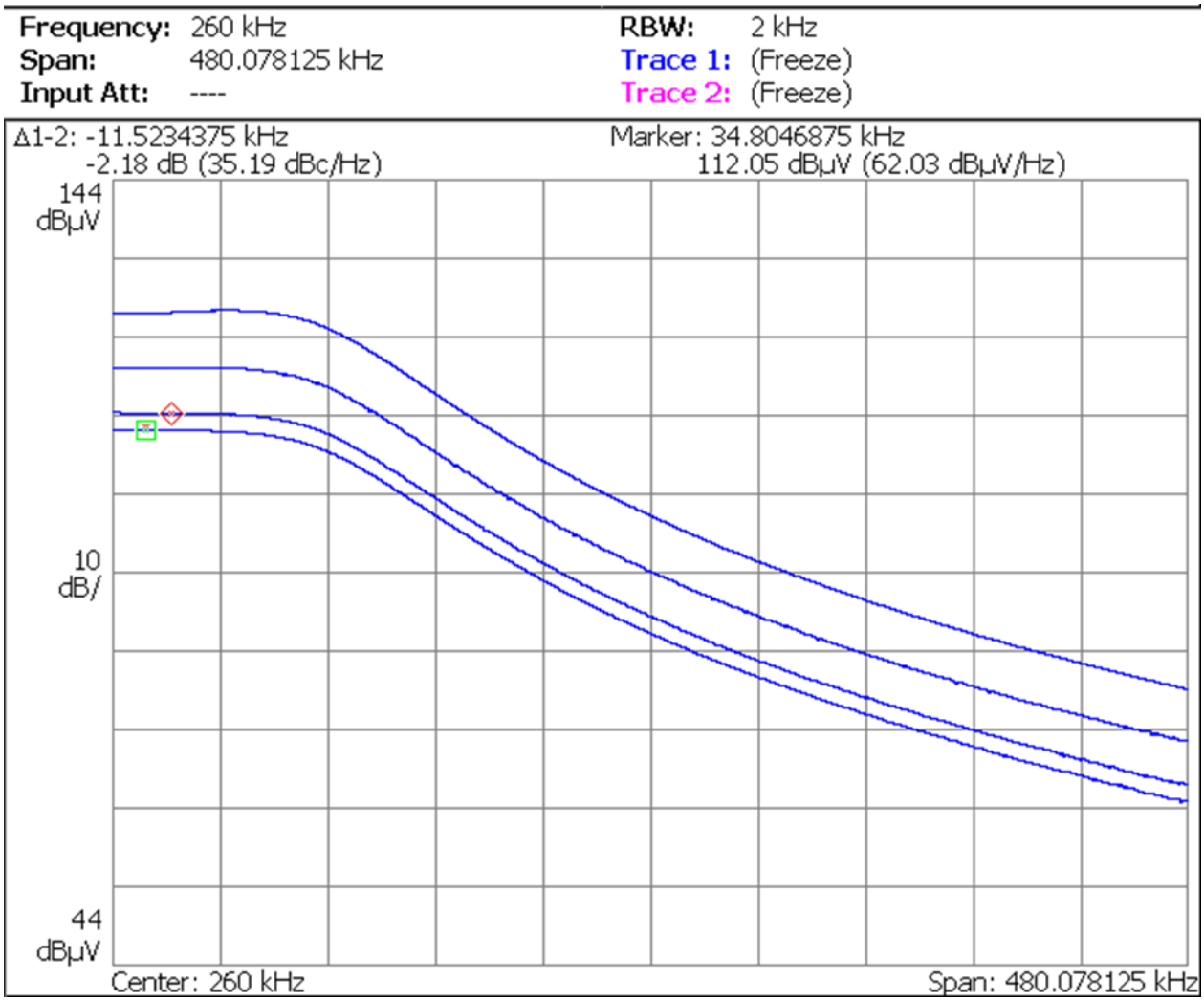

Figure 8. Transmitter attenuator and amplifier transfer function

6. Transmit Signal Harmonic Distortion

The CENELEC 50065 band specifies the bandwidth dedicated to electricity suppliers (9 kHz to 95 kHz), the maximum transmit signal levels, and the generated noise signal level within this frequency band. The signal is measured by a spectral analyzer on the artificial network with a defined impedance (CISPR 16-1:1993). For the wide-band signal, the maximum voltage level must not exceed 134 dBuV, and no part of the signal can exceed 120 dBuV (measured by a peak detector with RBW of 200 Hz).

The CENELEC 50065 standard defines the disturbance levels conducted to the artificial network.

The following figures show the signals generated the by the MK26FN2M0VLQ18 DA converter as an input to the TX amplifier NCS5651. The DAC reference voltage is 3.3 V, and the sampling frequency is 560 ksps. The DAC works in 75 % of the output voltage range.

The signal is measured by a spectrum analyzer with a RBW of 1 kHz. The signal is injected to the artificial mains network PMM L2-16.

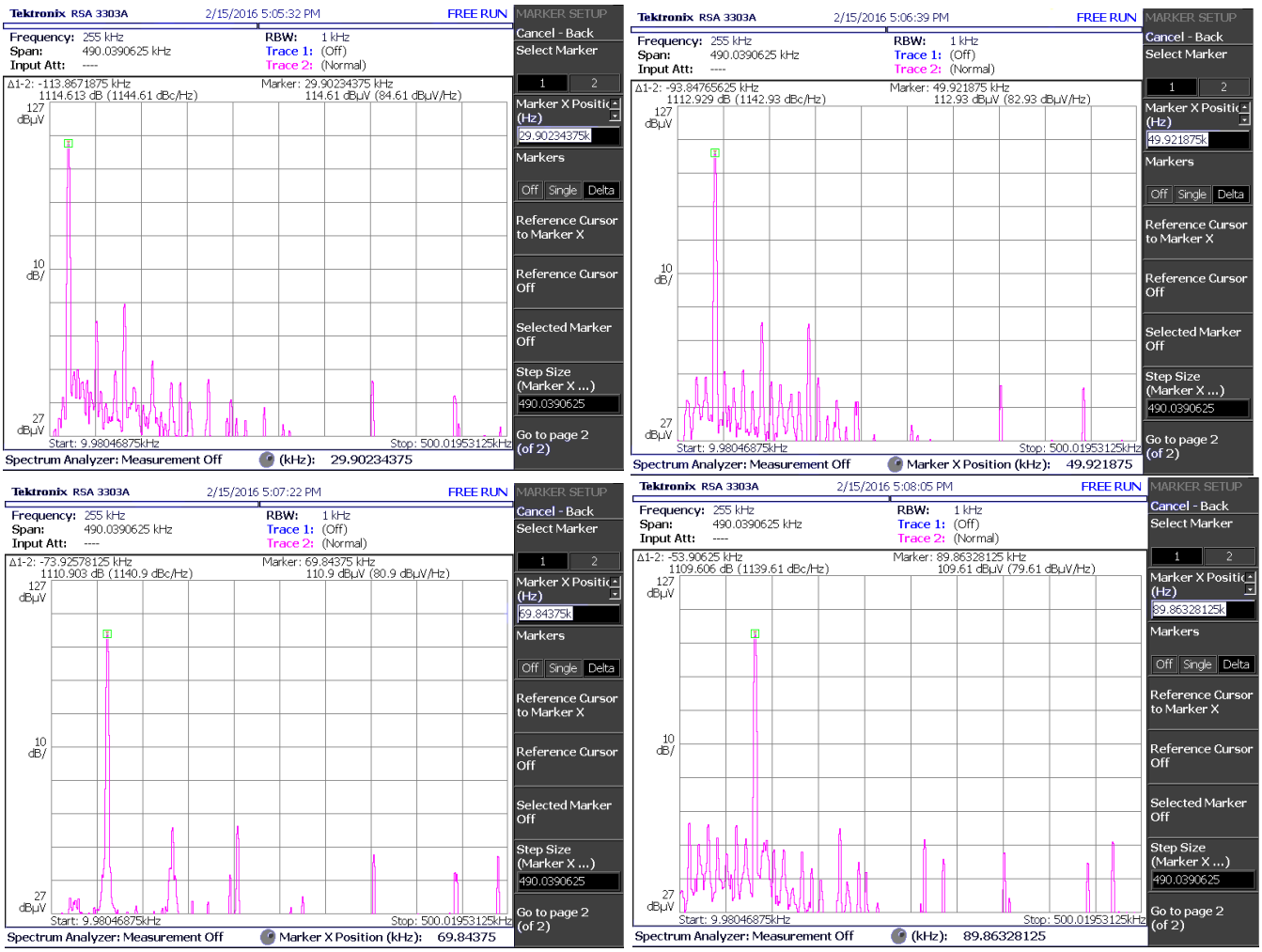

Figure 9. Transmit signal path—signal purity measurement

The signal is generated by the MK26FN2M0VLQ18 DAC, and amplified by the NCS5651 OpAmp. The measurement path is described in Figure 7, but the signal is generated by the MCU DAC.

7. Control Transmitter Amplifier

During reception, the transmitter amplifier U6 NCS5651 must be disabled, otherwise the received signal is short-cut. The amplifier is controlled by the PLC_TXEN signal, and when it is in the shutdown mode, the amplifier output goes into the high-impedance mode. If the PLC_TXEN signal is not driven by the MCU, the transmitter is disabled by the pull-up resistor R63 by default.

The device provides two independent thermal flags with hystereses. The thermal warning flag PLC_TW_FLG informs you that the internal junction temperature has reached the user-programmable thermal warning threshold (set to 105 °C by R60 and R61). The thermal shutdown flag PLC_TSD_FLG indicates that the internal junction temperature exceeded 150 °C and the device is shut down.

The current-limitation feature indicates that the output current reached the programmed maximum value. The maximum current is set to 2 A using resistor R28. When the current exceeds the programmed value, PLC_ILIM_FLG is set, and an action must be taken (e.g., decreasing the required output voltage).

Table 5. Transmitter control/flag signals

MK26FN2M0VLQ18 pins	PLC signal name	State and meaning	
		0	1
PTB5	PLC_ILIM_FLG	OK	Over-current
PTB4	PLC_TDS_FLG	OK	Shut down
PTB6	PLC_TW_FLG	OK	Temperature is above 105 °C
PTB7	PLC_TXEN	Enabled	Disabled

The transmitter amplifier switch-on/switch-off time is important due to a limited time between the packet reception and transmission. The transmitter amplifier ENABLE settling time is very short (below 10 μs), as shown in this figure:

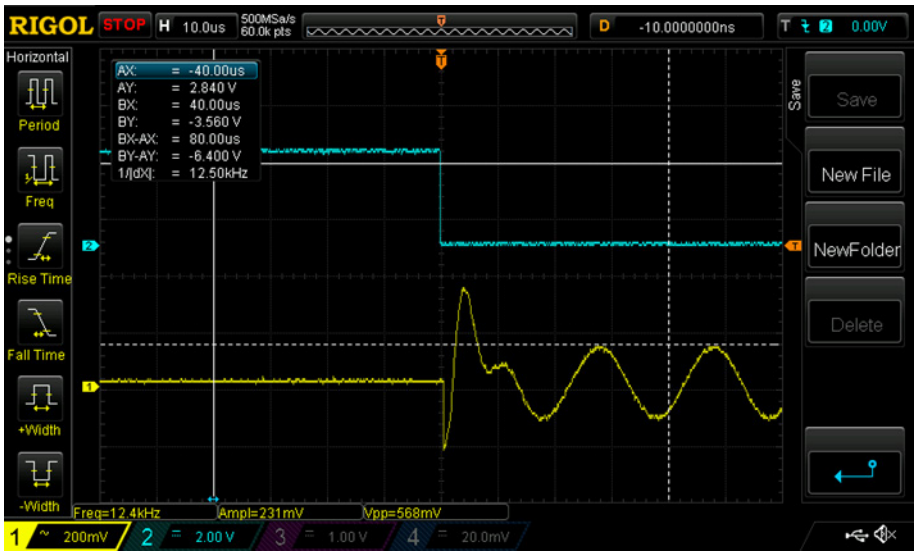

Figure 10. Transmitter amplifier ENABLE settling time

The blue line is the ENABLE signal. The yellow line is the transmitter output (AC-coupled).

8. Coupling Circuit

The coupling circuit connects the transmitter/receiver to the mains. The main purpose of the circuit is to remove the 120/230 V AC 50-Hz voltage to protect the low-voltage circuits of the communication module. The C20/L1 serial resonant circuit forms the band-pass filter, and attenuates the 50 Hz mains voltage. The resonation frequency is set to the middle of the communication band (~65 kHz).

The R19 varistor and the D14 TVS diode protect the coupling circuit from the over-voltage and various spikes in the mains. The TR1 transformer provides galvanic isolation from the mains.

The C13 capacitor removes the transmitter DC voltage signal, which would be short-cut on the transformer.

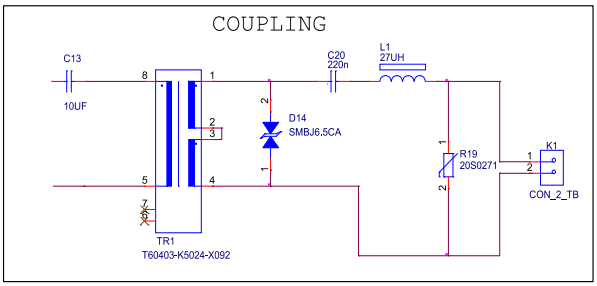

Figure 11. Coupling circuit

The coupling circuit is tuned to the center of the communication band to get a good coupling impedance.

The impedance of the coupling and protection circuit causes the transmit signal voltage drop, and limits the maximum current injected into the mains (provided that the maximum output voltage swing is 12 V). The impedance of the C20/L1 circuit is shown in the following figure (the equivalent serial resistivity values of the capacitor and inductor are ignored). Modify the component values to get a lower coupling-circuit impedance, for example 470 nF and 10 µH.

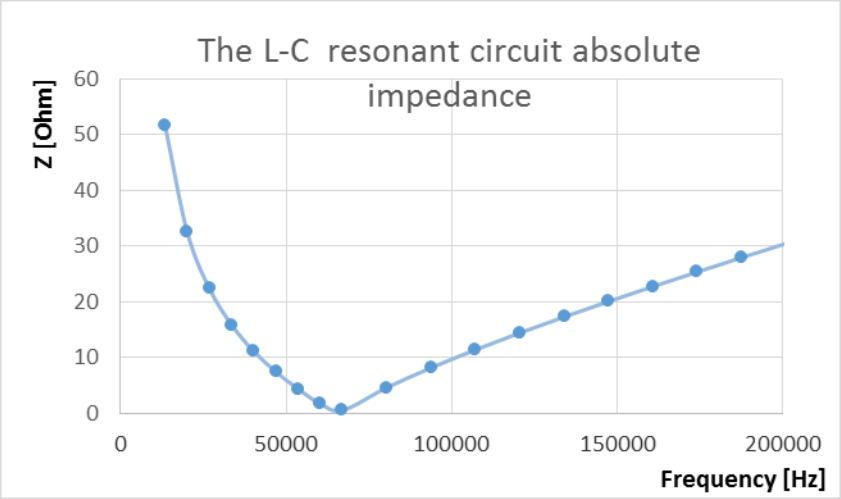

Figure 12. Absolute L-C resonant circuit impedance

9. Protection Circuit

The transmitter protection circuit is an essential part of the analog front end, because the mains is a very hostile environment with the common mode or differential over-voltage. The coupling circuit may inject a high current into the circuit during a hot plug into the mains. Therefore, there is a heavy protection circuit securing the line driver output and the receiver input. The protection circuit introduces an unwanted 0.33-Ω resistivity to the transmitter coupling path. The diodes D5/D15 and D4/D6 short-cut the voltage spikes to the capacitors and the power supply.

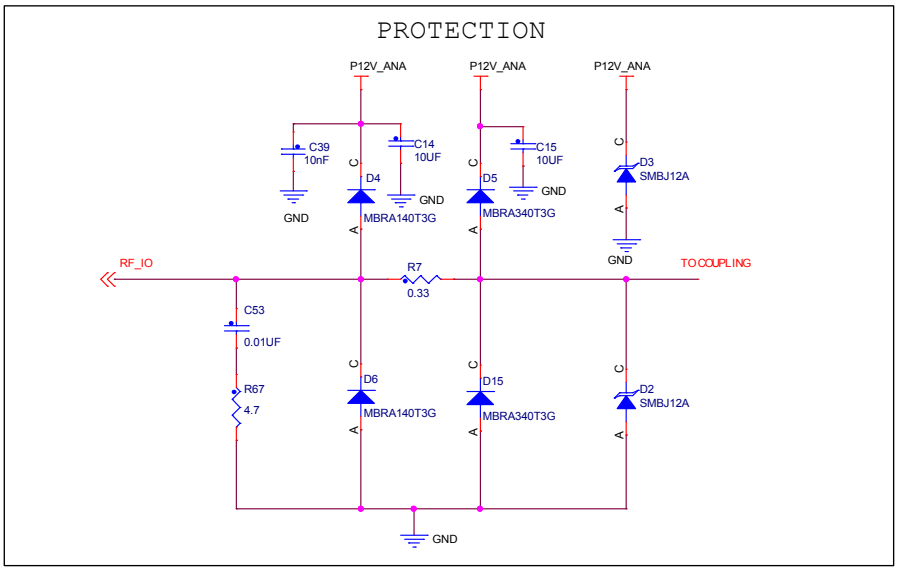

Figure 13. Protection unit

The protection unit must be robust to avoid over-voltage on the line-driver output.

10. Receiver

The purpose of the receiver is to scale the received input signal coming from the mains to a level appropriate for the MCU ADC. The receiver path consists of a passive high-pass input filter with a corner frequency of 25 kHz and an in-band attenuation of -6 dB, followed by two PGA stages with a combined gain from 0 dB to 63 dB. The final stage is a low-pass filter with a corner frequency of 110 kHz and an in-band attenuation of -6dB. After the final receiver stage (low-pass filter), the signal has a level of 1.65 V DC and the output swing of 1.5 Vpp. The ADC converter must use ~3.3 V as its voltage reference.

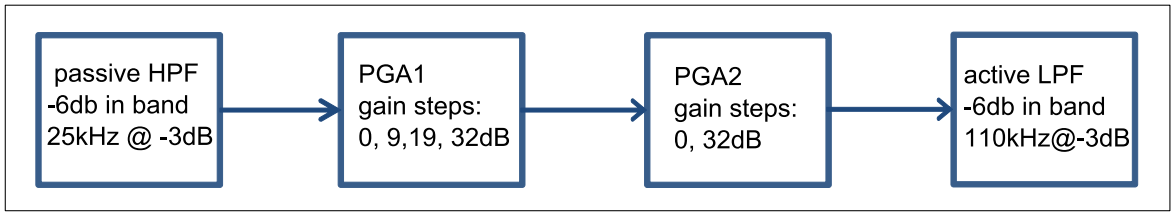

Figure 14. Receiver signal path

The receiver signal path is used to scale the received signal to a level suitable for the MCU ADC. The path consists of the low-pass filter, the high-pass filter, and two PGA stages.

10.1. High-pass filter

The third-order high-pass filter consists of passive components C34, C43, and L5, and the cut-off frequency is set to 25 kHz. The filter has an input impedance of 180 Ω, and uses the 180-Ω load resistor R15. The filter has a signal in-band attenuation of 6 dB. The filter removes the low-frequency noise and prevents the following PGA stages from saturation.

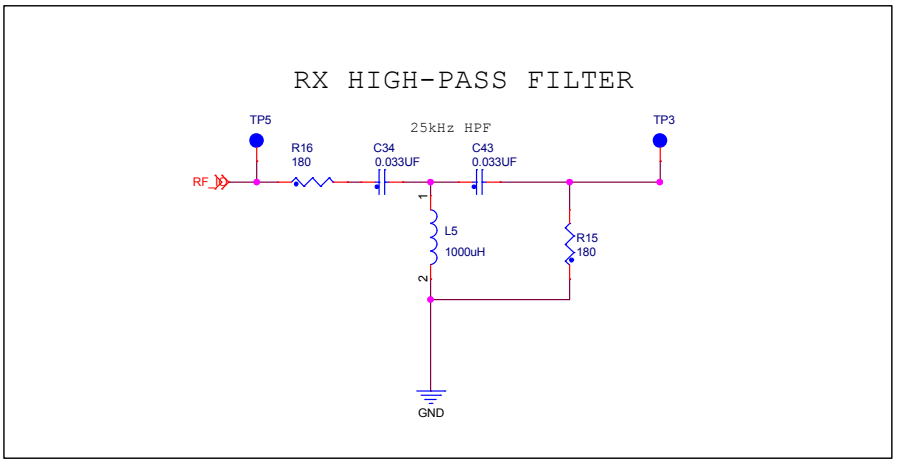

Figure 15. Receiver high-pass filter

The receiver high-pass filter removes the signals with frequencies lower than 25 kHz. The filter has a -6 dB in-band attenuation to prevent PGA1 from saturation.

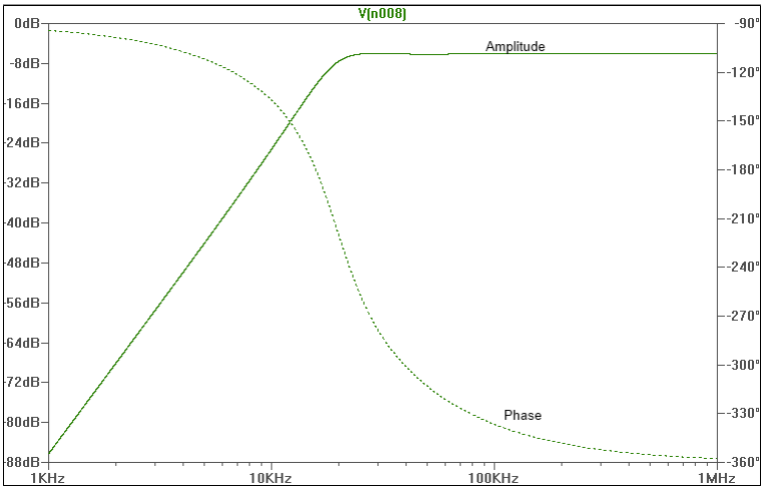

Figure 16. High-pass filter transfer function

10.2. Programmable gain amplifier

Because the PLC received input signal dynamic range is wider than what the MCU ADC can handle, the Programmable Gain Amplifier (PGA) is used to scale the signal to a level suitable for the MCU ADC input range. The expected dynamic range of the input signal is around 110 dB. Therefore, two PGA stages are used. The first stage (PGA1) has the gain steps of 0, 9.5, 19, and 31.5 dB, while the second stage (PGA2) has only two gain steps of 0 and 32 dB.

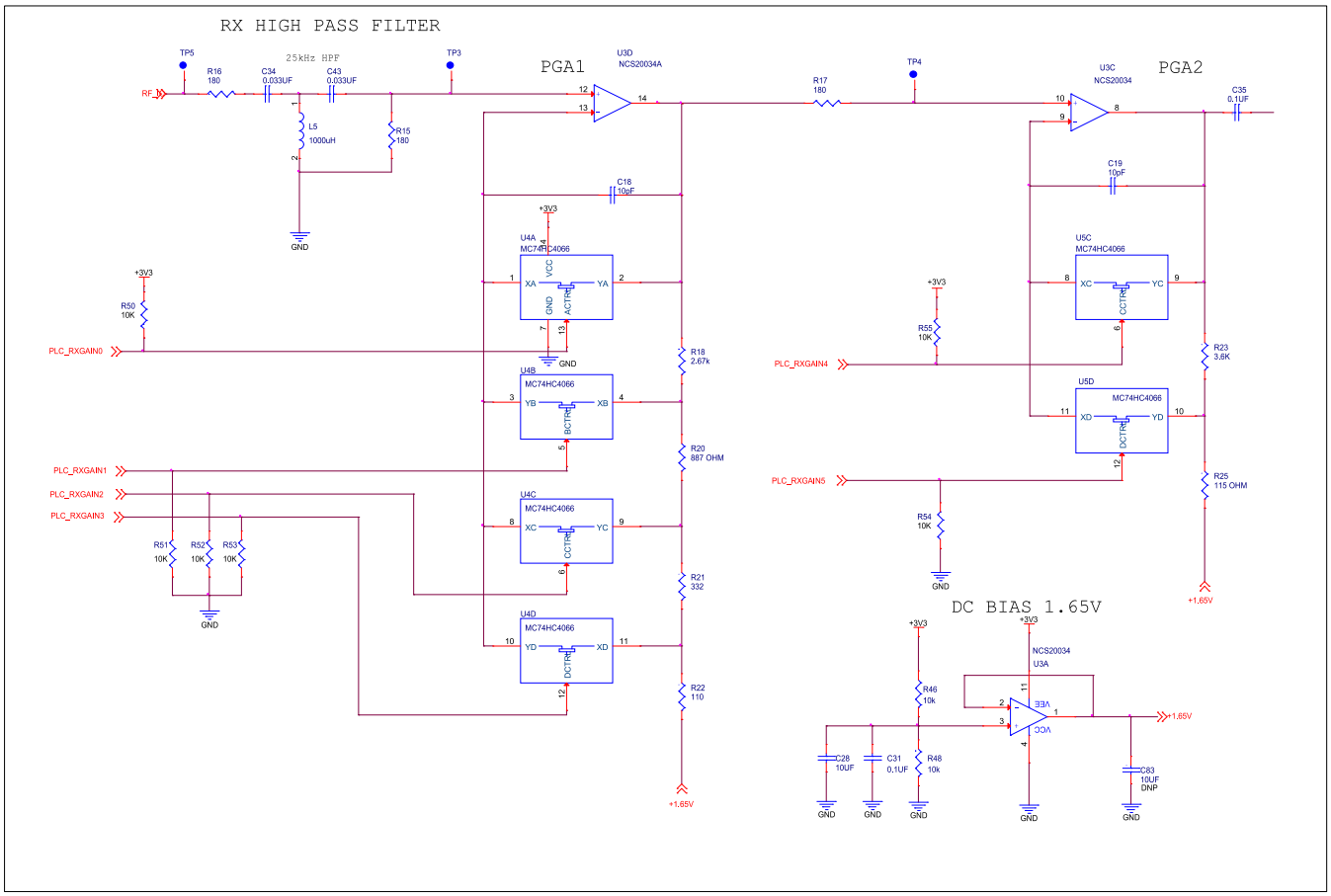

Figure 17. Two PGA stages and control circuits

The bias voltage for the receiver is created using the R46/R48 voltage divider, and uses the U3A operational amplifier as a buffer.

10.3. Receiver PGA gain control

The receiver uses six digital signals to control the gains on both PGA stages. The following tables show the gain-control signals' settings and the corresponding gains.

Table 6. PGA1 control signals' settings and corresponding gains

MK26FN2M0VLQ18 pins	PLC signal name	State and gain [dB]			
PTB21	PLC_RXGAIN0	1	0	0	0
PTB19	PLC_RXGAIN1	0	1	0	0
PTB18	PLC_RXGAIN2	0	0	1	0
PTB20	PLC_RXGAIN3	0	0	0	1
Gain [dB]		0	9.5	19	31.5

Table 7. PGA2 control signals' settings and corresponding gains

MK26FN2M0VLQ18 pins	PLC signal name	State and gain [dB]	
PTB22	PLC_RXGAIN4	1	0
PTB23	PLC_RXGAIN5	0	1
Gain [dB]		0	32

Table 8. PGAx control signals' voltage level thresholds

Digital VCC3V3 = 3.3 V	Input low max [V]	Input high min [V]
PLC_TXGAINx	1.5	1.9

The gain settling time is also an important parameter that serves to receive a correct signal. The gain settling times for both the PGA1 and PGA2 are short (in the range of microseconds). The following two figures show the gain settlings for PGA1 and PGA2.

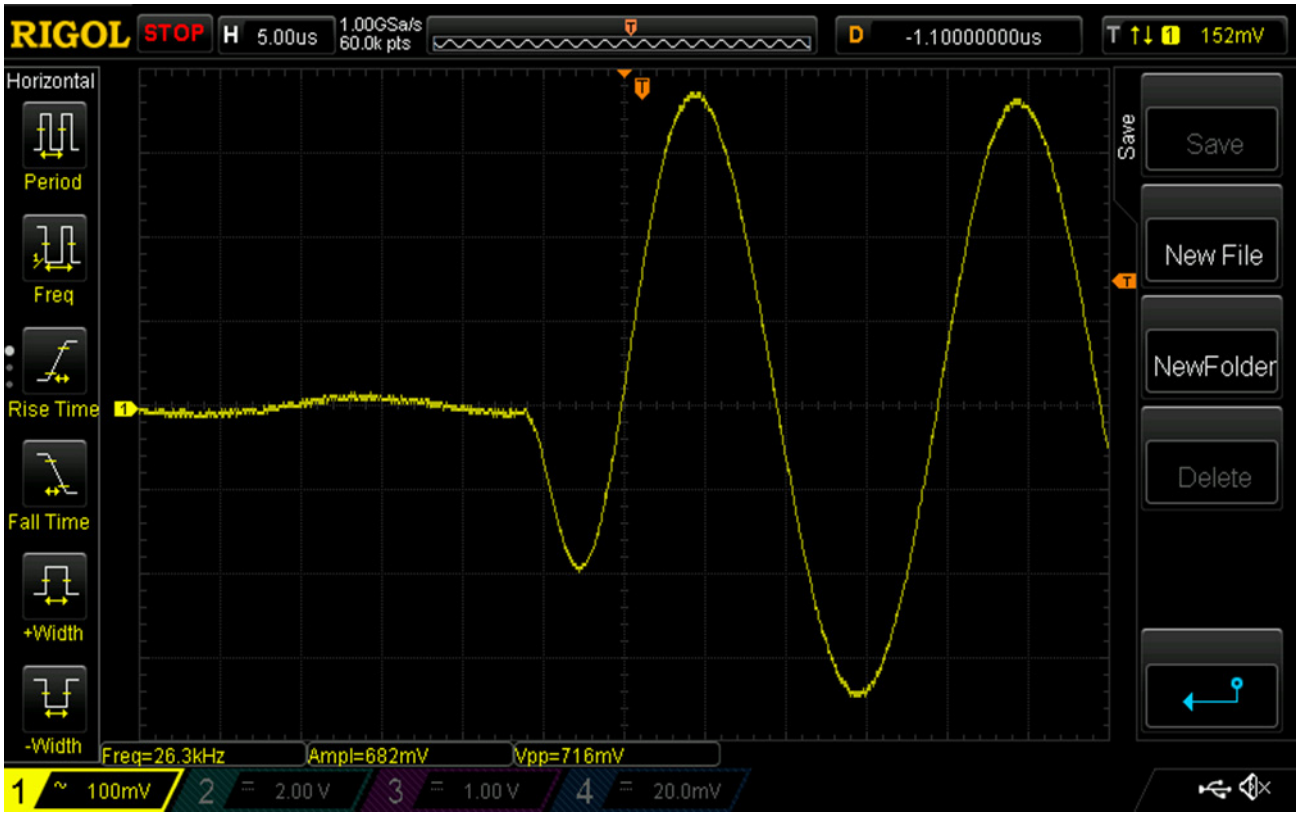

Figure 18. RX PGA1 gain-settling time (yellow trace measured on TP10) 0 db to 9.5 dB

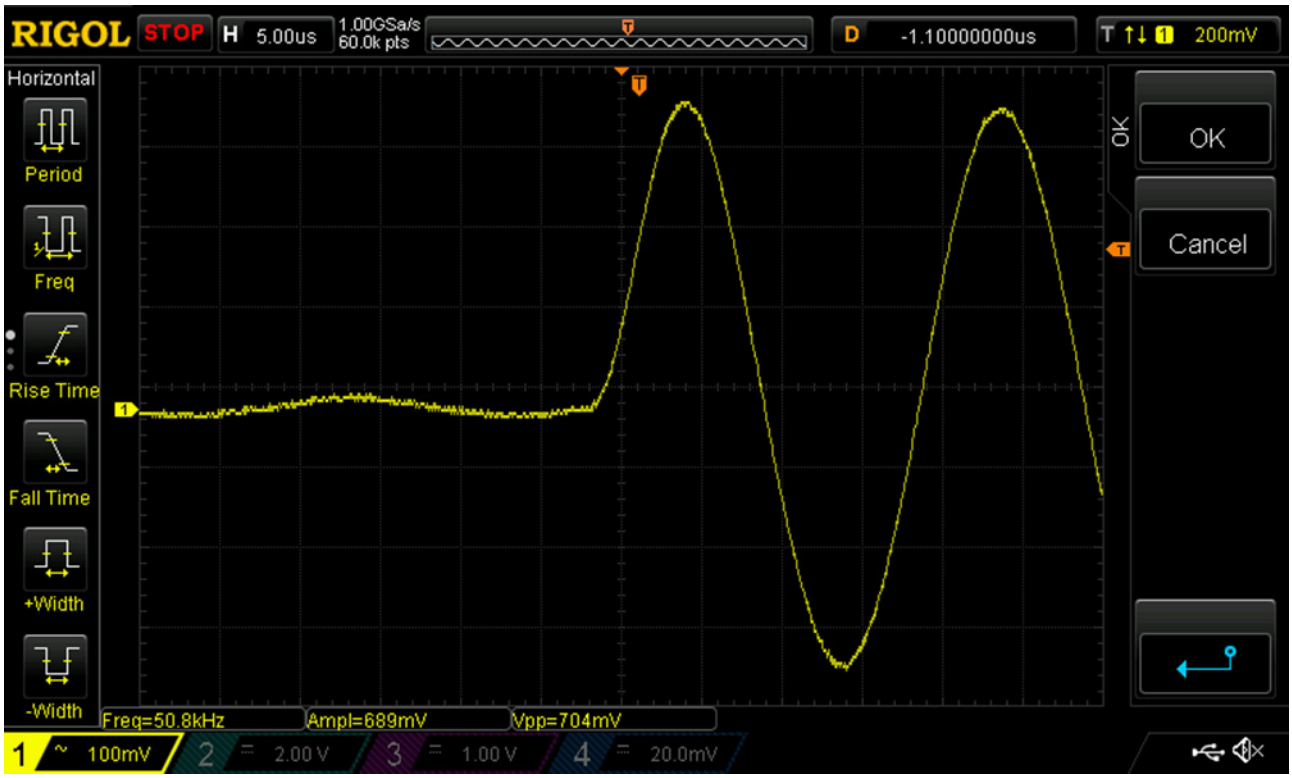

Figure 19. RX PGA2 gain-settling time (yellow trace measured on TP10) 0 db to 32 dB

10.4. Low-pass filter

The last stage of the receiver circuit is the third-order low-pass filter with a corner frequency of 125 kHz, filtering out all of the higher-frequency noise to fulfill the Nyquist criteria for an ADC converter input. The filter introduces a 6-dB in-band signal attenuation, and keeps the DC voltage level at 1.65 V, which is the center of the ADC converter input range (provided that it has a reference voltage of 3.3 V). The output from the low-pass filter feeds the MCU's single-ended AN0 ADC input.

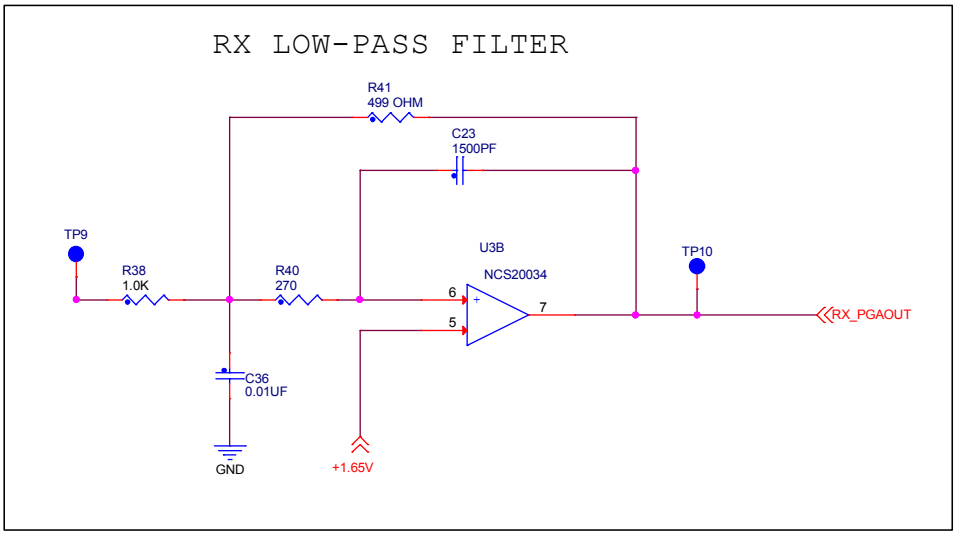

Figure 20. Receiver third-order low-pass filter schematic

The filter removes the signals with a frequency above 110 kHz. The filter has a 6-dB in-band attenuation:

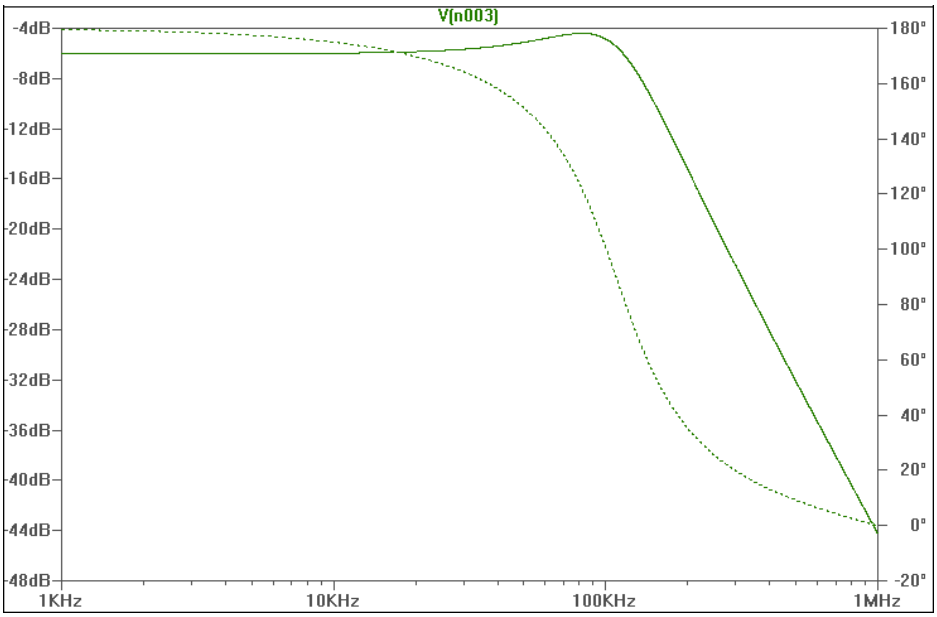

Figure 21. High-pass filter frequency and phase response (graph is simulated)

The receiver consists of four blocks with various gains, so it may be a bit confusing to set the gains. Table 9 shows the signal levels at various points of the receiver circuit. The maximum received signal voltage is chosen by the CENELEC signaling limit for a narrow-band signal (134 uVp, column 1 in Table 9). The expected line attenuation (column 2 in the table) varies from 0 to 110 dB. The first stage (the high-pass filter) attenuates the signal by 6 dB (column 4). The signal is then consecutively amplified by the gain chosen at the first and second stages of the PGA. The columns 5 and 6 show the PGA1 gain and signal levels. The columns 7 and 8 show the PGA2 gain and signal levels. At the last stage (the low-pass filter), the signal is attenuated by 6 dB (column 9).

The input RX signal higher than 129 dB is saturated at PGA1 (the red values in the first row).

For the line attenuation greater than 80 dB, the signal is lower than 104.5 dBuV. Therefore, the ADC input signal is 1/17 FS. From this point on, the receiver signal decoding starts to lose accuracy.

NOTE

As the receiver path consists of four blocks with various gains, there is a table that shows the voltage levels on each block for better understanding. It is also very important to avoid saturating the PGA2 input by a wrong gain setting in the first stage of PGA1.

This table shows the voltage levels at all receiver blocks for various input-voltage levels and gain settings:

Table 9. Received signal voltages

1. TX signal [dBuVpk]	2 Line attenuation [dB]	3 Line input [dBuVp]	4 High-pass filter -6dB [dbuVp]	5 PGA1 gain [dB]	6 PGA1 [dBuVp]	7 PGA2 gain [dB]	8 PGA2 [dBuVp]	9 Low-pass filter -6dB ADC level [dBuVp]
134	0	134	128	0	128	0	128	122
134	5	129	123	0	123	0	123	117
134	10	124	118	0	118	0	118	112
134	15	119	113	9.7	122.7	0	122.7	116.7
134	20	114	108	9.7	117.7	0	117.7	111.7
134	25	109	103	19.12	122.12	0	122.12	116.12
134	30	104	98	19.12	117.12	0	117.12	111.12
134	35	99	93	0	93	30.1	123.1	117.1
134	40	94	88	0	88	30.1	118.1	112.1
134	45	89	83	9.7	92.7	30.1	122.8	116.8
134	50	84	78	9.7	87.7	30.1	117.8	111.8
134	55	79	73	19.12	92.12	30.1	122.22	116.22
134	60	74	68	19.12	87.12	30.1	117.22	111.22
134	65	69	63	32.4	95.4	30.1	125.5	119.5
134	70	64	58	32.4	90.4	30.1	120.5	114.5
134	75	59	53	32.4	85.4	30.1	115.5	109.5
134	80	54	48	32.4	80.4	30.1	110.5	104.5
134	85	49	43	32.4	75.4	30.1	105.5	99.5
134	90	44	38	32.4	70.4	30.1	100.5	94.5
134	95	39	33	32.4	65.4	30.1	95.5	89.5
134	100	34	28	32.4	60.4	30.1	90.5	84.5
134	105	29	23	32.4	55.4	30.1	85.5	79.5
134	110	24	18	32.4	50.4	30.1	80.5	74.5

10.5. Receiver signal quality and transfer function

The signal quality is essential because the receiver works with relatively small signals. The following measurements show the signal transfer functions and the LP filter. The measurement is done using the topology shown in the following figure. The signal is generated by the Keysight 33600A signal generator (connected to the K1 connector), and measured at the test point TP10 (to offload the OpAmp through the 200 Ω resistor).

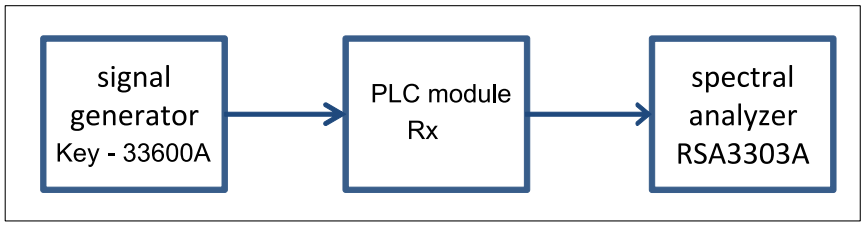

Figure 22. Receiver harmonic distortion measurement topology

10.6. Receiver transfer function for all gain settings

In the first measurement, there is a whole receiver path transfer function with all possible gains of the PGA. The lower lines are measured with PGA2 set to 0 dB, while the upper four lines are measured with PGA2 set to 32 dB. In the right-hand side of the picture, there is a noticeable noise for the lowest signal levels, generated partly by the MCU and partly by the power supply. The following figure shows the full receiver path transfer function for all the gains. The input signal is generated by the Keysight 33600A signal generator, connected to the K1 connector. The signal level is 2.3 mVpp.

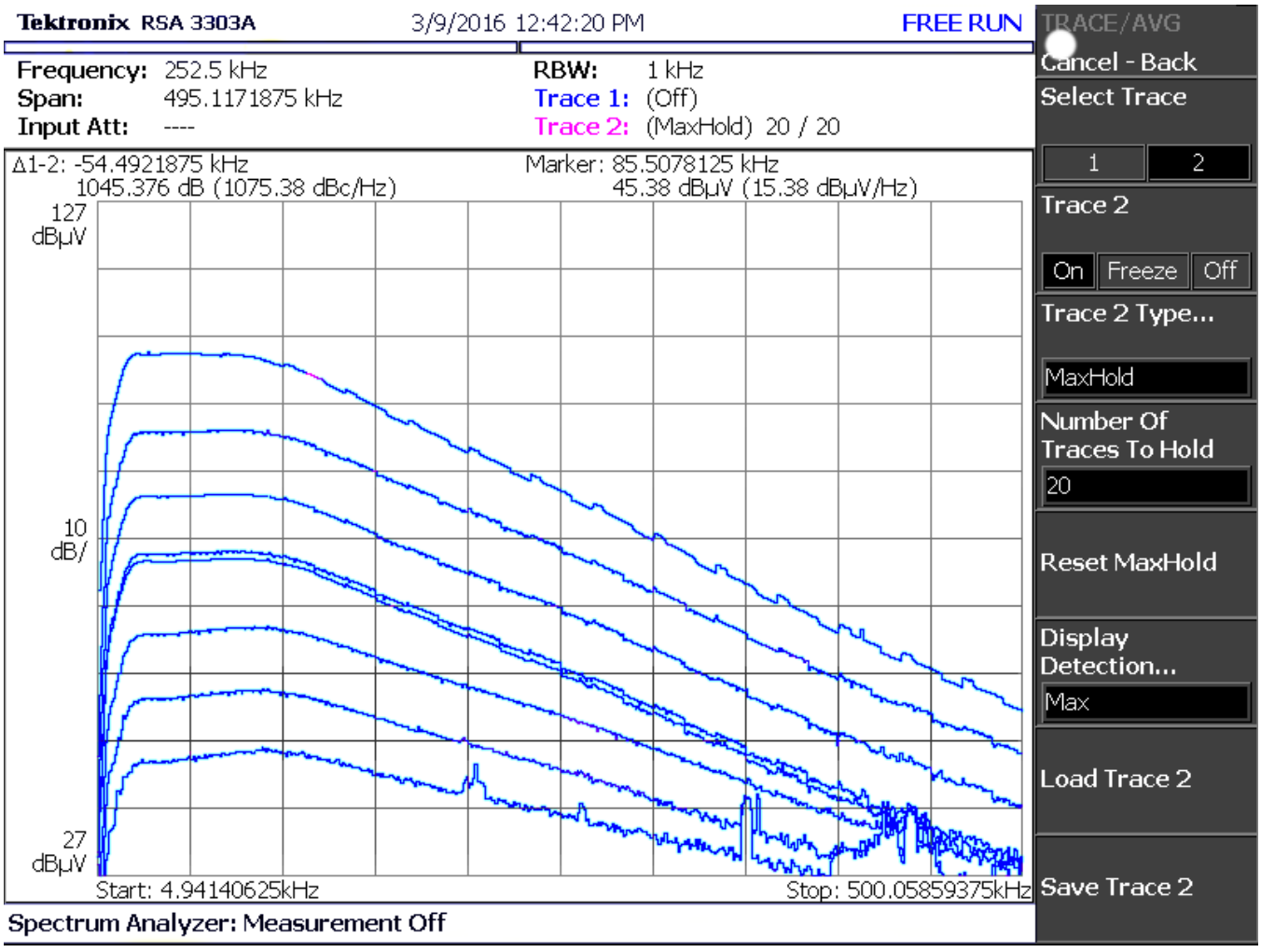

Figure 23. Full receiver path transfer function for all gains

10.7. Receiver harmonic distortion

The following two figures show the spectral parameters of the receiver. The input signal is generated by the arbitrary function generator Keysight 33600A, and injected into the mains connector K1.
The spectral chart is measured at resistor R44 (the input of the ADC). The harmonic distortion is measured for 30 kHz and 90 kHz. There are noticeable higher harmonics that are ~50 dB lower than the first one. There is also the background noise. In the following figure, the input RX signal is 4.4 Vpp @ 30 kHz. PGA1 = 0 dB and PGA2 = 0 dB.

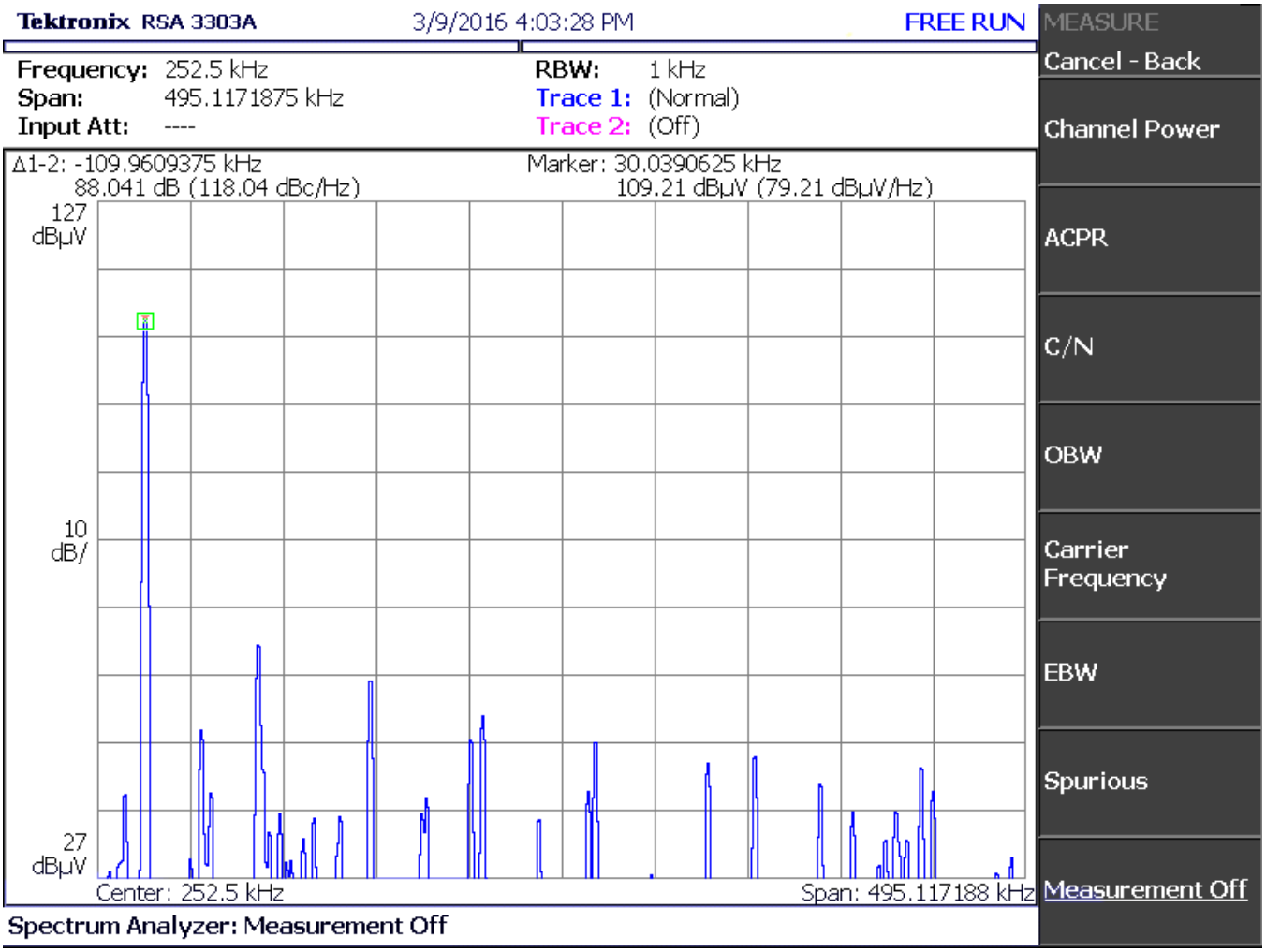

Figure 24. Receiver harmonic distortion (case 1)

In the following figure, the input RX signal is 4.4 Vpp @ 90 kHz. PGA1 = 0 dB and PGA2 = 0 dB.

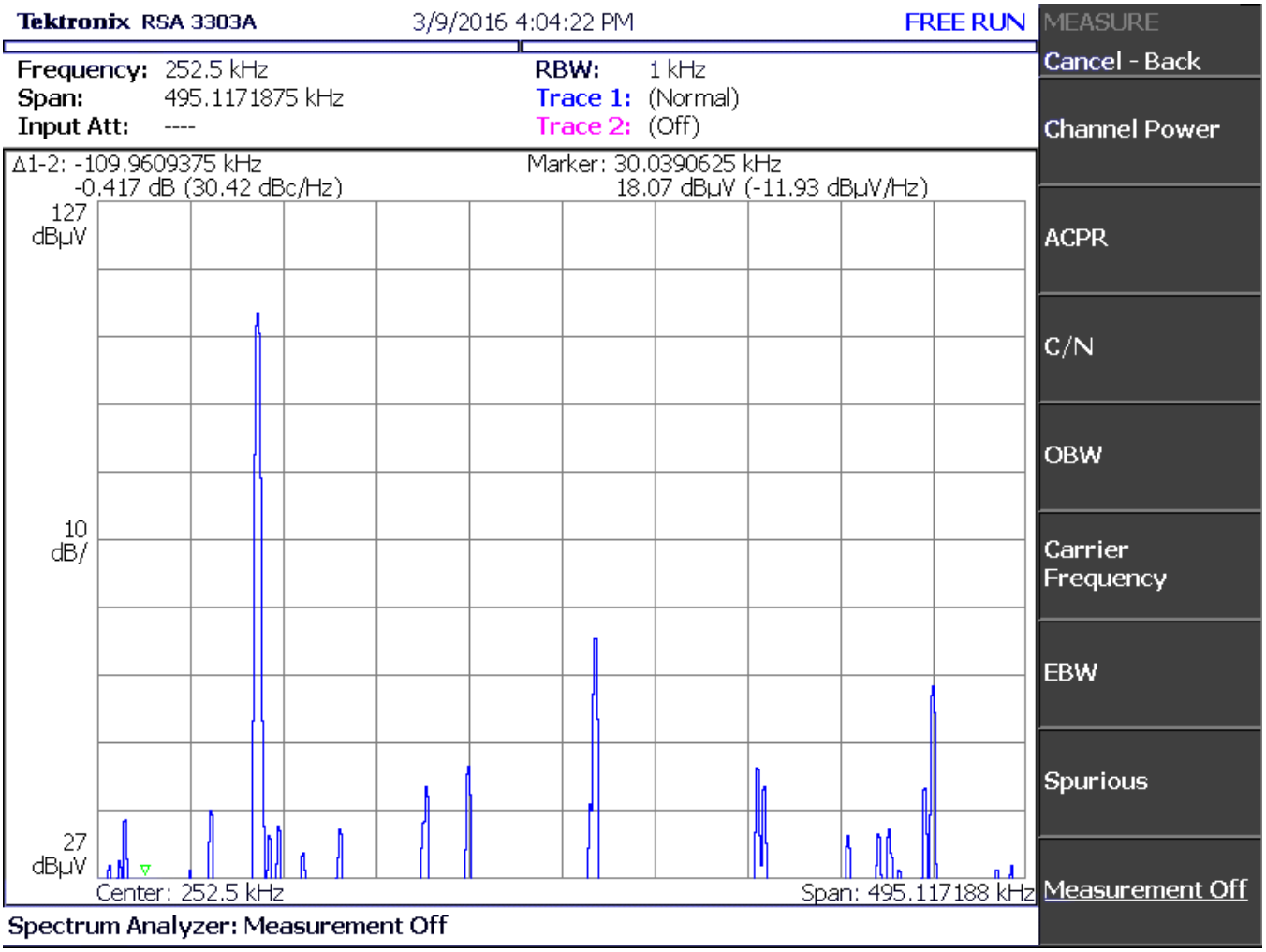

Figure 25. Receiver harmonic distortion (case 2)

11. Communication

The PLC module inherits its connectors from the Arduino system, and provides a similar set of communication interfaces. All the interfaces are connected directly to the MK26FN2M0VLQ18 MCU, and all signals have a voltage level of 3.3 V. There is no additional ESD protection for the interfaces, only the one implemented in the MCU.

The available communication interfaces are UART, SPI, I^2C, two timers, two GPIO pins, and six analog inputs.

The USB is available on the board.

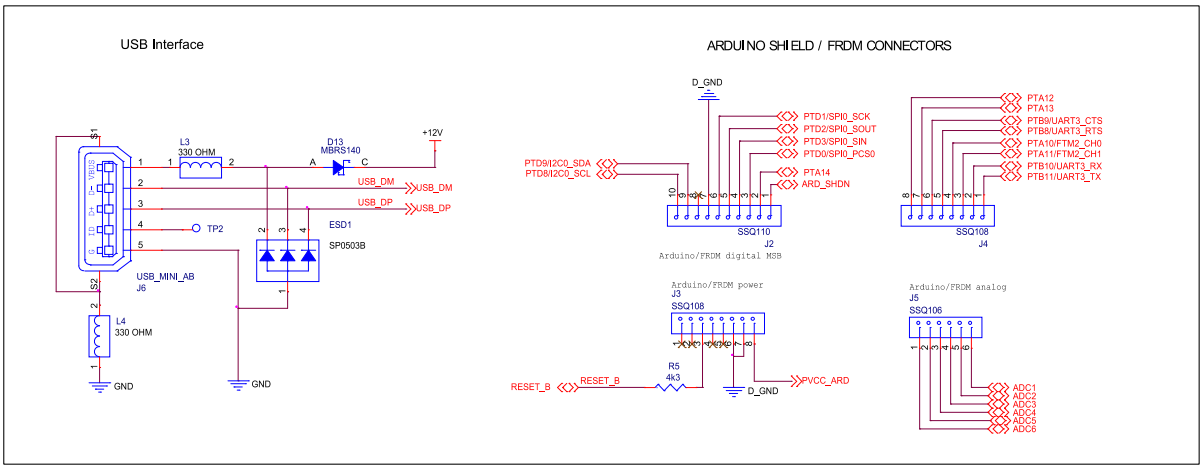

Figure 26. Communication interfaces available on communication board

12. Zero-Crossing Detection

Some of the PLC protocols use the mains zero-crossing event for synchronization. The communication module provides the zero-crossing signal. The signal is opto-isolated, and provides a rectangular analog output. This signal is connected to the MK26FN2M0VLQ18 comparator input CMP1_IN2 (pin 36).

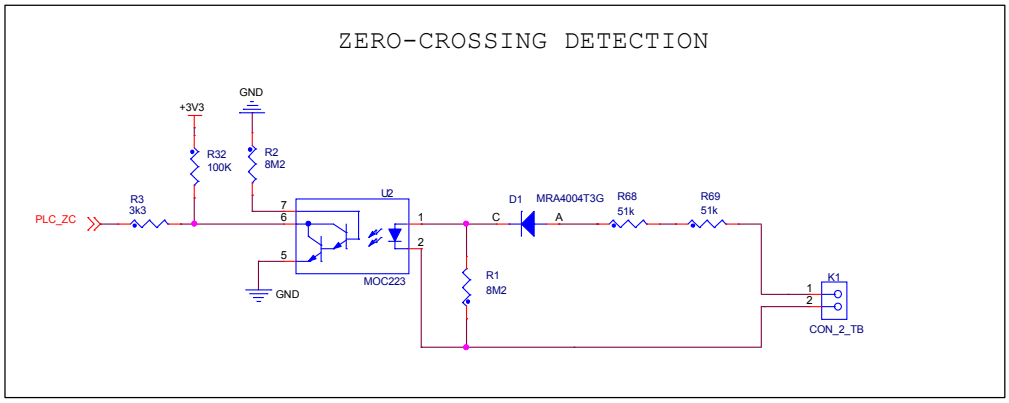

Figure 27. Zero-crossing detection circuit

13. Power Supply

The communication module nominal power supply is 12 V DC @ 2 A. Supply the module either via the power jack connector J8, or via the J3[PVCC_ARD] input. The board is equipped with the automatic power path controller U10, which automatically switches between the power sources.

If there is no power supply present on the J8 or J3[PVCC_ARD], supply the board from the USB VDD bus (+5 V DC). In this case, the transmitter analog part does not work, as this voltage level is not sufficient for NCS5651.

The whole board has two voltage levels: one for the TX analog part (12 V DC), and one for the digital part of the MCU and the receiver (3.3 V). The 3.3 V DC-bus that supplies the MCU is derived from the 12 V input by the step-down converter U9, and is able to supply up to 500 mA.

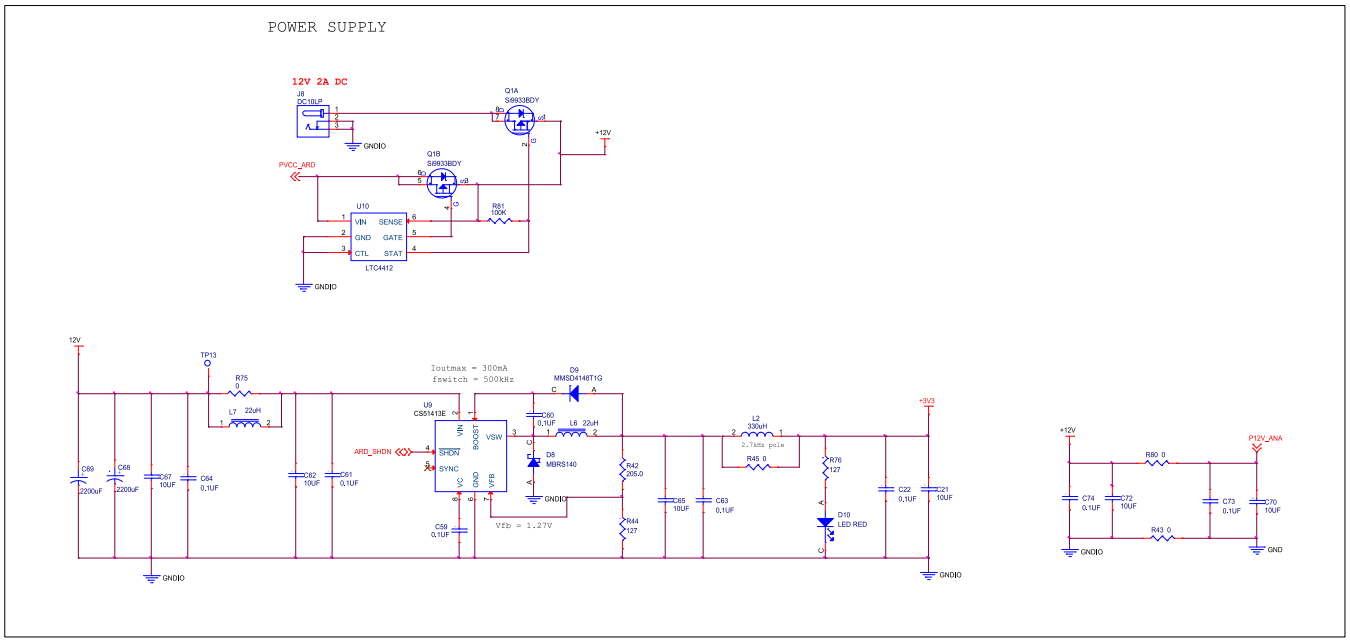

Figure 28. PLC module power supply

14. Revision History

This table summarizes the changes done to the document since the initial release:

Table 10. Revision history

Revision number	Date	Substantive changes
0	04/2016	Initial release.

15. Attachments

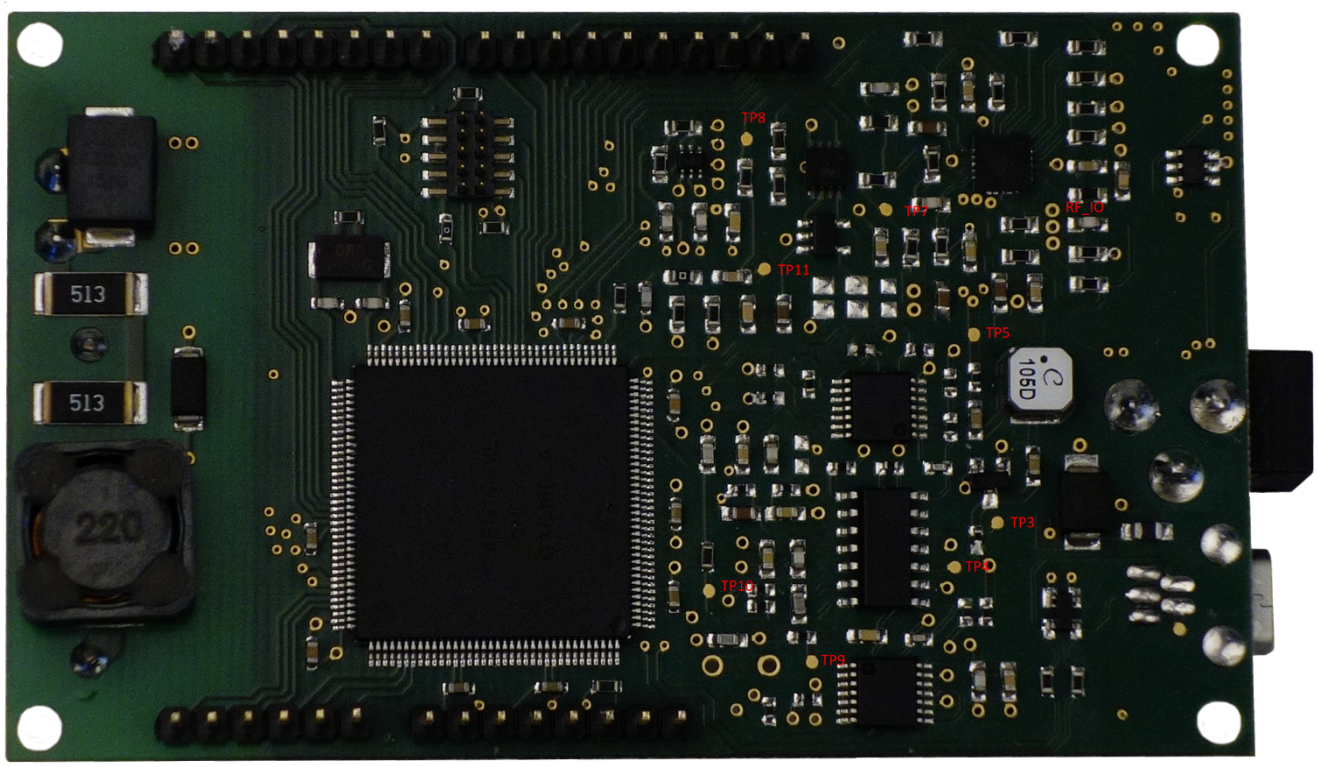

Figure 29. Test points position

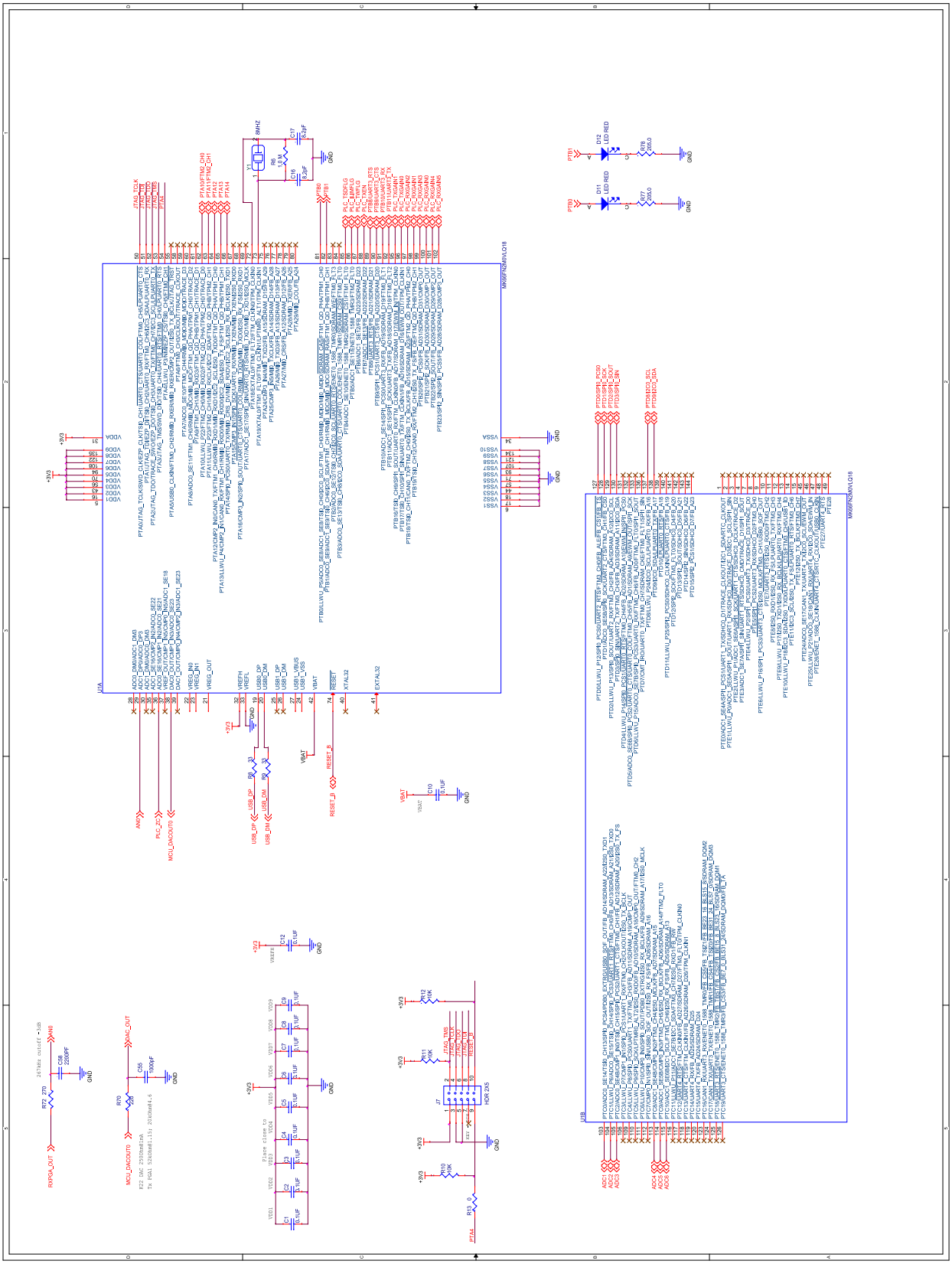

Figure 30.

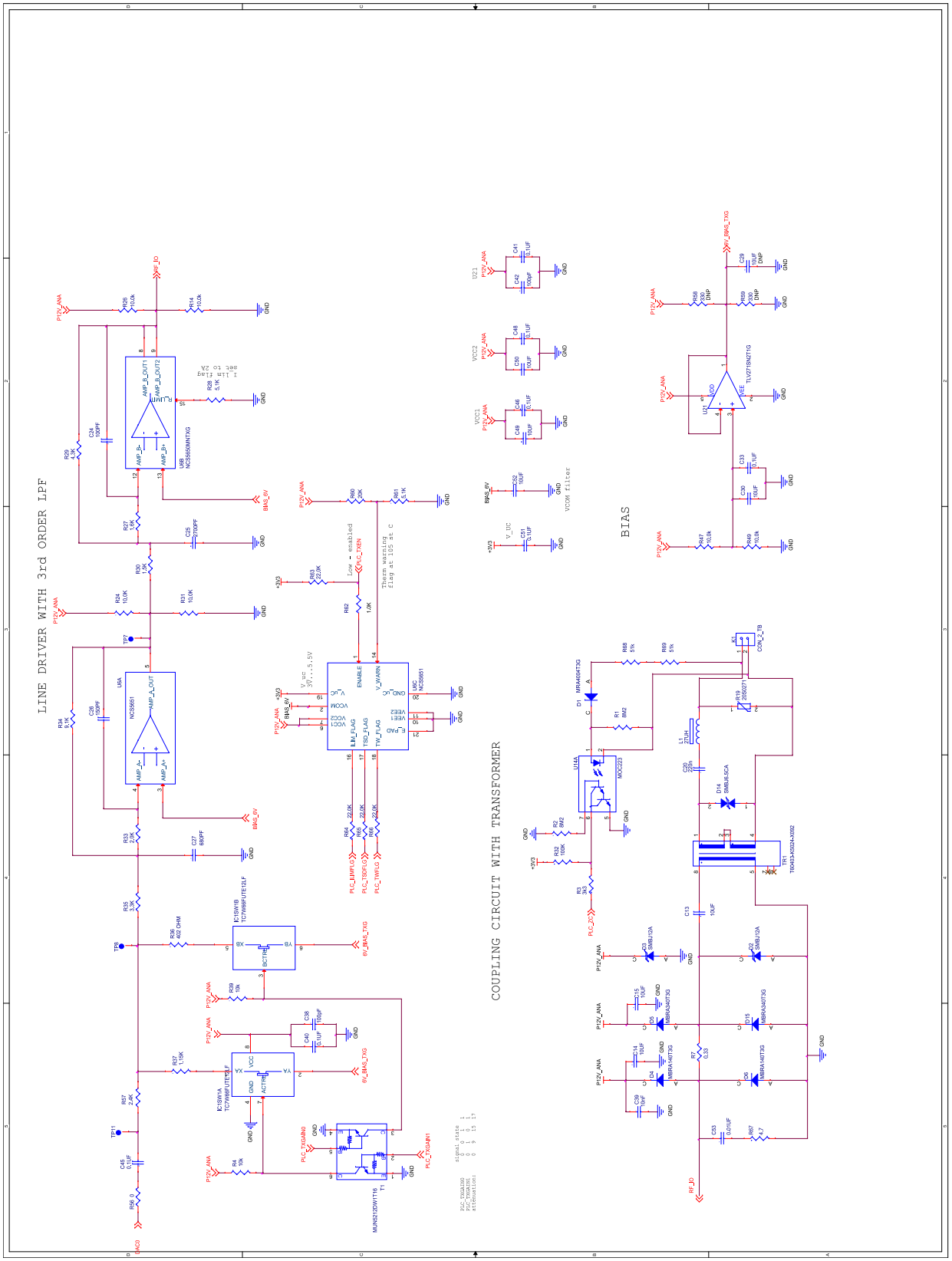
LINE DRIVER WITH 3rd ORDER LPF
COUPLING CIRCUIT WITH TRANSFORMER
BIAS

Figure 31.

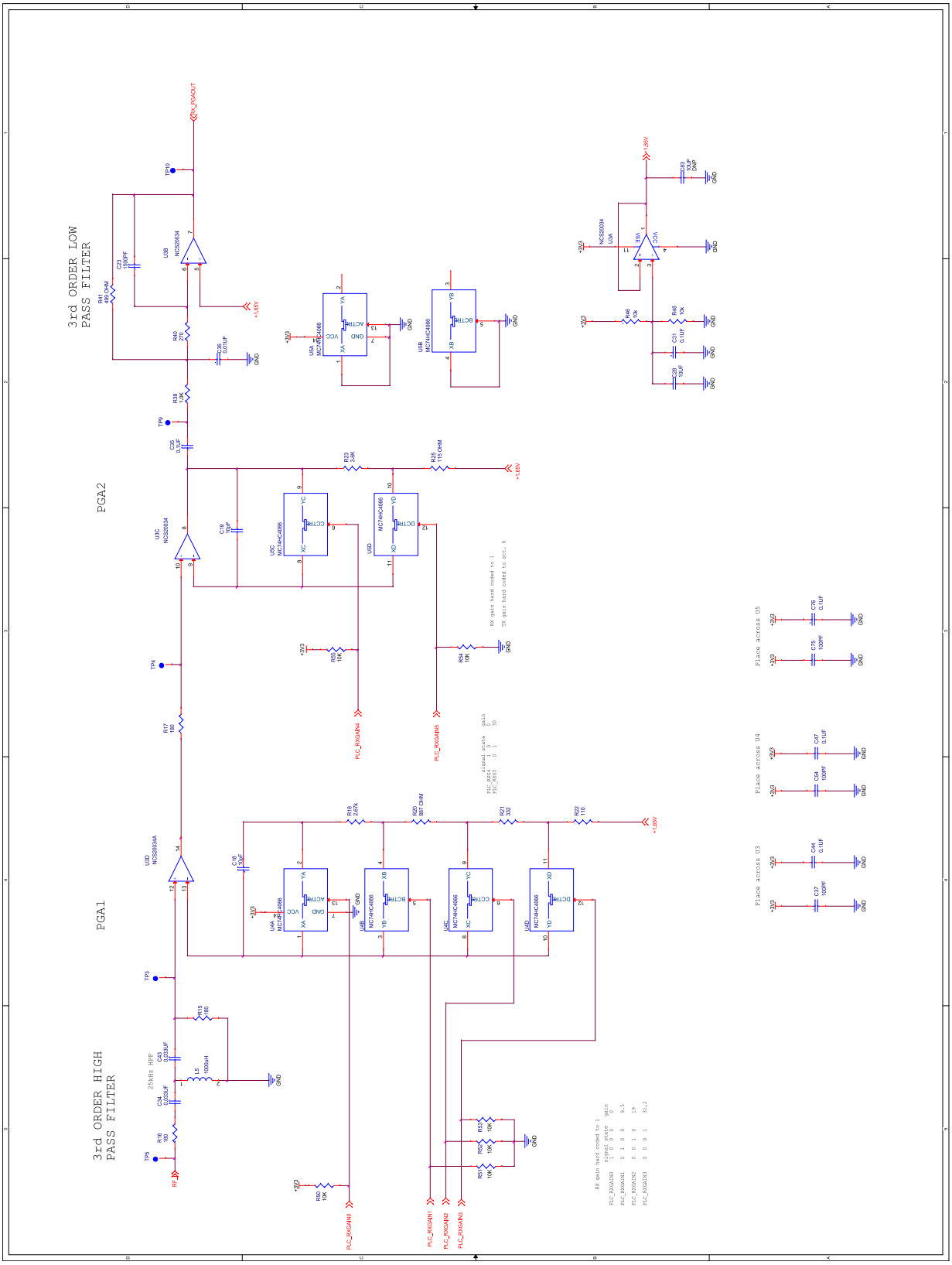
3rd ORDER LOW
PASS FILTER
PGA2
PGA1
3rd ORDER HIGH
PASS FILTER
Place across U5
Place across U4
Place across U3

Figure 32.

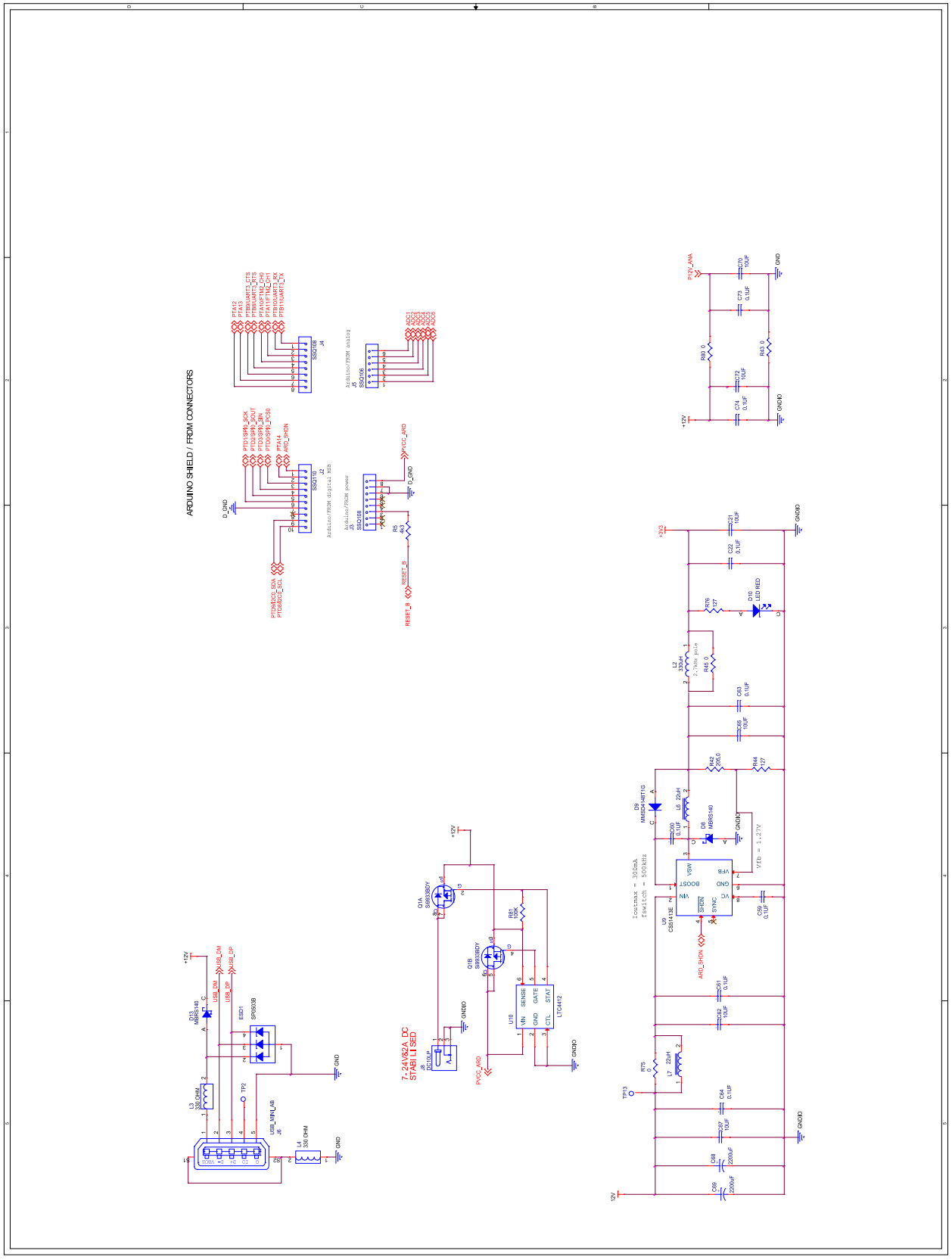

Figure 33.

Power-Line Communication Module for CENELEC Band, Design Reference Manual, Rev. 0, 05/2016

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