MSC8144ADS Processor Board

Reference Manual

MSC8144ADSRM
Rev 0, February 2007

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MSC8144ADSRM
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Contents

General Information 1

This document describes the MSC8144ADS processor board. The MSC8144ADS processor board is an application development system (ADS) that provides a complete debugging environment for engineers developing applications for the Freescale MSC8144 DSP family.The MSC8144ADS processor board is intended to serve as a platform for software and hardware development in the MSC8144 processor environment. On-board resources and the associated debugger enable developers to perform a variety of tasks: download and run code, set breakpoints, display memory and registers, and connect proprietary h/w via the expansion connector. This board answers the development needs of three different infrastructure applications: wireless transcoding, IP telephony, and video transcoding. It can also be used as a demonstration tool for these types of applications, and for control processing in applications such as network routers and switches, mass storage subsystems, network appliances, and print and imaging systems.

The MSC8144 device is a highly integrated DSP processor that contains four StarCore SC3400 DSP subsystems, 512 Kbyte of M2 shared memory, 10 Mbyte of M3 shared memory, L1 instruction and data caches optimized for packet telephony, 128 Kbyte of shared L2 instruction cache, a DDR memory controller, a serial RapidIO® interface, two 10/100/1000Base-T Ethernet controllers, an ATM Controller Supporting various ATM adaptation layers, eight 512-channel time-division multiplexing (TDM) interfaces, a 16-channel DMA controller, 32-bit PCI interface that runs at 66/33MHz, a UART interface, and an I^2C interface.

The MSC8144ADS processor board is based on the 64-bit MSC8144 as a slave processor controlled from an MPC8560 host processor via a PCI bus or GETH switch. However, the board can be configured to bypass the host in certain situations. In addition, the board can function in a standalone configuration or as an AMC card in the ATCA system. The ADS board uses a triple AMC form factor.

1.1 Working Configurations

The MSC8144ADS has two basic operating modes, as discussed in the following sections. In addition to the basic modes, there are two debugging chain options that can be used with either operating mode.

1.1.1 Standalone Mode

The MSC8144ADS processor board can be run in a standalone mode, like other application development systems, with direct connections to debuggers, power supply, and other external connections.

1.1.2 AMC Mode

As opposed to standalone mode, in this mode, the MSC8144ADS processor board can be connected to an additional MSC8144ADS processor board via the AMC ATCA edge connector. For details on this mode, see **Chapter 6**, *Expansion Options*. The MSC8144ADS processor board can also be connected to a TUNDRA platform via the edge connector.

1.1.3 Debugging Chain Options

Both options can be used in standalone and AMC modes.

1.1.3.1 Single

A single debugger connection can be used to debug applications for the MSC8144ADS processor board. The debugger can be connected to either the MSC8144, or the MPC8560, or both of them simultaneously (but independently). For a single connection to the MSC8144, use the P1 connection, and configure the board for this using the DIP switches (SW[2–3]). For a single connection to the MPC8560, use the P11 connection, and configure the board for this using the DIP switches (SW[2–3]).

1.1.3.2 Chain

A chain connection can be used to debug applications for the MSC8144ADS processor board. In such a case, the debugger can only be connected to the MSC8144-MPC8560 via the P1 connection. Use the DIP switches (SW2.3) to configure the board for this.

1.2 MSC8144ADS processor board Features

The ADS is based on the MSC8144 as slave processor controlled from a PQIII (MPC8560) via the PCI bus or GETH switch.

- Supports MSC8144 running at up to 1000MHz, with cores voltages at 1V.
- Dual DDR (DDR1 and DDR2) on SODIMM with 32 bits utilized, which provides a 256 Mbyte capacity, at a data rate up to 533 MHz
- Programmable Hard Reset Configuration for MSC8144 is executed from PCI host (MPC8560), I^2C EEPROM or other sources.
- Configuration and boot code for the host is loaded from Flash memory.

- PTMC expansion connectors carries most signals of both processors (except High Speed signals)
- PTMC pinout is designed to comply with the PT3MC or PT5MC standard.
- RGMII GETH switch and SGMII GETH switch (expands connectivity options)
- Two E1/T1 framers and codec on TDM bus.
- Debugging is performed via an external command converter connected to the OnCE 14-pin header or COP 16-pin header for separate access to the processors.
- JTAG Chain mode is provided via EOnCE header.
- After MSC8144 reset, the MSC8144 Debug Enable/Disable options may be selected. The processor EE pins enable and support the noted options.
- Board Control and Status Register (BCSR) implemented in FPGA.
- Board Identification and board status may be read via the BCSR.
- Two SMB form RF-connectors enable the connection of up to two external pulse generators to the two clock inputs of the MSC8144.
- Various configurations (configurable via DIP switches or BCSR):
  - Standalone mode with an external power 12 VDC @ 6 A.
  - As an AMC card in the ATCA system.
  - No host (the host MPC8560 stays in continued reset—configurable via SW 2.1). All local bus operations are emulated by I^2C expanders and controlled from the MSC8144.
- Push Buttons
  - Main Power-On Reset (for both Host and Slave);
  - Hard Reset, Soft Reset, and NMI for MSC8144

1.3 External Connections

The MSC8144ADS processor board interconnects with external devices via the following set of connectors (see **Figure 1-1** and **Figure 1-2**):

1. Double RS232 9-pin connector (P2).
   Upper - connects to Host UART port.
   Lower - connects to MSC8144 UART port
2. Stereo Jack, **LINE-IN** (P4)
3. Stereo Jack, **LINE-OUT** (P6)
4. Four GETH ports RJ-45 connectors with LEDs (100 MHz displays green and 1GHz displays amber) (P9)
5. Double RJ-48 eight pin E1/T1 connectors (J5)
6. Four 64-pin PTMC connectors for expansion cards (J1–J4).
7. Mictor LA Connectors hold host (MPC8560) LBC signals (P7–P8]).

8. 5 V connection for fan (J6)
   Mounted: Fan is connected
   Removed: Fan is not connected
9. Host (MPC8560) COP Debug connector 16-pin (P11 to work with host only with single JTAG).
10. Power jack for 12 V @ 6 A external power supply (P10)
11. ISP 14-pin connector to program Altera FPGA. (P3)
12. MSC8144 OnCE Debug connector 14-pin (P1 for single or chain).
13. AMC edge connector (P26)

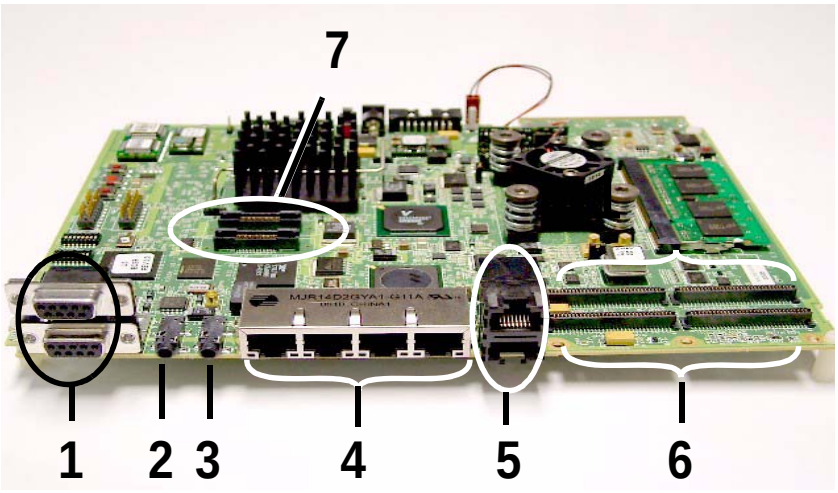


Figure 1-1. MSC8144ADS processor board External Connections (front view)

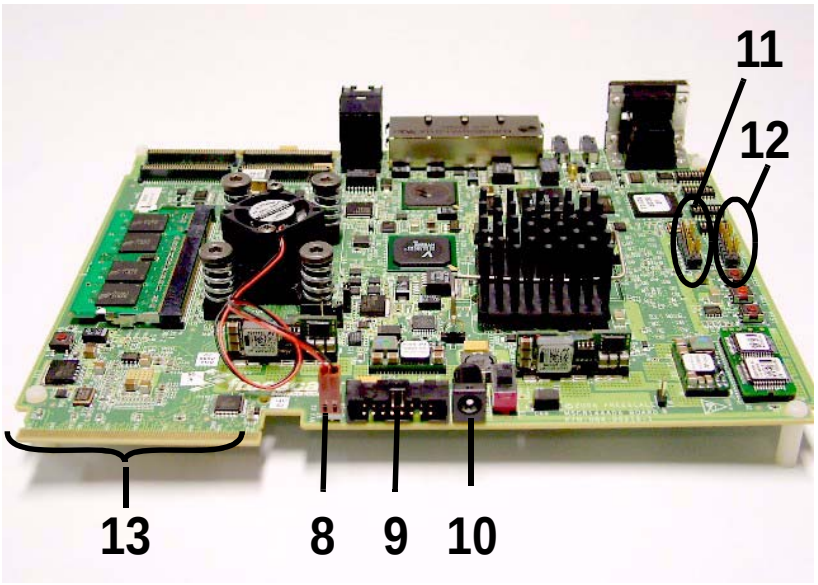


Figure 1-2. MSC8144ADS processor board External Connections (rear view)

1.4 Block Diagram

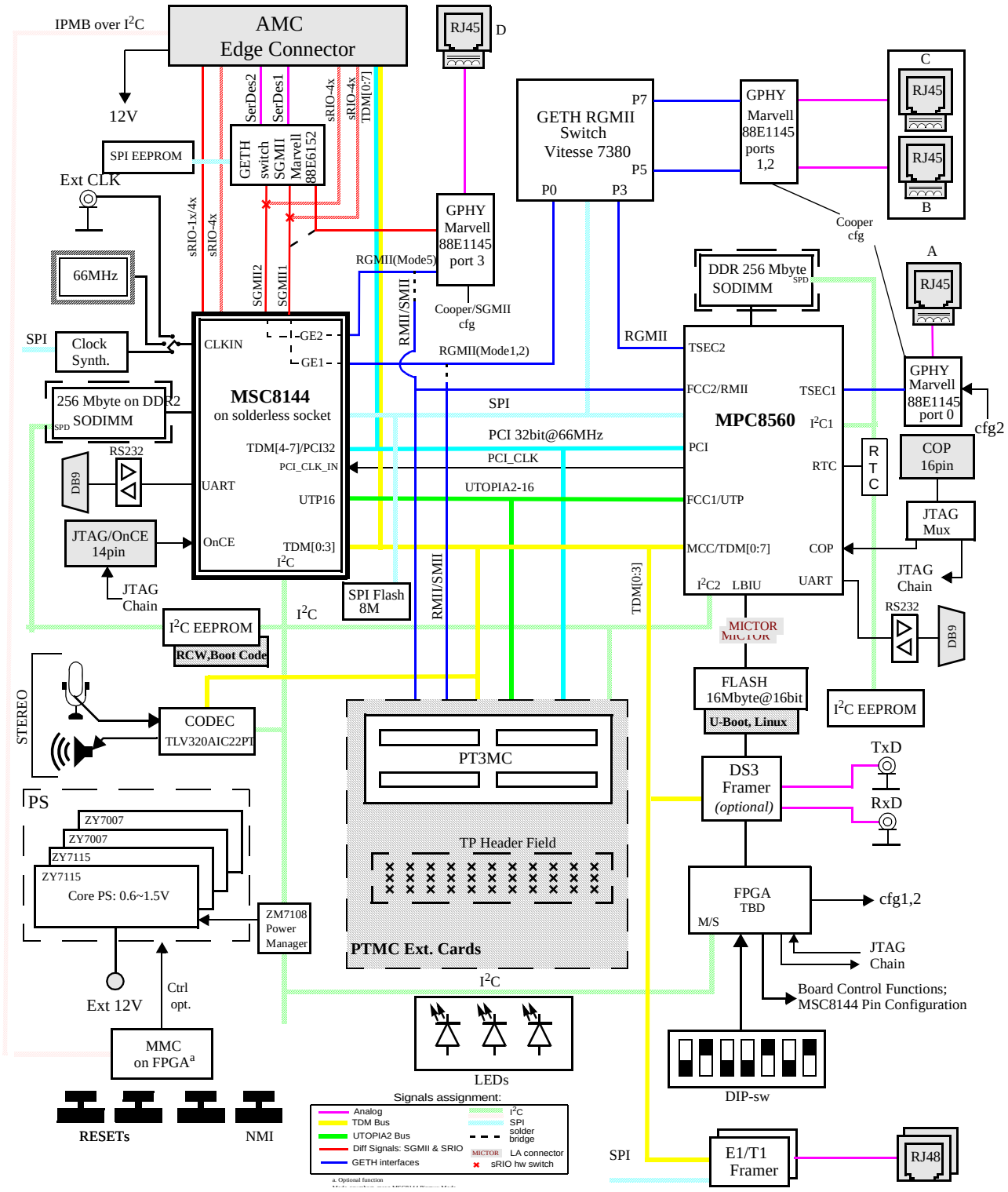


Figure 1-3. MSC8144ADS Block Diagram

1.5 Definitions, Acronyms, and Abbreviations

Table 1-1. List of Terms and Acronyms

Term	Definition
ADS	Application Development System
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
BCSR	Board Control and Status Register
BSP	Board Support Package
COP	Common On-chip Processor (JTAG Debug Port)
CS	Chip Select
DDR	Double Data Rate
DIP	Dual-In-Line Package.
DMA	Direct Memory Access
DUART	Dual UART
EEPROM	Electrical Erasable Programmable Memory
FLASH	Non volatile reprogrammable memory.
FPGA	Field-Programmable Gate Array
GETH	Giga-bit Ethernet
GPCM	General Purpose Chip-select Machine
GPL	General Purpose Line
I2C	Philips Semi Serial Bus
JTAG	Joint Test Access Group refers to the IEEE debug and test protocols
LBIU	Local Bus Interface Unit
LED	Light Emitting Diode
lsb	least significant bit
MII	Media Independent Interface
msb	most significant bit
PCI	Peripheral Components Interconnect
Phy	Physical Layer
POL	Point-of-Load DC-DC converter
PSU	Power Supply Unit
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RCW(L,H)	Reset Configuration Word (Low/High)
RTC	Real Time Clock
SGMII	Serial Gigabit Media Independent Interface
SerDes	Serializer/Deserializer
SMB	Type of Mini-RF connector

Table 1-1. List of Terms and Acronyms

Term	Definition
SMII	Serial Media Independent Interface
SODIMM	Mini DIMM Form Factor
SPD	Serial Present Detect
SPI	Serial Peripheral Interface
SRIO	Serial Rapid I/O High Speed differential interface

1.6 Related Documentation

- Freescale Documentation
  - MSC8144 Data Sheet
  - MSC8144 Reference Manual
  - MSC8144 ADS Processor Board Hardware Getting Started
  - MSC8144 ADS Using Code Warrior™ and MSC8144ADS Kit Configuration Guide
- Third Party Documentation
  - PICMG2.15 PCI Telecom Mezzanine/Carrier Card Specification

1.7 Specifications

The MSC8144ADS processor board specifications are given in Table 1-2.

Table 1-2. MSC8144 ADS Specifications

Characteristics		Specifications
Power requirements		12 V @ 4 A external DC power supply for stand alone mode. No extra power supply for AMC mode - powering from ATCA carrier board.
Operating temperature		0°C to 70°C
Storage temperature		–25°C to 85°C
Relative humidity		5% to 90% (non-condensing)
Dimensions according to triple AMC form factor:		Length: 222 mm Width: 181 mm Thickness: 1.6 mm
MSC8144 processor as slave and its interfaces		Cores run up to 1 GHz @ 1 V
Memory	Internal: M2,M3	Total: 10.96 Mbyte.
	DDR2 Module	256 Mbyte space 32 bits wide + 8-bit ECC Memory Module in SODIMM200 form factor (these are the quantities utilized from a device whose capacity is 512 Mbyte, and 64 bit). Clock = 200 MHz Data rate = 400 MHz Proprietary Interposer allows connecting a standard DDR1 SODIMM200 to the DDR2 SODIMM200 socket.
	I^2C EEPROM SPI Flash	64 kB serial EEPROM for Boot Code. 8 Mbyte serial Flash for Program Code.

Table 1-2. MSC8144 ADS Specifications (Continued)

Characteristics		Specifications
Buses	PCI	PCI specification revision 2.2 compliant. 33 MHz/66 MHz,32-bit PCI interface. 3.3-V compatible Available only when the Host (MPC8560) operates the MSC8144 as an agent (present on J1, J2 of PTMC connection)
	UTOPIA	UTOPIA level II supports 8/16 bits up to 50MHz. Slave/Host Mode are available (present on J4 of PTMC connection)
Communication ports	GETH	Two GETH Controllers with five Ethernet physical interfaces: MII, RMII, SMII (all legacy interfaces), SGMII (over SerDes), RGMII. RMII and SMII are supported over PT3MC expansion card.
	TDM	Eight TDM ports together support up to 2 K time-slots for receive and 2K time-slots for transmit -up to 256 PCM channels per link. TDM ports are present on AMC connector and on PTMC (J3): four ports for PT3MC configuration and eight ports for PT5MC board configuration.
	UART	Bit rate up to 6.25 Mbps. RS-232 transceiver allows data exchange at 115 Kbps.
	I^2C	Compliant with standard.
	SPI	Synchronous peripheral serial bus.
	SerDes	1x/4x serial RapidIO endpoint operates at 1.25 Gbaud and complies with Specification 1.2.
MPC8560 processor as host and its interfaces		Core runs at up to 667 MHz @ 1.2 V
Memory	DDR1	256 Mbyte space 64-bit wide in one standard SODIMM200. Clock - 133 MHz Data rate - 266 MHz
	Flash	16 Mbyte, may be upgraded to 32 Mbyte
Buses	PCI	PCI specification revision 2.2 compliant. 33 MHz/ 66 MHz,32-bit PCI interface. 3.3-V compatible. Acts as PCI Host. Present on J1,J2 of PTMC.
	Local Bus I^2C	Up to 166 MHz, 32-bit. Serial EEPROM 256 Kb for boot code.
Communication ports	GETH	Two TSEC Controllers with five Ethernet physical interfaces: GMII, TBI, RGMII, RTBI; configured as RGMII on the ADS.
	TDM	Eight TDM ports, shared with MSC8144 communication ports
	UART	RS-232 transceiver allows data exchange at 115 Kbps
	I^2C	Compliant with standard. Used to control peripheral devices
	UTOPIA2	8/16-bit UTOPIA level II interfaces for ATM running up to 50 MHz. Acts as a master

Hardware Preparation and Installation 2

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MSC8144ADS processor board. For more details on hardware preparation, see the Hardware Getting Started document for the MSC8144ADS processor board.

2.1 Unpacking Instructions

Note: If the shipping carton is damaged upon receipt, request carrier agent to be present during unpacking and inspection of equipment.

Caution: *Avoid touching areas of integrated circuitry; static discharge can damage circuits.*

- Unpack equipment from shipping carton.
- Refer to packing list and verify that all items are present.
- Save packing material for storing and reshipping of equipment.

2.2 Installation Instructions

To install the MSC8144ADS processor board properly, perform the following steps ***in the order indicated***:

1. Verify that Jumpers and Switches are in default positions (see **Chapter 4**, *Controls and Indicators* for a list of default positions).
2. Connect external cables in accordance with your development needs (see **Section 1.3** for details).
3. Connect PSU (to P10).
4. Move the power switch S1 to ON.
5. Verify that LEDs LD8 and LD1 display light. This indicates that board power is applied. Verify that LD3 and LD4 briefly display light. If the boot source is I^2C, LD5 will display light during code loading.
6. Check for completion of the reset sequence-indicated by all relevant LEDs reaching a steady state, according to their respective meanings. (see **Figure 2-1** for location of these LEDs, see **Table 4-6** for a more detailed description).
7. Operate the CodeWarrior™ software to verify that the board has been installed properly.

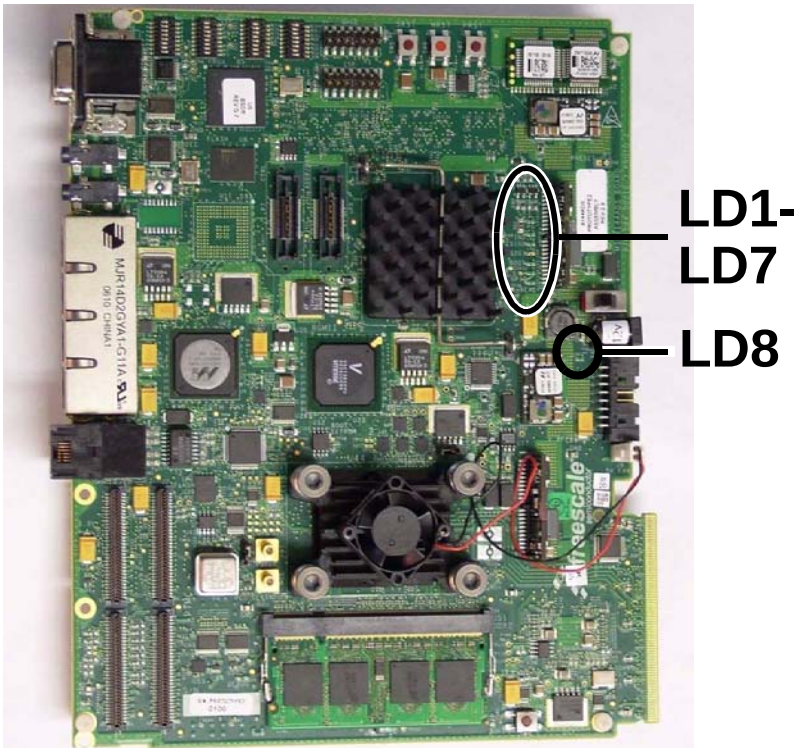


Figure 2-1. LED Locations

The LEDs operate in the following sequences during reset:

1. LD8 and LD1 light
2. LD3 and LD4 light and then go off

Memory Map 3

Each of the processors on the ADS board uses its own memory map.

3.1 MPC8560 Host Mapping for the MSC8144ADS

The MPC8560 Memory Controller governs all access to the processor memory slaves. Consequently, the memory map may be reprogrammed according to specific user needs. After performing a Hard Reset sequence, the debug host may initialize the memory controller via the JTAG/COP connector to allow additional access to bus addressable peripherals. The SDRAM DDR responds to all types of memory access including program, data, and direct memory accesses (DMA).

Table 3-1. MPC8560 Host Memory Map

Address Range	Target		Device Name	Volume in Byte	Port Size in Bits
	MPC8560 Port	Ext. Devices			
00000000–0FFFFFFF (3FFFFFFF)	DDR	DDR1 SODIMM on CS0	MT8VDDT3264H(I)Y-335 w/o ECC	256 Mbyte (1 Gbyte opt)	64
10000000–3FFFFFFF (40000000)	—	Empty Space (if 1GB DDR1 not used)	—	~66 Mbyte	—
40000000–400FFFFF	Internal 8560	—	Configuration Registers Space	1 Mbyte	32
40100000–7FFFFFFF	—	Empty Space	—	~1 Gbyte	—
80000000–9FFFFFFF	PCI			~512 Mbyte	32
80000000–87FFFFFF		MSC8144	PCI port		
88000000–8BFFFFFF		PTMC	Exp. Card		
A0000000–F7FFFFFF	—	Empty Space	—	1.5 Gbyte	—
F8000000VF8007FFF	LBIU GPCM	BCSR on CS1	Altera MAX2	32 Kbyte	8
F8008000–F800FFFF	LBIU GPCM	DS3/E3 Framer on CS2	Exar XRT79L71	32 Kbyte	8
F8010000–FDFFFFFF	—	Empty Space	—	~88 Mbyte	—

Table 3-1. MPC8560 Host Memory Map

Address Range	Target		Device Name	Volume in Byte	Port Size in Bits
	MPC8560 Port	Ext. Devices			
FE000000–FEFFFFFF (FFFFFFFF)	LBIU GPCM/UPMA	FLASH on CS0	(PC28F256P30B85)	(32 Mbyte)	16
FF000000–FFFFFFFF			Intel Strata-Flash PC28F128P30B85 (If using this 16 Mbyte option, FF000000–FFFFFFFF, and the lower 16 Mbyte are free)	16 Mbyte	

3.2 MSC8144 Mapping

The memory map defined in **Table 3-2** is only a recommendation. The user can choose to work with alternative memory mapping. It should be noted that the described mode is supported by Freescale CodeWarrior and Smart-DOS debug tools.

Table 3-2. MSC8144 Memory Map

Address Range	Target		Device Name	Volume in Byte	Port Size in Bits
	MSC8144 Port	Ext. Devices			
40000000–4FFFFFFF (5FFFFFFF)	DDR	DDR2 SODIMM on CS0	MT8HTF6464HDY-53E 512 Mbyte @ 64 bit	On-board 256 Mbyte @ 32 bit is available (512 Mbyte opt)	
50000000–BFFFFFFF (60000000– BFFFFFFF)	—	Empty Space	—	1.5 Gbyte (512 Mbyte if using the 512 Mbyte DDR2 option)	
C0000000–C007FFFF	M2 Shared	—	Internal	512 Kbyte	
C0080000–CFFFFFFF	—	Empty Space	—	255.5 Mbyte	
D0000000–D09FFFFF	M3 Memory	—	Internal	10 Mbyte	
D0A00000–DFFFFFFF	—	Empty Space	—	1 Gbyte	
E0000000–E7FFFFFF	PCI port	—	—	128 Mbyte	
E0000000–E3FFFFFF		MPC8560	PCI Port		
E4000000–E7FFFFFF		PTMC	Exp. Card		
E8000000–FEDFFFFF	—	Empty Space	—	366 Mbyte	
FEE00000–FEE3FFFF	Packet Processor	—	Internal	256 Kbyte	
FEE40000–FEEFFFFF		Empty Space	—	768 Kbyte	
FEF00000–FEF17FFF	Boot ROM	—	Internal	96 Kbyte	
FEF18000–FFFFFFFF	—	Empty Space	—	928 Kbyte	

Controls and Indicators 4

This chapter describes controls and indicators of the MSC8144ADS processor board, which includes switches, jumpers, LEDs, and push buttons.

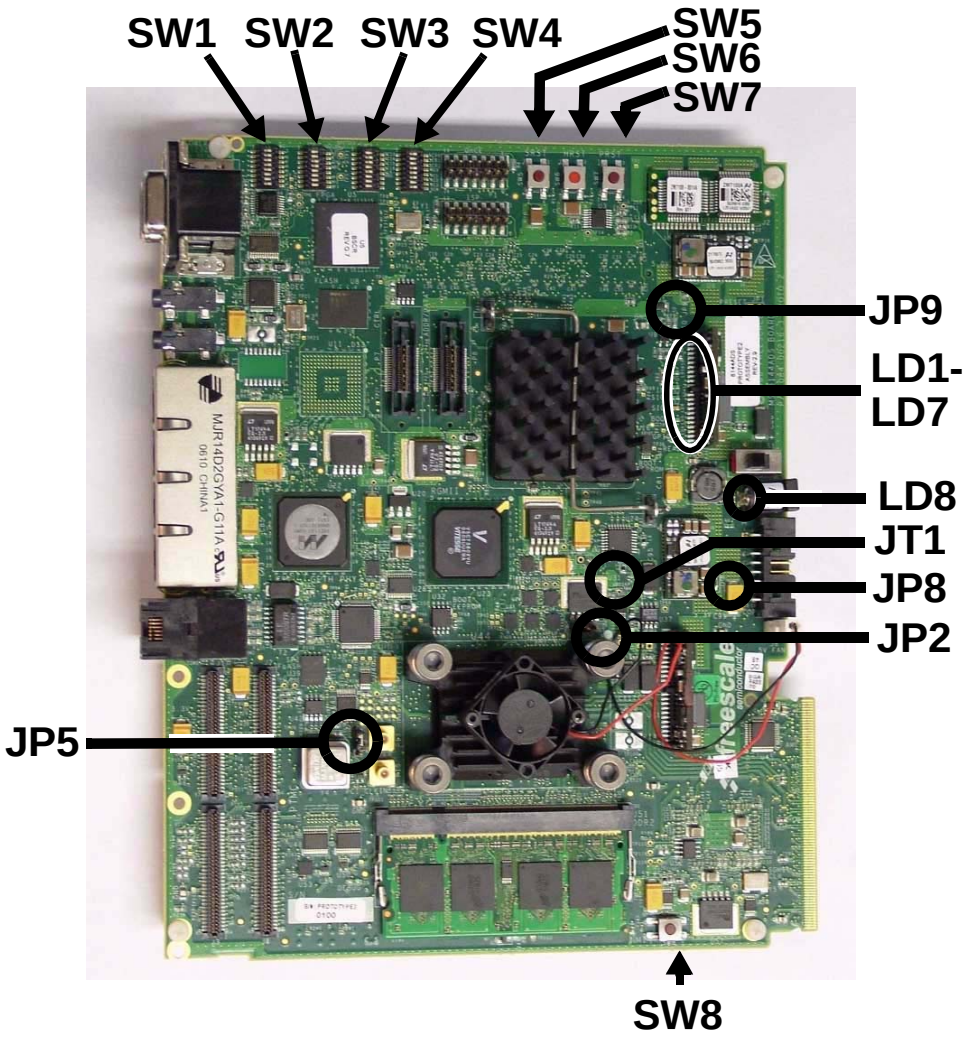


Figure 4-1. MSC8144ADS Switches, Jumpers, LEDs, Push Buttons Locations

4.1 DIP Switches

Figure 4-1 shows the locations on the board of the DIP-switches. **Table 4-1** describes the possible settings of the DIP switches. Note that when ON, the value of the switch is zero. For more detailed descriptions of the bits and fields, see the *MSC8144 Reference Manual*. Check the default positions, and verify that the board is operational before changing any settings.

Table 4-2 on page 4 shows default DIP-switch positions when the configuration word is taken from the I^2C EEPROM. Notice certain values are indicated as not specified (x). These values are taken from the EEPROM itself instead of from the DIP switch settings (which are ignored in these cases). The specific default values are the same as in 4-3, with the following exceptions:

- Pinmux = 6 (refer also to SW1.6–7)
- Boot port = EEPROM (refer also to SW3.1–3)

Table 4-1 shows default DIP-switch positions when the reset configuration word is taken from external pins.

Table 4-1. DIP Switch Settings Descriptions

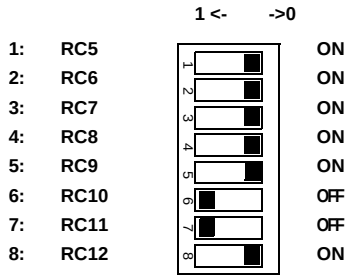
Switch	Setting Definitions
SW1 Configuration  1 <- ->0 1: RC5 ON 2: RC6 ON 3: RC7 ON 4: RC8 ON 5: RC9 ON 6: RC10 OFF 7: RC11 OFF 8: RC12 ON	**SW1.1–SW1.5: (RCW[5:9]) Device ID** (labelled RCn on board) 00000 Device ID (works together with SW4.8) For more details, see MSC8144 Reference Manual, under the RCW field **SW1.6–SW1.7: (RCW[10,11]) Pin Muxing[1:0]** 11 Sets Pin Mux Mode equal to 3 (default) 10 Sets Pin Mux Mode equal to 2 01 Sets Pin Mux Mode equal to 1 00 Sets Pin Mux Mode equal to 0 **SW1.8: (RCW[12]) Boot Port Select** (labelled RC12 on board) 0 Sets PCI as boot port (default) (works together with SW3.1–SW3.3) for more details and all options, see MSC8144 Reference Manual, under the RCW field Factory setting: '00000110

Table 4-1. DIP Switch Settings Descriptions (Continued)

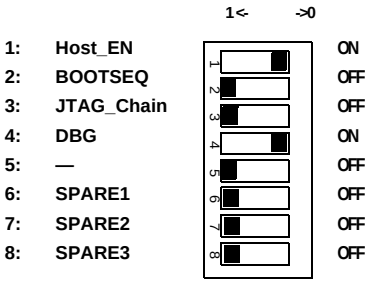
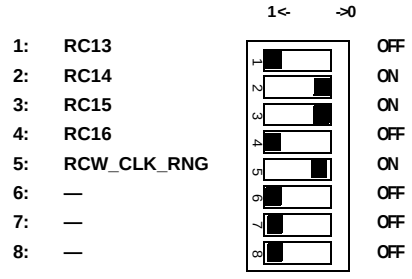
Switch	Setting Definitions
SW2 Configuration  	**SW2.1: Host (MPC8560) Enable** (labelled Host_EN on board) 0 Host Processor (MPC8560) operates normally (default) 1 Host Processor (MPC8560) disabled (placed in reset state) **SW2.2: Host (MPC8560) Boot Sequencer** (labelled BOOTSEQ on board) 0 Host (MPC8560) Boot Sequencer is enabled (boot from Host EEPROM) 1 Host (MPC8560) Boot Sequencer is disabled (default) **SW2.3: JTAG Chain** (labelled JTAG_Chain on board) 0 Enables Chain Mode for MSC8144 and MPC8560 - one JTAG connection for both, and both are viewed on one CodeWarrior instance) 1 Disables Chain Mode; MSC8144 and MPC8560 can be debugged independently, with a CodeWarrior instance and JTAG connection for each one (default) **SW2.4: Debug Enable** (labelled DBG on board) 0 MSC8144 enters Debug Mode after reset (default). See MSC8144 Reference Manual for more details 1 MSC8144 does not enter Debug Mode, but operates normally. **SW2.5–SW2.8: Reserved** (SPAREn) 1111 Default Factory setting: ’01101111
SW3 Configuration  	**SW3.1–SW3.3: (RCW[13:15]): Boot Port Select** Set PCI as boot port 100 PCI(default) DDR 256 Mbytes (default) (works together with SW1.8) for more details and all options, see MSC8144 Reference Manual, under the RCW field **SW3.4: SGMII, sRIO Mode (RCW[16])** 1 Enables SGMII1, SGMII2, and sRIOx1 (default) (works together with SW4.7) for more details and all options, see MSC8144 Reference Manual, under the RCW field **SW3.5: Clock Range (RCFG_CLKIN_RNG)** (RCW_CLK_RNG) 0 Clock_in frequency range is less than or equal 66 MHz (default) 1 Clock_in frequency is greater than 66 MHz. **SW3.6–SW3.8: Reserved** 111 Default Factory setting: ’10010111’

Table 4-1. DIP Switch Settings Descriptions (Continued)

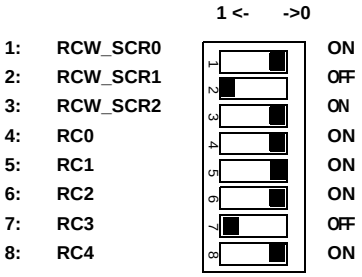
Switch	Setting Definitions
SW4 Configuration  	**SW4.1–SW4.3: RCW_SRC[0:2].** Reset configuration words source selection. 011 Some bits of the reset configuration word are loaded from external pins and others from the PCI 010 Reset configuration word is loaded from an I2C Boot EEPROM (default) For more details and all options, see MSC8144 Reference Manual, under the RCW_SRC field **SW4.4–SW4.6: (RCW[2:0]) MODCK[0:2]** “000 MODCK is 0 (default) For more details and all options, see MSC8144 Reference Manual, under the RCW and MODCK fields **SW4.7: SGMII, sRIO Mode (RCW[3])** 1 Enables SGMII1, SGMII2, and sRIOx1 (default) (works together with SW3.4) for more details and all options, see MSC8144 Reference Manual, under the RCW field **SW4.8: Device ID** 0 Device ID (default) (works together with SW1.1–SW1.5) For more details, see MSC8144 Reference Manual, under the RCW field Factory setting: '01000010'

Table 4-2. Default Settings (boot from EEPROM)

Switch	1	2	3	4	5	6	7	8
SW1	x	x	x	x	x	x	x	x
SW2	0	1	1	0	1	1	1	1
SW3	x	x	x	x	0	1	1	1
SW4	0	1	0	x	x	x	x	x

Table 4-3. Default Settings (boot from PCI)

Switch	1	2	3	4	5	6	7	8
SW1	0	0	0	0	0	1	1	0
SW2	0	1	1	0	1	1	1	1
SW3	1	0	0	1	0	1	1	1
SW4	0	1	1	0	0	0	1	0

Table 4-4 below shows the default clock mode. Check the default positions (as shown in **Table 4-3**) and verify that the board is operational before changing any settings.

Table 4-4. MSC8144 Clock Mode

Chip	Mode	Value
MSC8144	CLKIN, PCI_CLKIN	66 MHz
	Cores	800 MHz
	System Clock	400 MHz
	M3	200 MHz
	DDR	400 MHz
	QE	400 MHz
	sRIO	1.25 GHz
MPC8560	CLKIN, PCI	66 MHz
	Core	667 MHz
	CPM & CCB	266 MHz
	DDR	266 MHz
	LBC	33 MHz

4.2 Jumpers

Figure 4-1 shows the locations of the jumpers. MSC8144ADS processor board jumpers settings are described in 4-5, below.

Table 4-5. Jumpers

Jumper	Description
JT1	Soldered jumper. Sets GE interface voltage to 2.5V or 3.3V. • **CLOSED**, 2.5V • **OPEN**, 3.3V Default: Closed
JP2	Sets sRIO VDDSXP I/O Power Voltage level: • When **CLOSED**, 1.0V • When **OPEN**. 1.2V Default: Open
JP5	Selects MSC8144 CLOCKIN source: • When 1-2 is **CLOSED** source is in-socket clock oscillator • When 2-3 is **CLOSED** source is external (pulse generator) Default: 1-2
JP8	A test point that indicates the functionality of the 3.3V line
JP9	A test point that indicates the functionality of the 5V line

4.3 LEDs

Figure 4-1 shows the locations of the MSC8144ADS processor board LEDs that are described in **Table 4-6**.

Table 4-6. LED Descriptions

No.	Name	Color	LED On	LED Off
LD1	PG	Green	Power Good	Power Supply fail(*)
LD2	IND	Green	BCSR4.5 is low	BCSR4.5 is high
LD3	SIG0	Green	BCSR0.6 is low, or SRESET is asserted	No SRESET & BCSR0.6 is high
LD4	SIG1	Red	BCSR0.7 is low, or HRESET is asserted	No HRESET & BCSR0.7 is high
LD5	BOOT	Green	Boot is from I2C	Boot is not from I2C
LD6	GPIO	Green	For future use	
LD7	READY	Green	Host(8560) Processor in Ready state	Host(8560) Processor not in Ready state(*)
LD8	12V	Green	Indicates external power is ON(*)	
LD9	DEBUG	Green	MSC8144 in Debug mode	MSC8144 not in Debug mode
(*) Critical indicator				

4.4 Push Buttons

See **Figure 4-1** for the locations of the board push buttons. **Table 4-7** below describes their functionality.

Table 4-7. The MSC8144ADS Push Buttons

Push Button	Switch Color	Description
SW5 Soft Reset	 SRESET	Pressing button SW5 results in a Soft Reset for the MSC8144 only. Despite the reset, clock and chip-select data contents are retained.
SW6 Hard Reset	 HRESET	Pressing button SW6 results in a Hard Reset for the MSC8144 only.
SW7 Power-on-Reset	 PRESET	Pressing button SW7 results in Power-On-Reset for ***all components*** on the MSC8144ADS processor board.
SW8 NMI (Abort)	 NMI	Pressing button SW8 results in aborting program execution by issuing a level 0 interrupt to the MSC8144 (only). Sets pin EE0 to high.

ADS Functional Description 5

The ADS functional components are described in the following sections.

5.1 MSC8144 Memory System

The MSC8144ADS has two types of memory devices: DDR2 and DDR1.

5.1.1 DDR2

The DDR2 device is a SODIMM made by Micron (MT8HTF6464HDY-53E), with 512 Mbyte and rated at 533 MHz, with a width of 64bits. Half of its width is used (32 bits), in the 4 × 8-bit mode, giving a maximum effective capacity of 256 Mbyte. The DDR2 draws 1.8 V from the TPS51116 power supply on the MSC8144ADS.

5.1.2 DDR1

The MSC8144ADS can use two DDR1 SODIMM modules. These have ECC functionality and include 3 or 5 DDR1 parts with a 16- or 8-bit size, respectively. The DDR1 modules each draw 2.6 V from TPS51116 power supply on the MSC8144ADS.

5.1.3 DDR Connection

The main memory module used is the Micron DDR2 SODIMM MT8HTF6464HDY-53E, with 512 Mbyte, working at 533 Hz, and 64 bits wide. However, since the MSC8144 has a 32-bit DDR memory controller, therefore, only half of the DDR2 device capacity is utilized and only half of the data port DQ[31–0] must be connected. Another result of this is that the SODIMM effective volume is 256 Mbyte.

Address and control lines are terminated to VTT on the universal DDR power supply (TPS51116) that provides power to the DDR1 memory as well. SODIMM Data Lines omitted in the interface are terminated to VDD. When the MSC8144 Memory controller (which has a maximum size of 32 bits) is configured to have a 16-bit port size, the unused 16-bits are tied to VDD. The ECC byte remains the same as for a 32-bit configuration.

When the DDR1 module is inserted in the DDR interposer, the DDR pinout causes the MSC8144 to be signalled to supply its 2.6 V voltage.

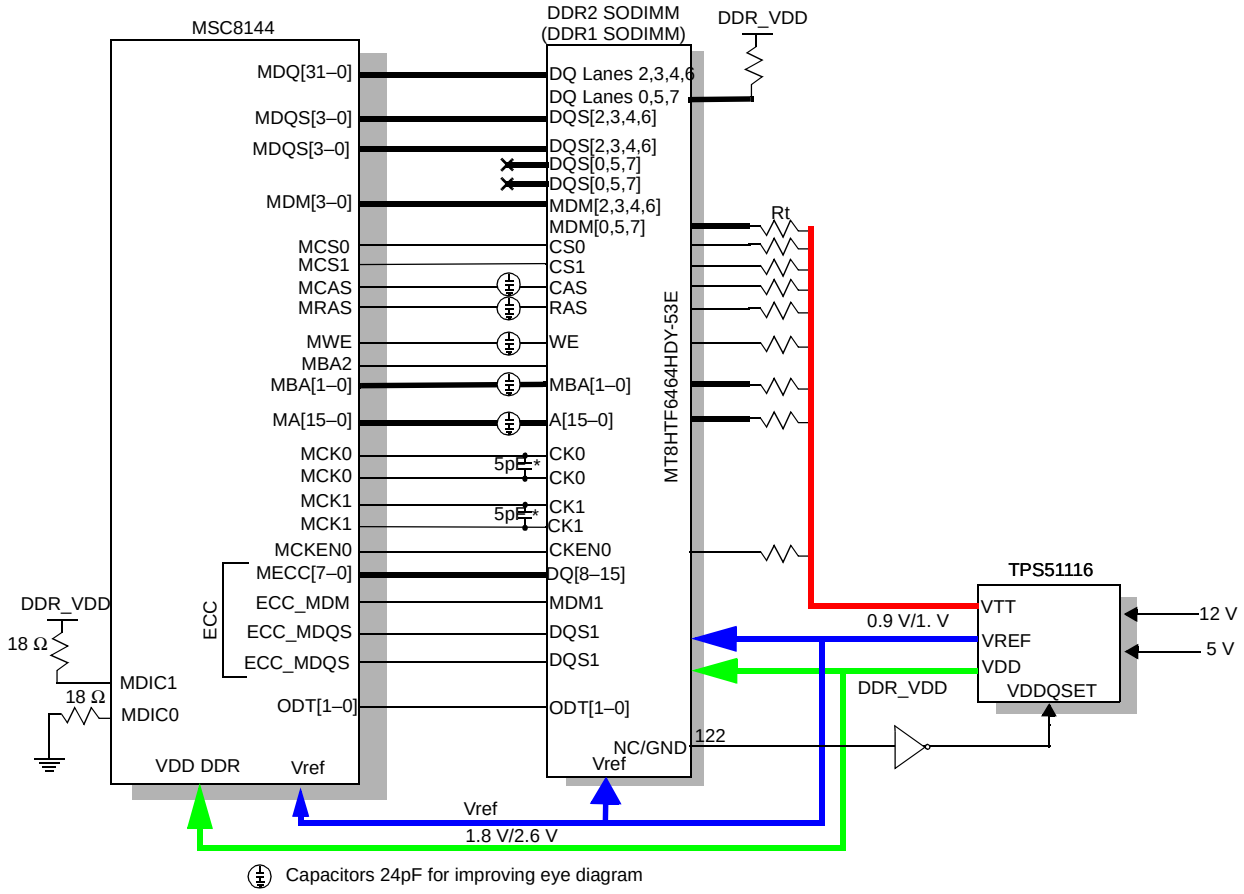


Figure 5-1. DDR2 SODIMM Interconnection

5.1.4 Power for DDR Devices

The synchronous buck controller TPS51116 by TI provides a complete power supply for both the DDR1 and DDR2 memory devices. The VDDQSET input pin selects the voltage for DDR2 or DDR1. Available modes are shown in **Table 5-1**. The SPD Serial I^2C EEPROM mounted on the DDR2 SODIMM is powered from the system 3.3 V power source..

Table 5-1. VDDQSET and Output Voltage

VDDQSET	VDDQ	VTTREF & VTT	Memory System
GND (GND on SODIMM)	2.6 V	$V_{VDDQ}/2$ = 1.3 V	DDR1
5 V (NC on SODIMM)	1.8 V	$V_{VDDQ}/2$ = 0.9 V	DDR2

5.2 MPC8560 PCI Host Bus

The PCI bus has a width of 32 bits, and connects the MPC8560 host processor with the MSC8144 and the PTMC expansion connector. If you are working with a PCI bus, the host MPC8560 must be enabled (clear SW2[1] to 0). If the MPC8560 is not enabled, the PCI bus is not functional.

A few notes on working with the PCI bus between the host MPC8560 and the MSC8144:

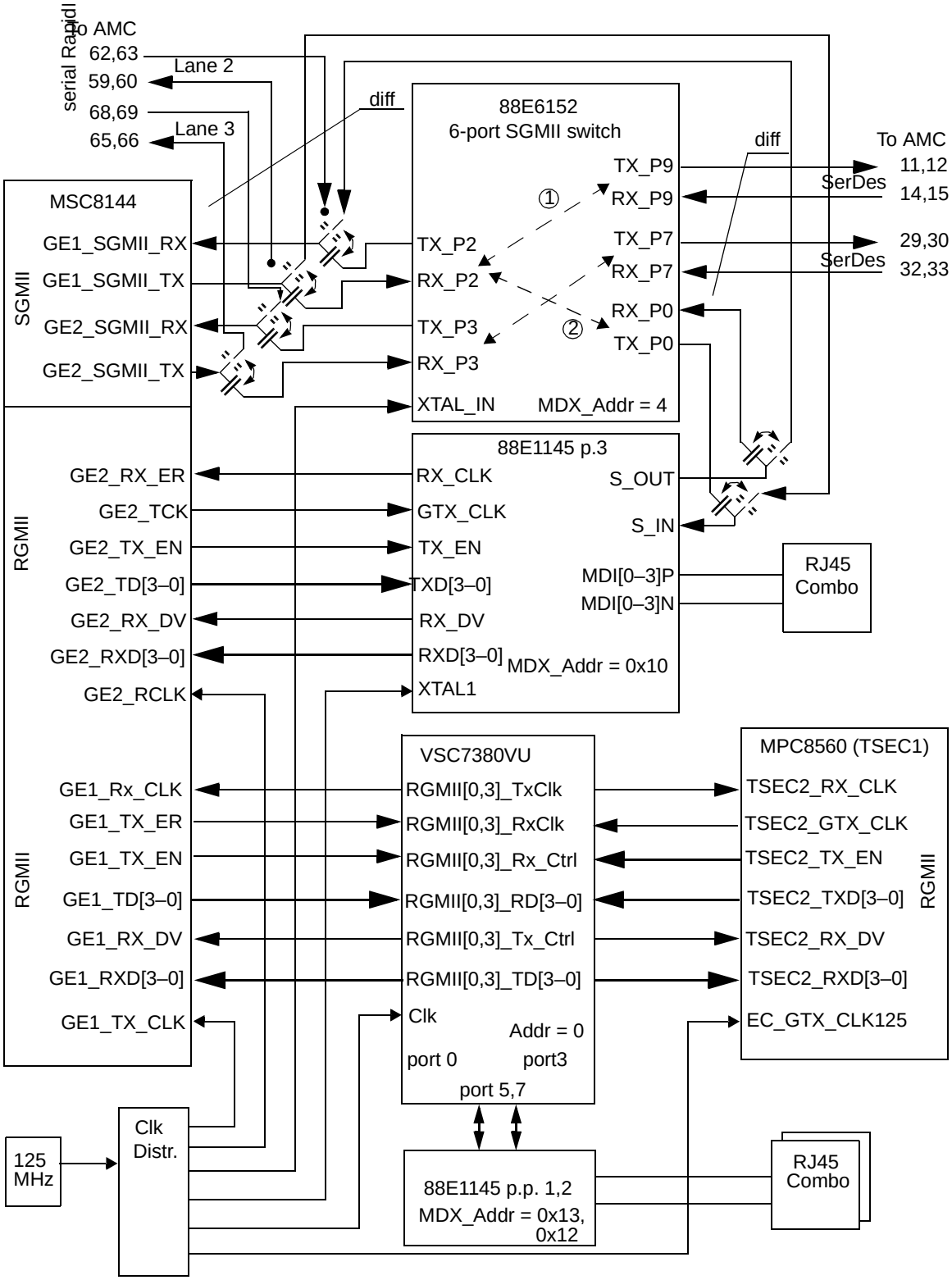
- The MSC8144 can work with a PCI, UTP, or TDM protocols on the PCI bus.
- If the user has enabled the MSC8144 to work with the PCI protocol, the MPC8560 PCI bus must also be enabled.
- If the user has enabled the MSC8144 to work with UTP (16-bit) protocol, the MPC8560 PCI bus must be disabled.
- If the user has enabled the MSC8144 to work with UTP (8-bit), the MPC8560 PCI bus can function in addition to the UTP, but it is not required.
- If the user has enabled any of ports 0–3 in TDM, the MPC8560 PCI bus can also function.
- If the user has enabled any of ports 4–7 in the TDM bus, the MPC8560 PCI bus cannot function, and must be disabled.

Note: Failure to disable (or enable) any of the above options prevents correct PCI bus operation.

The default I/O multiplexing mode is 3, which means that the default boot values are taken from the MPC8560 via the PCI bus, and that the MSC8144 functions as an agent.

5.3 GETH Interface Switch

The GETH switch is implemented by a Vitesse VSC7380VU GETH Switch. It is an 8-port Integrated Gigabit Ethernet Switch SoC, configured with an RGMII interface, and working at any one of three speeds (10/100/1000 Mbps). The switch configures two RGMII ports: One connected to the host MPC8560 (TSEC2 (MAC1)), and the other connected to the MSC8144 (G2 (MAC0)), both via the SPI bus. Three analog ports are tied to the RJ-45 connectors and the MSC8144 port G1 through the GETH phy. This interconnection allows exchanging of data between the host and the MSC8144, and to connect any port out to the LAN. **Figure 5-2** shows the GETH interconnection.



Note: The Host TSEC2 port configured as RGMII is connected to the Quad 88E1145 phy port 0.

Figure 5-2. GETH Interconnection Diagram

5.4 Serial RapidIO Ports

The MSC8144 serial RapidIO port Lane 0 (serial RapidIO 1x) is connected directly to the AMC edge connector. See **Table 6-3** on page 6-11 for a detailed list of these connections. It is possible to connect the serial RapidIO Lanes 2 and 3 to the AMC edge connector or the SGMII switch 88E6152 ports 2 and 3 when configured as SGMII ports 1and 2, but you must assemble appropriate serial capacitors for this configuration. Freescale configures the ports using customer requirements when the board is ordered

5.5 TDM Ports and Peripheral

The TDM ports use a 16-bit voice codec and a T1/E1 interface.

5.5.1 16-bit Voice Codec

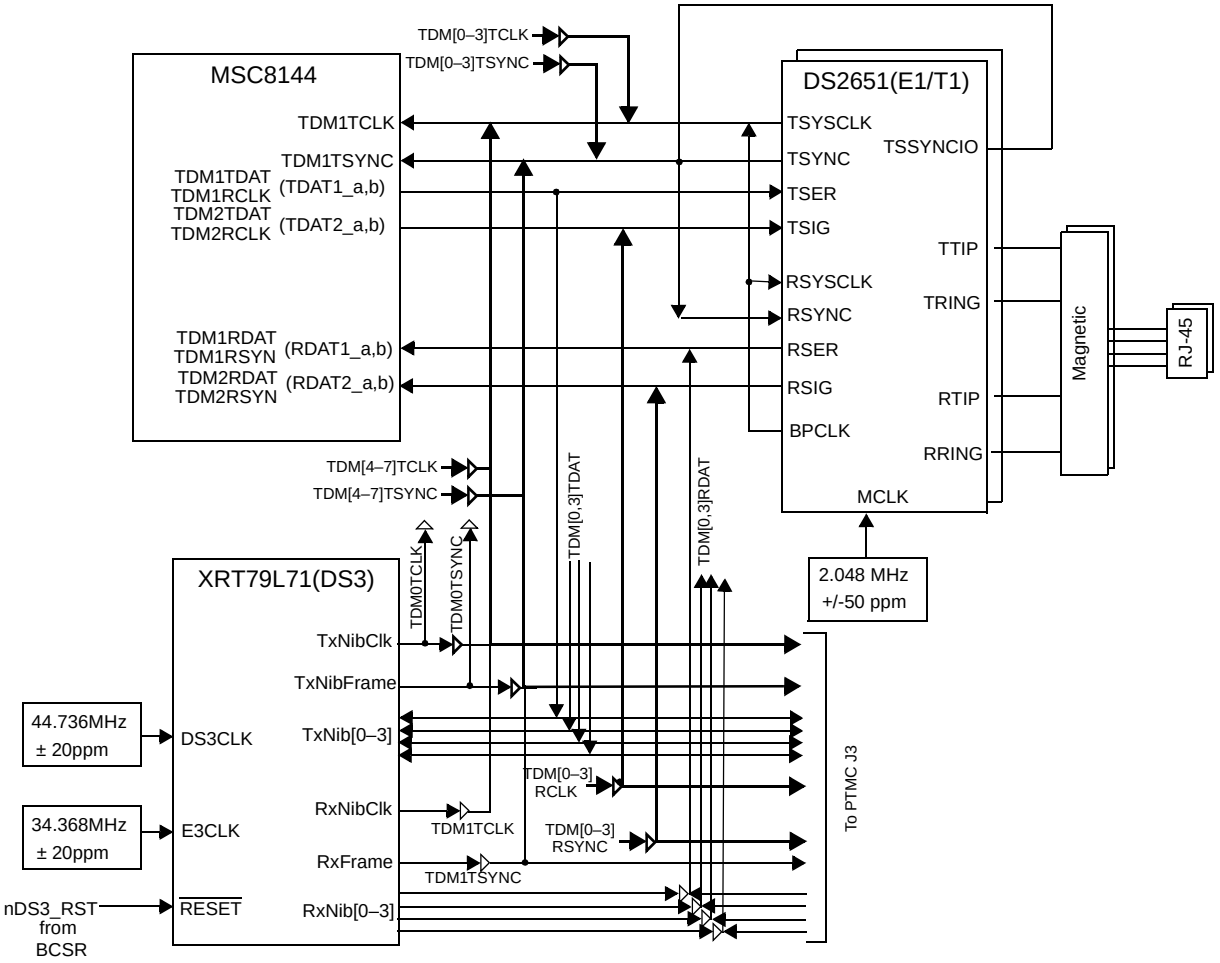
The codec is a TI dual TLV320AIC22PT that features two analog-to-digital converter (ADC) channels and two digital-to-analog converter (DAC) channels that can connect to a handset, headset, speaker, microphone, or a subscriber line via an analog crosspoint. The codec supports 8-Bit A-Law/µ-Law compounded data or 16-bit linear data complying with G.711. It also supports 8- and 16-kHz sampling rates, and its filters comply with G.712 and G.722 standards. Programming of the codec is performed via the I^2C interface from the Host processor (MPC8560), the MSC8144 or the FPGA I^2C controller. Power down signal CODEC_EN from bit BCSR0[0] isolates the codec drivers from TDM0 bus. The codec is enabled by default.

5.5.2 E1/T1 Framer

The E1/T1 framer is implemented using the Dallas DS26521, a single chip framer and LIU combination for T1, E1, and J1 applications that supports both long haul and short haul lines. The transceiver consists of a line interface unit, framer, HDLC controller, elastic store, and a TDM backplane interface (H.100). The framer is configured via the SPI bus. Access is available from the SPI port of the MPC8560 as well as via the MSC8144 SPI. The line interface is via a transformer and dual RJ-45 connector.

The TDM interface to the MSC8144 TDM port is based on a backplane configuration with an elastic store enable. All clocks are produced from a master clock of 2.048 MHz. The MSC8144 TDM ports 1 and 2 are programmed in Clock/Sync shared mode. Data channels use TDM port 1 lanes 1 and 2. Signaling channels use TDM port 2 lanes 1 and 2. See **Table 5-2** on page 5-7 for the configuration modes of all peripherals regarding TDM. For each framer (TDM Enable and Reset), there are two sets of control signals: BCSR0[1], BCSR2[4] and BCSR0[2], and BCSR2[5] that allow isolation of the framer outputs.

5.5.3 TDM Bus Interconnection



Note: XRT79L71 acts in Clear-Channel Framer Mode with 44.736MHz (DS3) or 34.368MHz clock (E3).
▷ -denotes three-state buffer or Hi-Z driver state

Figure 5-3. TDM Scheme A

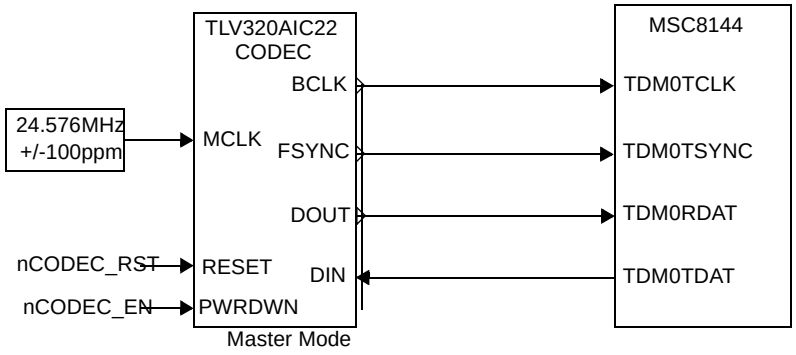


Figure 5-4. TDM Scheme B

Table 5-2. TDM Peripherals Configuration Modes

Device	MSC8144/MPC8560 Unmultiplexed TDM Ports				Comment
	TDM0	TDM1	TDM2	TDM3	
XRT79L1 DS3/E3 Framer	Bit 0	Bit 1	Bit 2	Bit 3	Nibble-Parallel Mode for DS3/E3 CTS independent for receive/transmit for MCS8144 TDM
2xDS2651 E1/T1 Framers	—	Data:(FR1+FR2)	SIG(FR1+FR2)	—	MSC8144 TDM Link A,B are in Shared Mode
TLV320AIC22CPT Codec	Two ch. 16-bit on TS 0–3 with AD0,AD1 = 0	—	—	—	CODEC Master Mode TDM0 works in clk&sync common mode

5.6 RS-232 on UART

Two RS-232 serial interfaces are connected to the UART ports of the MPC8560 and the MSC8144. The RS-232 connections assist in user applications and, further, provide convenient communication channels for both the terminal and host computer. Using a lone 3.3 V single power supply with disable mode, the MAXIM MAX3221 transceiver internally generates RS-232 levels during which receive buffers are tri-stated. When asserting (low) the RS-232 EN bit in BCSR0[3], the MSC8144 UART transceiver is enabled. When the bit is cleared, the receiver outputs are tri-stated and the transceiver is disabled. The MPC8560 RS-232 transceiver is always enabled. Dual stacked 9-pin female D-Type RS-232 connectors are configured to connect directly (via a flat cable) to a standard IBM-PC-like RS-232 connector. Note the figure, **Figure 5-5** shows the RS-232 connector pinouts. Directions I and O are relative to the on board processors (for example, I means input to the ADS). The lower connector belongs to MSC8144 and the upper to the MPC8560 UART. The RS-232 connector is intended for null-modem connectivity.

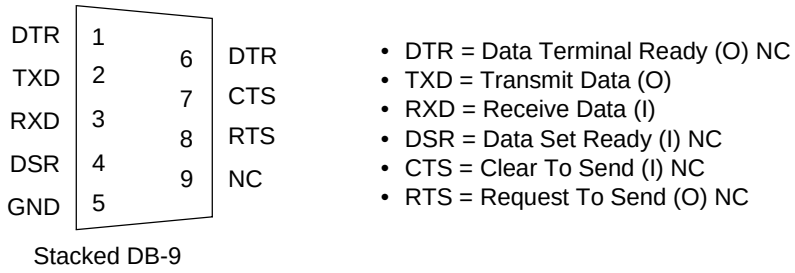


Figure 5-5. **RS-232 Serial Port Connectors**

5.7 I²C Bus Interconnection

There are two I²C on-board bus tied variant devices. **Table 5-3** and **Table 5-4** summarize their features:

Table 5-3. I²C Bus 1 Addressing

Number	Device Type	Master/Slave	Address
1	MPC8560(host) I²C1	M/S[a]	—
2	I2EEPROM 256 kb -boot sequencer	S	50h
3	SPD DDR1 MPC8560	S	51h
4	RTC - Real Time Clock	S	68h

a. Slave Mode is available but not used on the board

5.7.1 Serial EEPROM for MPC8560 Boot

Table 5-4. I2C Bus 2 Addressing

Number	Place	Device Type	Master/Slave	Address
1	On-Board	MSC8144	M/S	-/57h[a]
2		MPC8560(host) I²C2	M/S	—
3		FPGA JTAG-to-I²C controller	M/S[b]	—
4		I2EEPROM 2566 kb boot to MSC8144	S	50h
5		SPD DDR2 MPC8144	S	51h
6		ZM7108 Power Manager	S	28h
7		TLV320AIC22PT CODEC	S	70h
8		I²C Expander 1	S	20h
9		I²C Expander 2	S	21h
10	Off-Board	PTMC SMII I²C EEPROM	S	54h
11		PTMC RMII I²C EEPROM	S	55h

a. Boot setting

b. Slave Mode allows to verify MSC8144 multi device configuration mode

The serial EEPROM is an I²C-compatible electrically erasable programmable 256Kbit memory (EEPROM) organized as 32 K × 8. Serial interface supports 400KHz protocol. Hardware write pin is controlled by the BOOTWP bit BCSR0[4]. Its default value is high, which protects the device against undesirable write operation. Chip Enable pins E0, E1, and E2 are grounded to provide MPC8560 boot function.

5.7.2 Serial EEPROM for MSC8144 Boot

The serial EEPROM for the MSC8144 is the ST M24512. This device is an I²C-compatible electrically erasable programmable 512 Kbit memory organized as 64 K × 8. The serial interface supports a 400 KHz protocol. Its hardware write pin is controlled by the GPIO19 pin of the MSC8144. A pull-up on the write control input protects the EEPROM device against undesirable write operation. The device carries a built-in 4-bit Device Type Identifier code (1010) in accordance with the I²C bus definition. Chip Enable pins E0, E1, and E2 are grounded to provide MSC8144 boot function. Since the MSC8144 I²C bus is shared with the I²C bus of MPC8560 CPM module (bus port 2 of the host), the boot code may be prepared by the host software.

5.7.3 RTC

The device used for the real-time clock (RTC) is the Dallas DS1374. This device is controlled via the I²C port 1 of the MPC8560 host processor at address 0x68. An on-chip oscillator circuit uses a customer-supplied 32.768 kHz crystal to keep time. Square-wave output SQW is used to generate the programmable square-wave signal used on the RTC input of the host. The output default frequency is 32.768 kHz. Upon reset, the RST pin has a floating value.

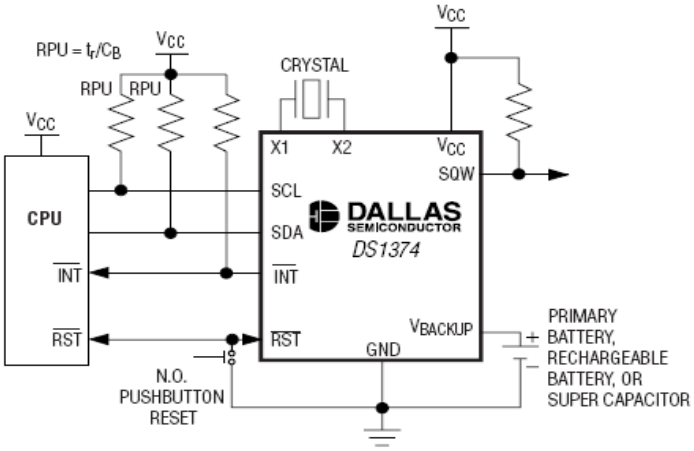


Figure 5-6. RTC Connection Diagram

5.7.4 Codec

The codec resides at address 0x70 on the I²C bus, port 2 of the host MPC8560. The I²C interface is provided to program the registers of the TLV320AIC22C in situations where programming them through the serial interface is not convenient. Below is summary info about the TLV320AIC22C internal register functions:

- Registers 1–5 and 15 are used to control codec 1.
- Registers 6–10 and 16 are used to control codec 2.
- Registers 11–14 and 17 are used to configure the device inputs, outputs, and clocking.
- Register 21 is used for Device ID and preamp control.

5.7.5 Power Manager

The power manager is the Power-One ZM7108 controller, and this device stores all power system parameters. Access to it is available from a shared I^2C bus and can be provided from the host MPC8560 or from the MSC8144. Updated values for this controller may be programmed in internal non-volatile memory.

5.8 SPI Bus

There are two SPI master devices (MPC8560 and MSC8144) and four slave devices (two DS26521 E1/T1 Framers, a 7380 RGMII switch, and an ICS30703 Clock Synthesizer). Serial Flash memory is accessed from MSC8144 only. The SPI bus connection is shown in **Figure 5-7**.

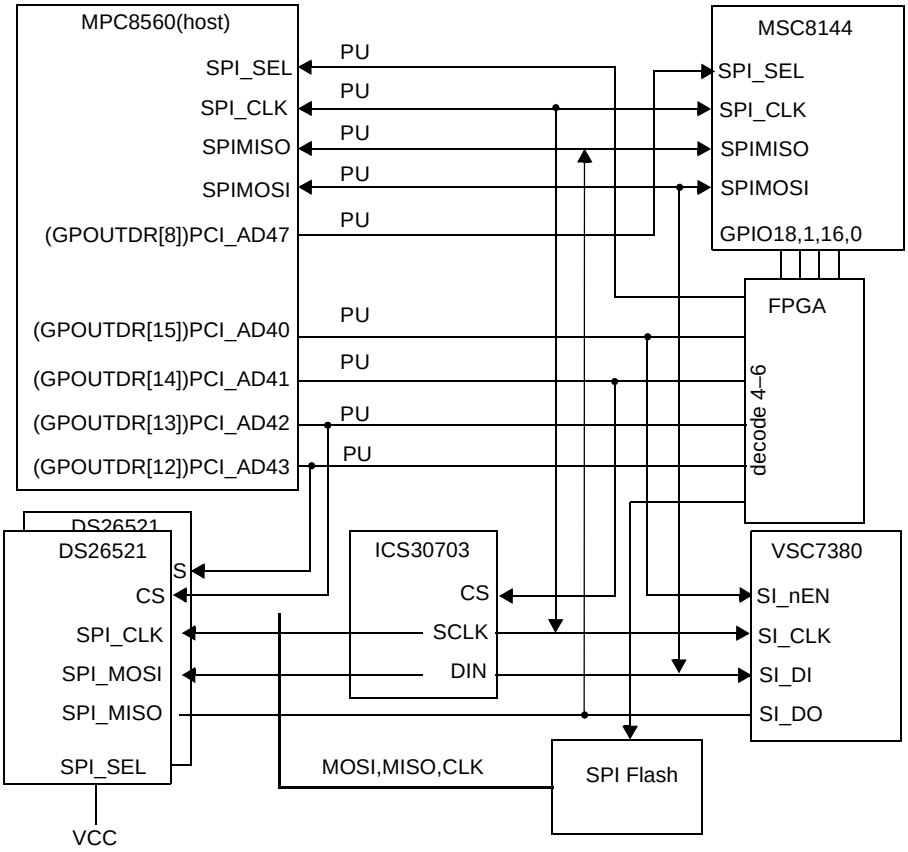


Figure 5-7. SPI Bus Devices

Four GPIO pins (GPIO18,GPIO16,GPIO1,GPIO0) enable selecting the different SPI bus parts. The coding for this is shown in **Table 5-5**. This feature requires a disable signal on the SPI Select lines driving from the Host (MPC8560). This may be achieved while the Host stays in reset with DIP-switch SW2[1] in the OFF position.

Table 5-5. MSC8144 SPI Select Coding

GPIO18,GPIO1, GPIO16,GPIO0	SPI Bus Device Select	Note
0001	RGMII Switch VSC7380	
0010	ICS30703 Clock Synthesizer	
0011	DS26521-1 E1/T1 Framer	
0100	DS26521-2 E1/T1 Framer	
0101	MPC8560 SPI as slave	
0110	Serial Flash M25P64	
other	All disable	default state

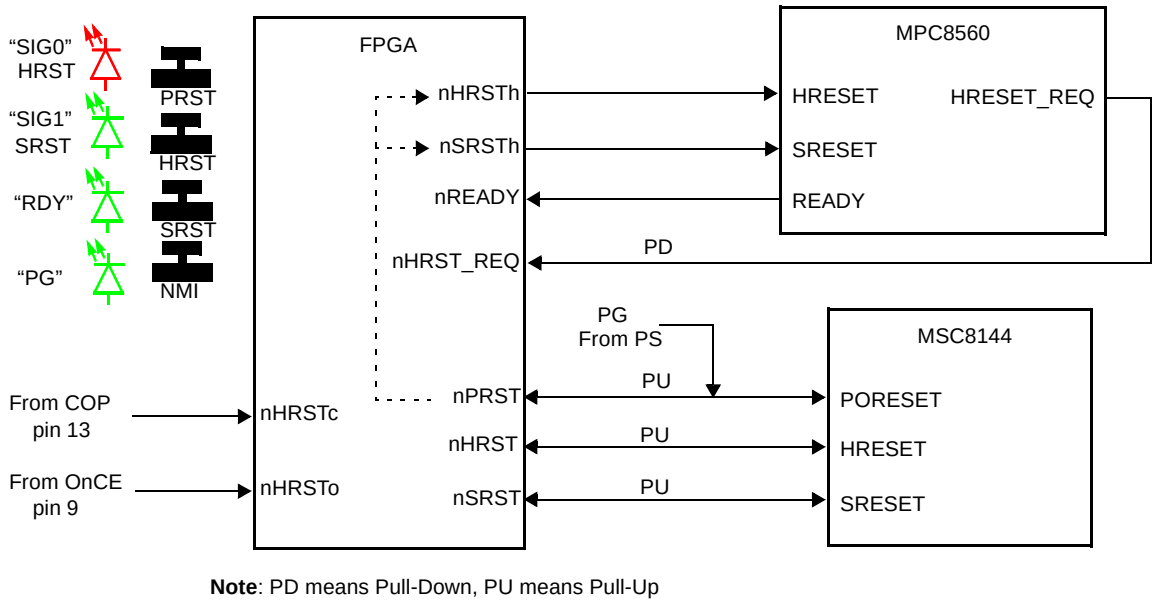
The M25P64 is a 64 Mbit (8 M × 8) Serial Flash produced by ST. Serial SPI Flash is used as indirect boot memory for the MSC8144 for large-size code (>= 64 kB) segments from the I^2C Boot EEPROM. The memory is accessed by a high speed SPI-compatible bus. By using the Page Program instruction, the memory can be programmed from 1 to 256 bytes at a time. The Write Protect (WP) input allows the user to freeze the size of the area of memory that is protected against program or erase instructions when low. The WP pin is controlled from the MSC8144 GPIO20. To enable write operation, configure GPIO20 as an output and to drive the high level.

5.9 Reset Operation and Configuration

This section describes overall reset connectivity on the ADS board and how the power-on reset and hard reset sequences function.

5.9.1 Reset Connectivity

Figure 5-8 shows the reset connectivity scheme. **Section 5.9.2** and **Section 5.9.3** describe the reset procedures.



Note: PD means Pull-Down, PU means Pull-Up

Figure 5-8. ADS Reset Scheme

5.9.2 PORESET Configuration

When $\overline{\text{PORESET}}$ is deasserted, six signals are sampled: DDR_VSEL, GE1_VSEL, GE2_VSEL, CLKINRNG, LDFAIL, and SOURCE[0–2]. The CFG_RCW [0–16] or HCW for Reduced Configuration Mode is also sampled during the assertion of $\overline{\text{PORESET}}$. Default settings are listed below:

- SOURCE[0–2] = 011 meaning Reduced Configuration Mode.
- DDR_VSEL = 0 to support DDR2.
- GE1_VSEL and GE2_VSEL are both 1 for GETH 2.5 V operation for RGMII mode.
- CLKINRNG = 0 for CLKIN 66 MHz.

When the reset configuration is loaded from I^2C EEPROM, the LDFAIL output becomes high which indicates boot error.

These initiate values are defined by DIP-switch values latched into the FPGA BCSRs during $\overline{\text{PORESET}}$ and driven towards the appropriate MSC8144 pins until $\overline{\text{SRESET}}$ is deasserted. The RCW[0–16] configuration signals used for Reduced Configuration Word apply the similar way.

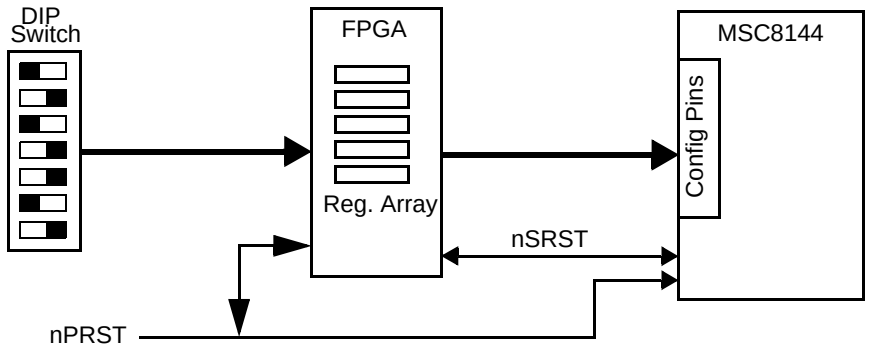


Figure 5-9. Configuration Scheme

5.9.3 Hard Reset Configuration

There are two reset systems on the board:

- Host processor (MPC8560) reset
- MSC8144 reset

The JTAG debug access for the processors is independent: via the COP connector for the MPC8560, and via the OnCE connector for the MSC8144. There are two reset signals: (nHRSTh and nHRST), and these initiate the appropriate processor and its peripherals separately. The user can configure the Board so that the JTAG interface is connected in a chain. This means that debug access to both processors is available from the OnCE header and a debugger will initiate all board devices with a single reset signal (in this case, the two reset signals nHRSTh and nHRST have a logical connection in the FPGA). In additional any MPC8560 internal reset will reset the MSC8144 as well.

Table 5-6 and **Table 5-7** show the Reset Configuration Word settings for normal ethernet and reduced mode Ethernet (RMII, SMII) configurations.

Table 5-6. RCW Low

Bits	Name	Meaning	Normal Mode from Boot EEPROM		Reduced Mode RS[0-2] within '011' to '111	
			Setting	Value	Setting	Value
31–29	-	Reserved	Reserved	000	Reserved	000
28–23	PTE	RapidIO Prescale Timer Enable	RIO prescaler timer enabled.OCeaN clock is 200 MHz	011000	RIO prescaler timer enabled.OCeaN clock is 200 MHz	011000
22	-	Reserved	Reserved	0	Reserved	0
21-20	RS_RCS	RapidIO/SGMII Reference Clock Select	RCW3. Selects whether to enable or disable power to the RapidIO and Ethernet blocks.	-	RIO/SGMII reference Clock is 100MHz.	00

Table 5-6. RCW Low (Continued)

Bits	Name	Meaning	Normal Mode from Boot EEPROM		Reduced Mode RS[0-2] within '011' to '111	
			Setting	Value	Setting	Value
19	RIOE	RapidIO Enable	Selects 100 MHz reference clock for RapidIO and Ethernet blocks.	RCW[16], RCW[3]	RCW[16],RCW[3] - no SGMII, no 1x protocols	00000
18	1x	RIO 1x Select	Reserved			
17	SGMII1	SGMII1 Enable				
16	SGMII2	SGMI2 Enable				
15–13	MODCK[15:0]	Clock Modes			MODCK[15:13] No reset Slave	00
12					~RCW[2] Select system PLL for PCI	1
11					Select system PLL for DDR.	1
10					Select system PLL for M3.	1
9					Reserved.	0
8					Disable global PLL	1
7–6					Enables core and system PLLs.	00
5–0					MODCK[5:3].	00
					RCW[2:0] MODCK[2:0].	

Table 5-7. RCW High

Bits	Name	Meaning	Normal Mode from Boot EEPROM		Reduced Mode RS[0-2] within 011 to 111	
			Setting	Value	Setting	Value
31 -30	-	Reserved	Reserved	00	Reserved	00
29	EWDT	Watchdog Timer	Disable watchdog timer	0	Disable watchdog timer	0
28	BPRTC	Boot Port Configuration	Boot port configured with no SMII	0	Boot port configured no SMII (PCI)	0
27 -26			RCW[15–14]. Boot port configuration value 1 and 0.	-	RCW[15–14]	000

Table 5-7. RCW High (Continued)

Bits	Name	Meaning	Normal Mode from Boot EEPROM		Reduced Mode RS[0-2] within 011 to 111	
			Setting	Value	Setting	Value
25	BPRT	Boot Port Select	Boot port selected 2.	0	Boot port selected 2	0
24 -23			RCW[13–12]. Boot port select 1–0 (Ethernet/RapidIO/PCI/ATM)	0	RCW[13–12]. Boot port select PCI	10
22	PCI	PCI Host Access	PCI host disabled	0	PCI host disabled	0
21	RIO	RapidIO Host Access	RapidIO host access disabled.	0	RapidIO host access disabled.	0
20 -16	RST_SLV	Reset Slaves	No reset slaves to be configured	00000	No reset slaves to be configured	00000
15	-	Reserved	-	0	Reserved	0
14 -12	PIN_MUX	Pin Multiplexing	Pin multiplexing 4–2	000	Pin multiplexing 4–2	000
11 -10			RCW[11–10]. Pin multiplexing 1–0	-	RCW[11–10]. Pin multiplexing 1–0	-
9 -4	Device ID	Device ID	RCW[9–4]. Device ID	-	RCW[9–4]. Device ID	-
3 -0	-	Reserved	Reserved	000	Reserved	000

5.10 Clock Options

The main clock source is a 66MHz clock oscillator on socket. An external clock can be used instead of the on-board clock. Other clocking options are: external pulse generator (on the SMB RF connector), and a programmable clock oscillator used in SHMOO measurement. The selection between clock sources is done by jumper (JP5). Additional MMCX RF connectors on several MSC8144 pins allow chip characterization.

5.10.1 Clock Distribution

The clock circuits generate the clocks for the cores, the internal CLASS buses, the packet processor, the PCI interface, the TDM, internal memory, the DDR-SDRAM memory controller, and SERDES interface for the RapidIO controller. The clock generation components and clock scheme are shown **Figure 5-10**. The clock circuits are locked, according to the selected clock mode, when the first stage of the system reset configuration is done (reset configuration is controlled by the RESET block).

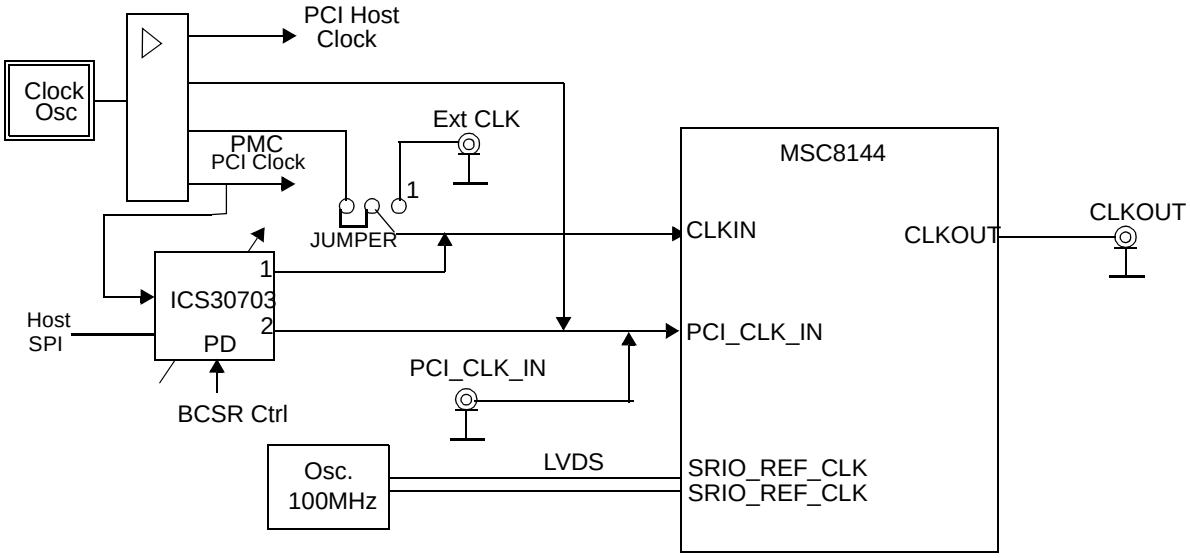


Figure 5-10. MSC8144 Clock Scheme

5.10.2 SHMOO Programmable Clock

The device used for the SHMOO programmable clock is the ICS307-03 by ICS. The ICS307-03 is a dynamic, serially programmable clock source that is flexible and takes up minimal board space. Output frequencies are programmed via the host SPI port. In advanced PLL coupled to an array of configurable output dividers and three outputs allows low-jitter generation of frequencies from 200 Hz to 270 MHz. The device can be reprogrammed during operation, where the output frequency may be determined at run time. The CLK1 output may be connected to the MSC8144 CLKIN pin. The CLK2 output drives variant frequencies to MSC8144 PLL2 (**Figure 5-11**), which is connected to the PCI_CLK_IN input.

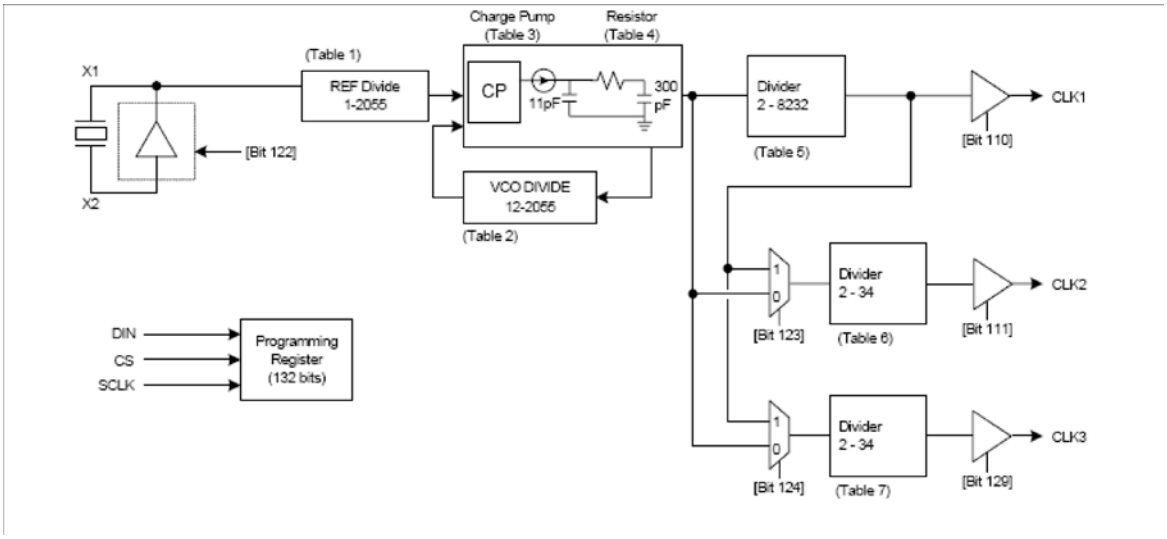


Figure 5-11. Programmable Clock Block Diagram

5.11 JTAG Debug Port Connectivity

The JTAG debug connectivity scheme is shown in **Figure 5-12** The MSC8144 has two options for JTAG: both processors connected in a chain, and both (or one) processors connected independently. If both processors are connected in a chain (set SW2[3] = 0, or BCSR3[5] = 0), only the OnCE 14-pin connector is used. The command chain flows via the MSC8144 to the MPC8560, and both processors are viewed as one entity via CodeWarrior. If the processors are connected separately (set SW2[3] = 1, or BCSR3[5] = 1), then use the OnCE connector for the MSC8144, and the COP 16-pin connector for the MPC8560. This second option allows the user to focus on debugging the MSC8144 only, without the distraction of code from the MPC8560.

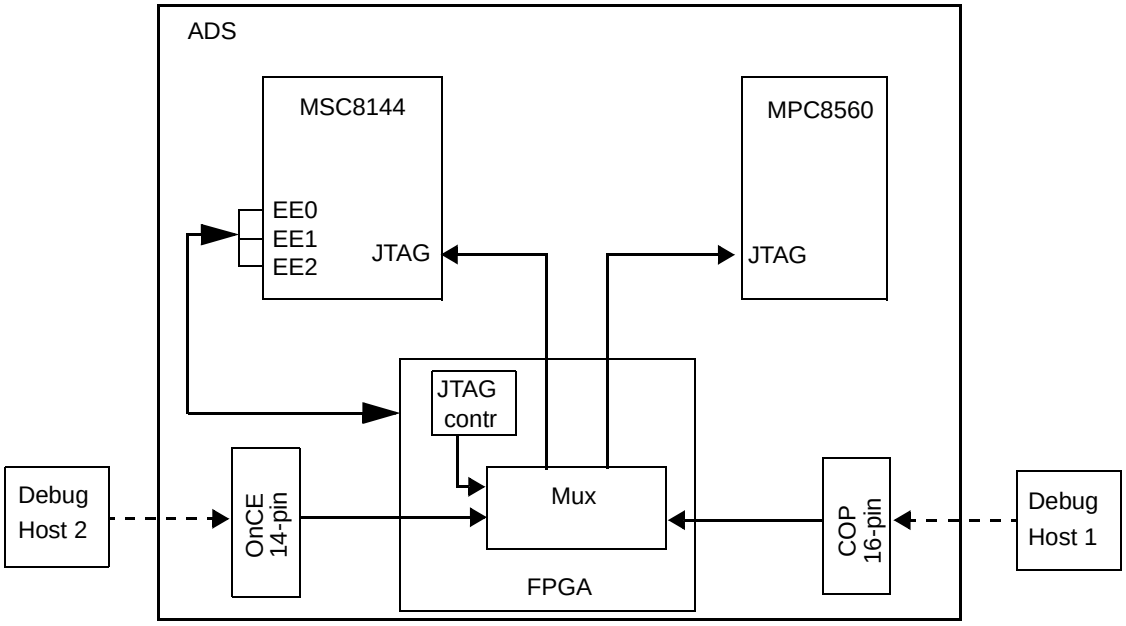


Figure 5-12. JTAG Multiplexing

5.12 Host Processor

The Host processor, the MPC8560, is a member of the PowerQUICC III family of network processors. The MPC8560 integrates two processing blocks—a high-performance embedded e500 core, and a communications processor module (CPM). Below is a list of MPC8560 ports used on the ADS:

- DDR controller in 64-bit Mode at 266MHz;
- LBC bus;
- 64-bit PCI controller configured in 32-bit mode;
- Two integrated TSEC 1Gbps in RGMII mode.
- CPM SPI port in multi-master mode;
- CPM FCC1 Utopia bus;

- CPM FCC2 MII/RMII port;
- Eight CPM MCC TDM ports;
- Two I2C bus controllers: dedicated and CPM based;
- Dedicated UART.

It is possible to configure the ADS so that all peripherals are programmed from MSC8144. If configured this way, the MPC8560 must be set in reset state in order to avoid contention on the parallel control bus (do: SW2[1] = 1).

5.12.1 Host Configuration

After the reset procedure is completed, the host has the following default clock values:

- CPU clock 667 MHz,
- CPM and CCB 266 MHz,
- DDR 133 MHz (266 MHz Data Rate),
- LBC 32 MHz with SYSCLK 66 MHz

Table 5-8 shows reset signals for the Host, their default values, and a description for each signal.

Table 5-8. MPC8560 Reset Configuration Signals

Signal Name	Mode	Value	Implemented
nPCI_REQ64	The PCI interface operates as a 32-bit interface	1	Internal Pull-Up
nPCI_GNT4	PCI Mode. Non PCI-X	1	Internal Pull-Up
nPCI_GNT3	PCI operates in normal mode	1	Pull-Up
nPCI_GNT2	The on-chip PCI arbiter is enabled/disable	1/0	4.7k Pull-Up or Pull-Down
nPCI_GNT1	42Ohm/25Ohm I/O drivers are used on the PCI interface	1/0	4.7k Pull-Up or Pull-Down
EC_MDC	Ethernet interfaces operate in reduced mode RGMII mode	0	4.7k Pull-Down
TSEC1_TXD7, TSEC2_TXD7		0,0	4.7k Pull-Down
TSEC1_TXD[6:4]	Boot ROM is on local bus 16-bit Flash	110	Internal Pull-Up 4.7k Pull-Down
TSEC2_TXD[6:5]	One added buffer delay (default) (zero added buffer delays for LALE)	11	Internal Pull-Up
TSEC2_TXD[2:4]	RapidIO ID	11	Internal Pull-Up
LA[28:31]	cfg_sys_pll[0:3]	0100 CCB/SYSCLK = 4	4.7k Pull-Up/Down
LALE,LGPL2	cfg_pll_core[0:1]	10 Core/CCB = 3	4.7k Pull-Up/Down
LA27	The e500 core is allowed to boot without waiting for configuration by an external master	1	4.7k Pull-Up

Table 5-8. MPC8560 Reset Configuration Signals (Continued)

Signal Name	Mode	Value	Implemented
LWE[0:1]	PCI:Two added buffer delays—required to meet 2-ns hold time requirement	1/0 1/0	4.7k Pull-Up/Down
LWE[2:3]	MPC8560 acts as the host processor/agent mode	11/00	4.7k Pull-Up/Down
LGPL[0:1]	The CCB clock is the source of the RapidIO transmit clock	11	Internal Pull-Up
LGPL3,LGPL5	Boot sequencer is disabled/enable	11/00	According to SW2.2 setting
MSRCID[1:0]	Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL signals	11	Internal Pull-Up

5.12.2 Host Memory Module

Main memory for the Host (MPC8560) is the Micron DDR1 MT8VDDT3264H(I)Y-335 256 Mbyte SODIMM.

5.12.3 Host Local Bus

The Host Local Bus allows multiplexing of addresses with data signals. The devices (configured in asynchronous mode) located on the bus are:

- Flash memory is Intel 16 Mbyte PC28F128P30B85
- DS3 Framer is Exar XRT79L71
- FPGA is Altera MAXII

5.12.3.1 Flash on LBIU

The Intel StrataFlash embedded memory (P30) is used as the boot source for the MPC8560 processor. The space on the Flash memory utilized on the ADS is 16 Mbyte with a bottom boot sector. This can be upgraded to 32/64 Mbyte parts. Access time is 85 ns. Access to the Flash memory is via the local bus GPCM memory controller using a 16-bit port size.

When the board $\overline{\text{PORESET}}$ signal is asserted, a RST signal input is sent to the Flash memory. This signal resets the Flash memory internal automation and inhibits write operations until the signal is deasserted. **Figure 5-13** shows the read timing for the Flash memory. **Figure 5-14** shows the signal connections between the Flash memory and the MPC8560 multiplexed local bus. The interface also supports single/page asynchronous and burst synchronous with 16-bit accesses.

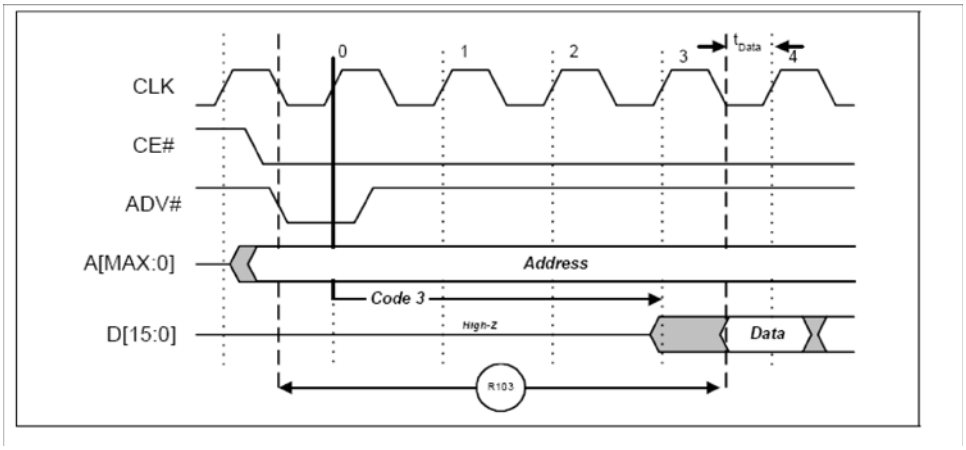


Figure 5-13. Flash Memory Synchronous Read Timing

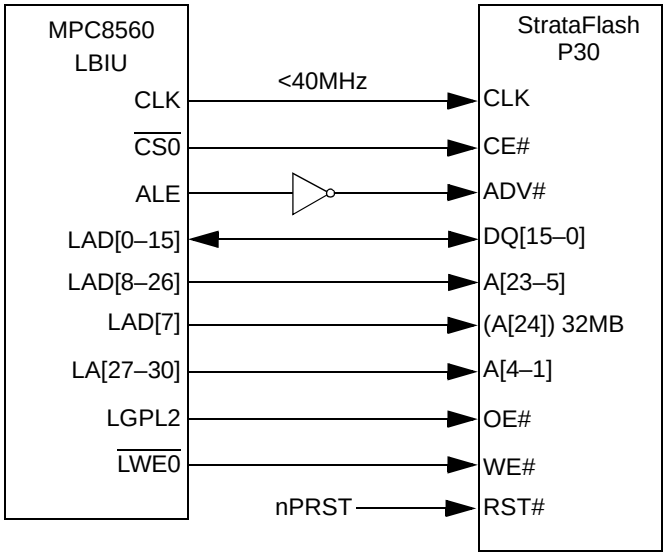


Figure 5-14. Flash memory to Host Signal Connections

5.12.3.2 DS3 Framer on LBIU

The DS3/E3 framer is the Intel XRT79L71. It is located on the CS2 Memory Controller and is set by three PTYPE[0:2] pins. This device requires LBIU GPCM programming. The XRT79L71 resets via the host HRST_REQ output signal or by setting BCSR2[0] = 0. **Figure 5-15** shows the read/write timing for the DS3 framer. **Figure 5-16** shows the signal connections between the DS3 framer and the MPC8560 Multiplexed Local bus.

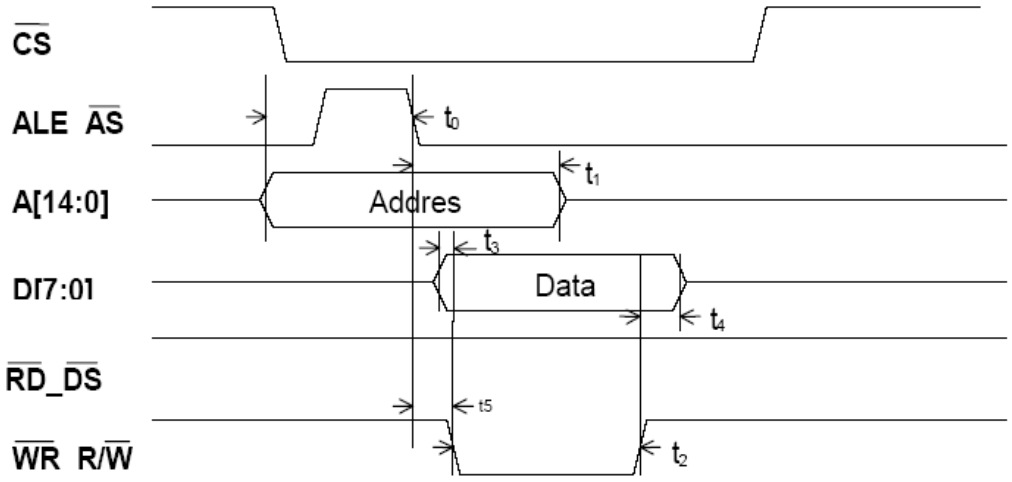


Figure 5-15. DS3 Framer on LBIU Timings

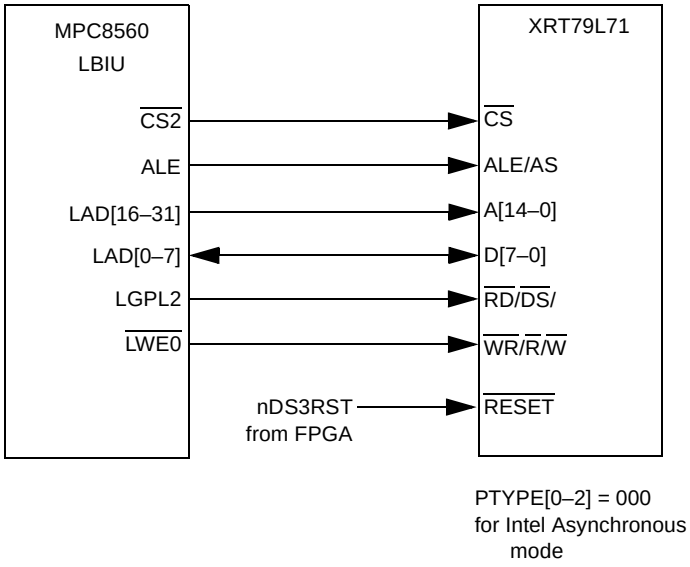


Figure 5-16. DS3 on the LBIU

5.12.3.3 BCSR on FPGA (optional)

The BCSR implemented on the MSC8144 is the Altera EPM1270F256-5. The FPGA resides on LBIU in the CS1 Memory Space. The Register File may achieve 32 8-bit slices. CS1 configures as GPCM. **Figure 5-17** shows the signal connections between the FPGA and the MPC8560 Multiplexed Local bus.

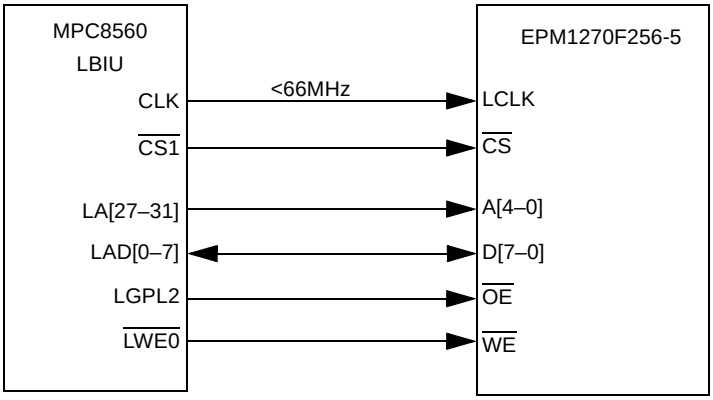


Figure 5-17. FPGA on the LBIU

5.13 Interrupt Assignment

The interrupt assignments between the Host, the MSC8144, and the board peripherals are shown in <Cross Refs>Figure 5-18.

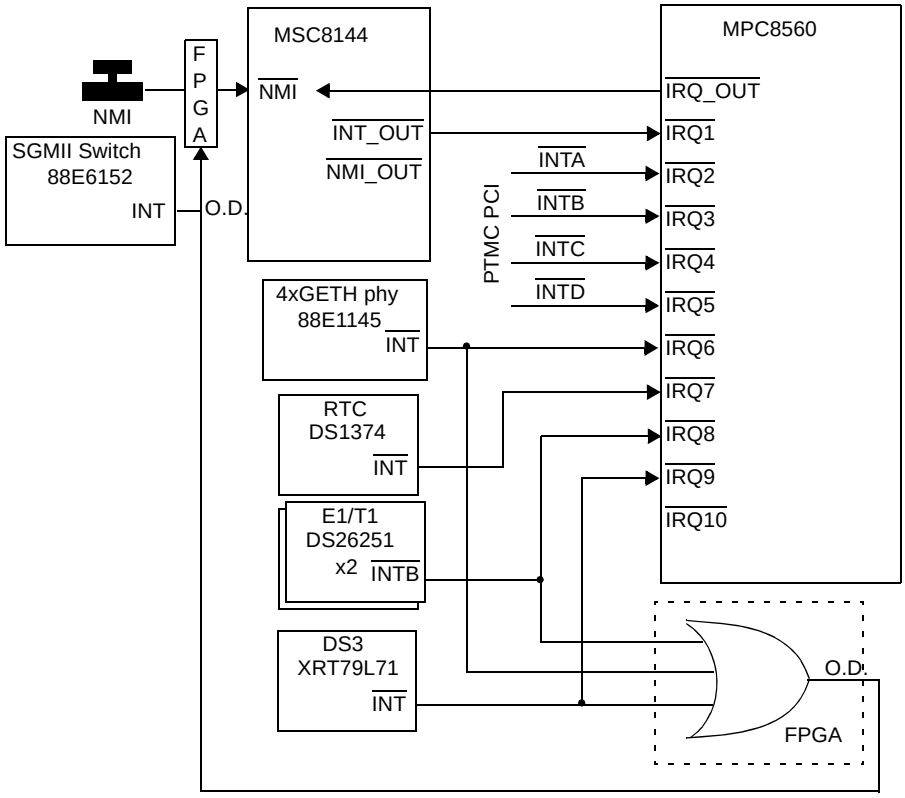


Figure 5-18. ADS Interrupt Scheme

5.14 Board Control and Status Registers (BCSRs)

The BCSR, an 8-bit wide read / write register file, controls or monitors most of the ADS hardware options. The BCSRs may be accessed from the Host Local Bus or via FPGA internal JTAG controller. The BCSR includes up to 16 registers.

BCSR registers are duplicated numerous times within a CS1 region. This is due to the CS region 4 Kbyte minimum block size and the fact that only address lines A[28–31] are decoded for register selection by the BCSR. BCSR is implemented on a FPGA device that provides register and logic functions over some Board signals.

The BCSR controls or monitors the following functions:

- Programmed Power-on-Reset for the board.
- MSC8144 Hardware Reset Configuration signals stored in BCSR registers are available for modification from the Host Local Bus or JTAG.
- Hard- Soft- Reset and $\overline{\text{NMI}}$ ($\overline{\text{IRQ0}}$) push buttons debounce function for the MSC8144.
- Hardware Configuration for the GETH transceiver: SGMII-to-Copper or RGMII-to-Copper setting.
- Enable/Disable to:
  - SPI CS decoding.
  - RS232 Transceiver.
  - SHMOO function.
  - LED off.
- BCSR provides h/w write protection for FLASH and Host I2C EEPROM.
- Logic to prevent signals contention.
- Two LEDs (LD3, LD4) provide software and board reset state signaling.
- Status registers BCSR10, BCSR11 and BCSR16-20 include:
  - ADS Setting
  - BCSR Revision code
  - Firmware date
    - Internal JTAG controller.
    - Programmable JTAG multiplexing
    - TDM reference clock/sync generation.
    - Identification and Control signals to PTMC expansion Card
    - FA functions control.

Sections of the BCSR slice control registers generally have low active notations. This means that a bit function will be enabled while the bit is zero. When a bit is set to high (or 1) a related function is disabled. The most significant bit is bit 0.

All BCSR registers (up to 32) are 8-bit joined in two groups: control registers with read/write access and only read status registers. Control registers obtain their default value during Power-on-Reset. The CNFLOCK bit in BCSR7[7] enables saving of settings values until the ADS powers down.

5.14.1 BCSR0 Board Control Register 0

The BCSR0 serves as a 8-bit control register on the board The BCSR0 may be read or written at any time. BCSR0 defaults are attributed at the time of Power-On-Reset. BCSR0 fields are described below in **Table 5-9**:

Table 5-9. BCSR0 Peripheral's Control 1 (Offset 0)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	CODECEN	***CODEC Enable.*** The CODEC is functional when the CODECEN is asserted (**low**), otherwise when **high** the CODEC enters in power-down mode.	0	R,W
1	E1T1TDM1EN	***E1T1 Framer 1 Enable.*** Upon activation **(low),** the E1T1 Framer 1 is enabled. When negated (**high**), the Framers enters standby mode and isolates electrically from TDM bus.	0	R,W
2	E1T1TDM2EN	***E1T1 Framer 2 Enable.*** Upon activation **(low),** the E1T1 Framer 2 is enabled. When negated (**high**), the Framers enters standby mode and isolates electrically from TDM bus.	0	R,W
3	RS232EN	MSC8144 ***UART Port Transceiver Enable***. Upon activation **(low),** the RS232 Transceiver, using the UART port of the MSC8144, is enabled. When negated (**high**), the RS232 Transceiver enters standby mode.	0	R,W
4	BOOTWP	***BOOT I2C EEPROM Protect***. When asserted (**low**) Host BOOT EEPROM write operations are disabled, when negated (**high**) the EEPROM functions normally,.	0	R,W
5	FLWP	***Flash Protect.*** Upon activation **(low)** the Flash is write-protected. When **high** the Flash functions normally.	0	R,W
6	SIGNAL0	***Signal LED 0***. A dedicated **Green** LED is illuminated when SIGNAL0 is **low** or when MSC8144 GPIO[0:3] = 4'b0101 code is present. The LED is unlit when in its inactive (default) state **(high)**. During the MSC8144 Reset Configuration sequence the LED indicates the SRESET assertion. The user may utilize the LED for s/w Slave signalling purposes.	1	R,W
7	SIGNAL1	***Signal LED 1***. A dedicated **Red** LED is illuminated when SIGNAL1 is **low** or when MSC8144 GPIO[0:3] = 4'b1010 code is present. The LED is unlit when in its inactive (default) state **(high)**. During the Reset Configuration sequence the LED indicates the HRESET assertion.	1	R,W

5.14.2 BCSR1 Board Control Register 1

On the board, the BCSR1 acts as a control register. The BCSR1, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR1 fields are described below in **Table 5-10**:

Table 5-10. BCSR1 Peripheral Control 2 (Offset 1)

BIT	MNEMONIC	Function	DEF	ATT.
0	TDMTSTEN	***TDM Test Clock Buffer Enable***. TDM Clock/Sync generated by internal counter will apply to MSC8144 TDM port when this bit is **low**. When this bit is **high,** it will disable the clock buffer. Other TDM on-board clock sources (CODEC, E1T1 Framers, DS3) are still available.	1	R,W
1	TDMSHREN	***TDM Test Clock in Shared Mode***. TDM Clock/Sync generated by internal counter will apply to MSC8144 TDM port 0 in shared mode when this bit is **low**. When this bit is **high,** it will disable the clock buffer. CODEC will provide clocks to TDM port 0.	1	R,W
2	RGMII1EN	***GE1 Bus Switch Select RGMII.*** When **low** GE1 port signals are tied to RGMII peripherals. If **high** low speed I/F such PCI/UTP are selected.	0	R,W
3	RGMII2EN	***GE2 Bus Switch Select RGMII.*** When **low** GE2 port signals are tied to RGMII peripherals. If **high** low speed I/F such PCI/UTP are selected.	0	R,W
4	GE1EN	***GE1 Port Bus Switch Disable.*** When **low** GE1 port functions in normal mode. If **high** the reference clock 125MHz is disabled.	0	R,W
5	UTPHEN	***Host Utopia Mode.*** When **low** Host Utopia port is selected. If **high** a buffer isolates CPM Utopia signals to available I^2C2 port over Utopia signals.	1	R,W
6	SorRGMII	***GETH Phy Mode Select.*** This bit provides the configuration sequence to GETH phy Port 3. **Low** configures the Phy to SGMII-to-Cooper Mode, **high** - sets it in RGMII-to-Copper Mode.	1	R,W
7	BOOTSQEN	***Host Boot Sequencer Enable***. **Low** enables boot from Serial EEPROM during reset, when **high** Boot Sequencer is disabled - no boot configuration initializes code.	SW2.2	R,W

5.14.3 BCSR2 Board Control Register 2

On the board, the BCSR2 acts as a control reset register. The BCSR2, which may be read or written at any time, receives its defaults upon Power-On-Reset. All reset signals mentioned

below activated also when main Hard Reset is asserted. The BCSR2 fields are described below in ***Table 5-11***:

Table 5-11. BCSR2 Peripheral's Reset (Offset 2)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	DS3_RST	***Reset to DS3 Framer.*** **Low** provides reset to DS3 Framer. Normal operation is available when **high**.	0	R,W
1	SGMII_RST	***Reset to SGMII Switch.*** **Low** provides reset to SGMII Switch. Normal operation is available when **high**.	1	R,W
2	RGMII_RST	***Reset to RGMII Switch.*** **Low** provides reset to RGMII Switch. Normal operation is available when **high**.	1	R,W
3	PHY_RST	***Reset to GETH Phy.*** **Low** provides reset to GETH Phy. Normal operation is available when **high**.	1	R,W
4	E1T1RST1	***Reset to E1T1 Framer 1.*** **Low** provides reset to E1T1 Framer 1. Normal operation is available when **high**.	1	R,W
5	E1T1RST2	***Reset to E1T1 Framer 2.*** **Low** provides reset to E1T1 Framer 2. Normal operation is available when **high**.	1	R,W
6	CODEC_RST	***Reset to CODEC.*** **Low** provides reset to CODEC. Normal operation is available when **high**.	1	R,W
7	RST	***Reset Signal.*** Writing **low** asserts reset to an expansion PTMC card. If the bit is set to **high** the reset signal is negated. This bit also indicates MSC8144 reset status. The bit remains low until the MSC8144 configuration sequence is completed.	1, HRST level when read	R,W

5.14.4 BCSR3 Board Control Register 3

On the board, the BCSR3 acts as a control register. The BCSR3, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR3 fields are described below in **Table 5-12**:

Table 5-12. BCSR3 Special Function 1 (Offset 3)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0	PRST	***Power-on-Reset.*** Writing **low** will generate PORESET pulse for MSC8144ADS to re-configure it except the M3 Reset.	'1' after reset	R,W
1	M3PRST	***M3 Power-on-Reset.*** Writing **low** will generate RESET pulse for the MSC8144 M3 Memory and main PORESET for the whole board..	'1' after reset	R,W
2	DEBUG	***Debug Request.*** A **low** value for this bit causes the MSC8144 to enter debug mode by driving "1" to EE0 input. When this bit is **high** the chip starts running after reset negation.	SW2.4	R,W
3	SHMOOEN	***Clock Synthesizer Enable.*** **Low** enables clock synthesizer for SCHMOO purpose. When **high** the synthesizer enters in power-down mode.	1	R,W

Table 5-12. BCSR3 Special Function 1 (Offset 3) (Continued)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
4	AMCCLK	***AMC Clock Select.*** A **low** value for this bit means that when the ADS works as an AMC card the CLOCK1 coming from the ATCA carrier will be directed to the MSC8144 TIMER0 input. When **high**, CLOCK2 is selected.	0	R,W
5	JTAGCHN	***JTAG Chain Select.*** **High** means 'Single' chip JTAG configuration. When **Low** 'Chain' JTAG configuration is selected.	SW2.3	R
6	PTMCCTRL1	***PTMC Control 1.*** PTMC User defined control1 signal. The signal reflects bit value.	1	R,W
7	PTMCCTRL2	***PTMC Control 2.*** PTMC User defined control2 signal. The signal reflects bit value.	1	R,W

5.14.5 BCSR4 Board Control Register 4

On the board, the BCSR4 acts as a control register. The BCSR4, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR4 fields are described below in **Table 5-13**:

Table 5-13. BCSR4 Description MSC8144 Special Function 2 (Offset 4)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-2	TDMDIV	***TDM Clock Divider.*** Three bits set TDM clock divider. See coding **Table 5-14** below.	'000'	R,W
3	TDMx4	***TDM Mux Enable.*** **Low** sets TDM mux to narrow port mode. **High** provides selection for full eight TDM ports wide. The bit is not relevant for external pins configuration mode.	1	R,W
4	GETHEN	***GETH Enable.*** **Low** enables GETH bus switches. When **high** GETH bus switches are disabled.	0	R,W
5	IND	***Indication.*** **Low** illuminates the appropriate LED "IND". When **high**, the LED is dark	1	R,W
6-7	RSRV4	Reserved	'11'	R,W

Table 5-14. TDM Clock Divider

TDMDIV[0–2]	Frequency
1	16 MHz
2	8 MHz
3	4 MHz
4	2 MHz
0,5–7	Disabled

5.14.6 BCSR5 Board Control Register 5

On the board, the BCSR5 acts as a MSC8144 configuration register. The BCSR5, which may be read or written at any time, receives its defaults upon Power-On-Reset. The value of the bits is set according to indicated DIP-Switch. ON position provides 0 value, OFF - 1.The BCSR5 fields are described below in **Table 5-15**:

Table 5-15. BCSR5 Description MSC8144 Configuration 1 (Offset 5)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-2	CFG_RS	***Reset Configuration Source.*** MSC8144 Configuration pins[a].	SW4.1-4.3	R,W
3-7	RC0-RC4	***External Configuration Bits 0 to 4.*** MSC8144 Configuration pins.	SW4.4-4.8	R,W

5.14.7 BCSR6 Board Control Register 6

On the board, the BCSR6 acts as a control register. The BCSR6, which may be read or written at any time, receives its defaults upon Power-On-Reset. The value of the bits is set according to indicated DIP-Switch. ON position provides 0 value, OFF - 1.The BCSR6 fields are described below in **Table** .

Table 5-16. BCSR6 - MSC8144 Configuration 2 (Offset 6)

BIT	MNEMONIC	Function	DEF on PRST	ATT
0-7	RC5-RC12	***External Configuration Bits 5 to 12.*** MSC8144 Configuration pins.	SW1.1-1.8	R,W

5.14.8 BCSR7 Board Control Register 7

On the board, the BCSR7 acts as a MSC8144 configuration and control register. The BCSR7, which may be read or written at any time, receives its defaults upon Power-On-Reset. The value of the bits is set according to indicated DIP-Switch. ON position provides 0 value, OFF - 1. The BCSR7 fields are described below in **Table 5-17**.

Table 5-17. BCSR7 Configuration 3 & Special Function 3 (Offset 7)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-3	RC13-RC16	***Enable Chip Test Mode.*** MSC8144 Configuration pins[a].	SW3.1-3.4	R,W
4	CLKRNG	***Clock-in Range***. MSC8144 Configuration pin[a].	SW3.5	R,W
25	PHYStoR	***SGMII Phy Mode.*** **Low** configures the GETH Phy in SGMII Mode. **High** sets the phy in RGMII Mode.	0	R,W

Table 5-17. BCSR7 Configuration 3 & Special Function 3 (Offset 7) (Continued)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
6	PTEN	***PTMC Buffers Enable.*** Used to control the PTMC card buffer enable logic in order to prevent undesired signal contention on the ADS. **Low** enables buffers. **High** isolates PTMC card output driver from the base board.	'1'	R,W
7	CNFLOCK	***Configuration Lock.*** Allows locking of the values of control registers until power down. The bit is activated when **low. High** is a default mode when configuration bits are rewritten from the DIP-switches.	1	R,W

a. Defined in the <Tcross-ref>MSC8144 Reference Manual

5.14.9 BCSR8 Board Miscellaneous Register 1

On the board, the BCSR8 acts as a reserved control register. The BCSR8, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR8 fields are described below in **Table 5-18**.

Table 5-18. BCSR8 Reserved Function (Offset 8)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-2	SPARE[1:3]	***User Defined*** Control Bits 1-3. Reflects appropriate DIP-Switch setting.	SW2.6-2.8	R,W
3-7	RSRV8	Reserved	'11111'	R,W

5.14.10 BCSR9 Board Control Miscellaneous Register 2

On the board, the BCSR9 acts as a control register for FA mode. The BCSR9, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR9 fields are described below in **Table 5-19**.

Table 5-19. BCSR9 FA Functions (Offset 9)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-1	FA_MODE	***FA Mode.*** Two bits define different FA module operation modes. They are affected when the FA Module is activated. Default mode - FA module is disabled	0	R,W
2-3	FA_M3_MODE	***FA_M3 Mode.*** Two bits define the different FA_M3 module operation modes. They are affected when the FA_M3 Module is activated. Default mode - FA_M3 module is disabled.	0	R,W
4	FA_MODE_ACT	***FA Module Activation.*** **High** with PORESET places FA Module in operation mode.	0	R,W
5	FA_M3_ACT	***FA_M3 Module Activation.*** **High** with PORESET places FA_M3 Module in operation mode.	0	R,W

Table 5-19. BCSR9 FA Functions (Offset 9) (Continued) (Continued)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
6	WAKEUP	***VSTABLE control***. **Low** enables generating a trigger in the MSC8144. If **high** this function is disabled.	1	R,W
7	LEDEN	***LEDs Enable.*** Used for FA. When **low**, the LEDs are lit. When **high** the LEDs are off.	0	R,W

5.14.11 BCSR10 Board Status Register 1

The BCSR10 Register is a status register (read only). The BCSR10 fields are described below in **Table 5-20**.

Table 5-20. BCSR10 Firmware Revision (Offset 0xA)

BIT	MNEMONIC	Function	Read At
0-3	REV	***BCSR Revision***. Four bits revision coding	Programmed value
4-7	SubREV	***BCSR Sub Revision.*** Four additional bits revision coding	Programmed value

5.14.12 BCSR11 Board Status Register 2

The BCSR11 Register is a status register (read only). The BCSR11 fields are described below in **Table 5-21**.

Table 5-21. BCSR11 Description (Offset 0xB)

BIT	MNEMONIC	Function	Read At
0-1	PTMC_type	***PTMC Type.*** Defines type of inserted PTMC card. See **Table** below.	Read coding from PTMC Card
2-5	EE2	***EE2 Four Pins.*** MSC8144 Event signals.	8144 EE2 Pins
6	RCW_LOAD_FAIL	***Reset Configuration Load Fail.*** When **high**, indicates that the RCW loading from an I^2C EEPROM failed due to an error. **Low** indicates normal operation	0
7	-	Not Implemented.	1

Table 5-22. PTMC Card Type Assignment

PTMC_type[0:1]	Description
'00'	-
'01'	PCI protocol is supported
'10'	Incapable PCI protocol
'11'	Disconnected

5.14.13 BCSR12 Board Status Register 3

The BCSR12 Register is a status register (read only). The BCSR12 fields are described below in **Table 5-23**.

Table 5-23. BCSR12 Description (Offset 0xC)

BIT	MNEMONIC	Function	Read At
0-2	GA	***AMC Geographical Address.*** Three bits define AMC Card geographical address depend on slot in ATCA carrier board.	AMC connector
3	AMCEN	***AMC Mode Enable***. Low is meant the ADS functions as AMC card	8144 EE2 Pins
4-7	-	Not Implemented.	'1111'

5.14.14 BCSR13 FA Data Register

On the board, the BCSR13 acts as a data register for FA mode. The BCSR13, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR13 fields are described below in **Table 5-24**.

Table 5-24. BCSR13 - FA Data Register (Offset 0xD)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-7	FA_DATA	***FA Data.*** Data register used for FA operations.	0	R,W

5.14.15 BCSR14 FA_M3 Data Register

On the board, the BCSR14 acts as a data register for FA_M3 mode. The BCSR14, which may be read or written at any time, receives its defaults upon Power-On-Reset. The BCSR14 fields are described below in **Table 5-25**.

Table 5-25. BCSR14 - FA_M3 Data Register (Offset 0xE)

BIT	MNEMONIC	Function	DEF on PRST	ATT.
0-7	FA_M3_DATA	***FA_M3 Data.*** Data register for FA_M3 operations.	0	R,W

5.14.16 BCSR15 Reserved

5.14.17 BCSR16 Board Status Register 4

The BCSR16 Register is a status register (read only). The BCSR16 fields are described below in **Table 5-26**.

Table 5-26. BCSR16 Time Stamp 1 (Offset 0x10)

BIT	MNEMONIC	Function	Read At
0-7	TIMED	Firmware Creation Day.	Programmed

5.14.18 BCSR17 Board Status Register 5

The BCSR17 Register is a status register (read only). The BCSR17 fields are described below in **Table 5-27**.

Table 5-27. BCSR17 Time Stamp 2 (Offset 0x11)

BIT	MNEMONIC	Function	Read At
0-7	TIMEM	Firmware Creation Month.	Programmed

5.14.19 BCSR18 Board Status Register 6

The BCSR18 Register is a status register (read only). The BCSR18 fields are described below in **Table 5-28**.

Table 5-28. BCSR18 Time Stamp 3 (Offset 0x12)

BIT	MNEMONIC	Function	Read At
0-7	TIMEY	Firmware Creation Year.	Programmed

5.14.20 BCSR19 Board Status Register 7

The BCSR19 Register is a status register (read only). The BCSR19 fields are described below in **Table 5-29**.

Table 5-29. BCSR19 Time Stamp 4 (Offset 0x13)

BIT	MNEMONIC	Function	Read At
0-7	TIMEH	Firmware Creation Hour.	Programmed

5.14.21 BCSR20 Board Status Register 8

The BCSR20 Register is a status register (read only) The BCSR20 fields are described below in **Table 5-30**.

Table 5-30. BCSR20 Time Stamp 5 (Offset 0x14)

BIT	MNEMONIC	Function	Read At
0–7	TIMEm	Firmware Creation Minute.	Programmed

5.15 Power Supply System

5.15.1 Primary Power Supply

There are two possible sources of power, depending on the working mode:

- Standalone Mode external 12 VDC @ 3 A Power Supply with On/Off power switch.
- AMC Mode 12 V from ATCA carrier board

The External 12V Power Supply is a standard power supply. Its parameters are:

- Vin = 100 V– 240 V AC @ 50–60 Hz
  Vout = 12 VDC±5% @ 3 A

5.15.2 Power Supply Operation

The secondary power system is built on the MAXYZ family of power supplies, produced by Power-One. The power supply includes the ZM7108 Power Manager-DPM and several POL converters for each power rail.

The ZM7108 is a fully programmable digital power manager that utilizes the industry-standard I2C communication bus interface to control, manage, program and monitor up to 8 Z-series POL converters. The ZM7108 completely eliminates the need for external components for power management and POL converters programming, monitoring, and reporting. Parameters of the ZM7108 are programmable via the I^2C bus and can be changed by a user at any time during product development and service. **Table 5-31** shows the power distribution on the MSC8144ADS, for the MPC8560, and for the MSC8144.

Table 5-31. Power Distribution

Proc.	Circuit	Voltage @Current	Adjustment	Supply	Primary supply	Comment
MSC8144	Internal Logic Power and Cores: VDDC0,VDDC1, VDDC2,VDDC3, VDD,VDDPLL	1.0 V @ 10 A	0.6 V—2.0 V	POL1 ZY7115(15A) or ZY7120(20A)	12 V	SHMOO capability, Option to disconnect any core power rail. VDDPLL has dedicated LPF
	M3 Internal Logic: VDDM3	1.2 V @ 1 A	Fixed	LDO1 MIC49300(3 A)	POL3 3.3 V	—
	M3 I/O Power: VDDM3IO	2.5 V @ 0.2 A	Fixed	LDO2 MIC49150(1.5 A)	POL3 3.3 V	—
	M3 Charge Pump: M3V25	2.5V @ 0.2A	Fixed	LDO8 MIC49150(1.5 A)	POL3 3.3 V	—
	IO Supply: VDDIO	3.3V				
	GEthernet 1&2 I/O: VDDGE	2.6 V/3.3 V@ 0.5 A	Fixed	No dedicated	LDO2/POL3	Select with jumper
	DDR2/DDR1: VDDDR	1.8 V/2.6 V @ 6 A	Fixed	POL2 ZY7007(7A)	12V	—
	DDR2/DDR1 on SODIMM: VTT, VREF	VDDDR/2 0.9V/1.23 V	Fixed	TPS51116	12 V and LDO7	—
	Serial RapidIO Core Power: VDDSXC, VDDRIOPLL	1.0 V @ 1.5 A	Fixed	LDO3 MIC49150(1.5A)	POL3 3.3 V	VDDRIOPLL has dedicated LPF
	Serial RapidIO IO Power: VDDSXP	1.0 V @ 1.5 A	Fixed	LDO9 MIC49150(1.5 A)	POL3 3.3 V	
MPC8560	Internal Logic Power and Cores: VDDH	1.2 V @10 A	—	POL4 ZY7115(15 A)	12 V	VDDHPLL has dedicated LPF
	GEthernet 1&2 I/O: VDDGE	2.5V @ 0.5A	Fixed	LDO4	POL3 3.3 V	—
	DDR1 on SODIMM: VDDDRH	2.5 V @ 3 A	Fixed	LDO5 LT1764EQ_2.5		—
	DDR1 on SODIMM: VTT, VREF	VDDDRH/2 1.25 V	Fixed	LDO6 FAN1655MTF		—

Table 5-31. Power Distribution (Continued)

Proc.	Circuit	Voltage @Current	Adjustment	Supply	Primary supply	Comment
ADS Common	General	5V @ 3.0A	Fixed	Dedicated POL4 ZY7007(7 A)	12 V	Most current is over PMC expansion board
	8144 GPIO,TDM, PCI, 8560 I/O, LBIU phr etc. FPGA core power: VDDIO	3.3 V @ 3 A	2.5–4.0 V programmed	Dedicated POL3 ZY7007(7 A)	12 V	—
	GETH1,2 phy internal	1.0 V @ 1 A	—	LDO7 MIC49150(1.5 A)	POL3 3.3 V	—

5.16 Interconnection Details

Table 5-32 below shows the interconnection signal details between the MPC8560 and the MSC8144, for each port (PCI, UTP, TDM, and MII).

Table 5-32. MSC8144 to MPC8560 Ports Interconnection

Port	MSC8144 Signal	MPC8560 Signal	Comment
PCI			
	PCI_AD[31:0]	PCI_AD[31:0]	PCI-32bit mode
	PCI_C/BE[3:0]	PCI_C/BE[3:0]	
	PCI_PAR	PCI_PAR	
	PCI_FRAME	PCI_FRAME	
	PCI_TRDY	PCI_TRDY	
	PCI_IRDY	PCI_IRDY	
	PCI_STOP	PCI_STOP	
	PCI_DEVSEL	PCI_DEVSEL	
	—	PCI_IDSEL	Pull-up acts always as host
	$\overline{\text{PCI\_PERR}}$,$\overline{\text{PCI\_SERR}}$	$\overline{\text{PCI\_PERR}}$,$\overline{\text{PCI\_SERR}}$	MSC8144 pin mux Mode3 doesn't support Errors reporting
	$\overline{\text{PCI\_REQ\_B}}$,$\overline{\text{PCI\_GNT\_B}}$	$\overline{\text{PCI\_REQ0}}$,$\overline{\text{PCI\_GNT0}}$	
	—	$\overline{\text{PCI\_REQ1}}$,$\overline{\text{PCI\_GNT1}}$	To PTMC
	INT_OUT	IRQ1	Interrupt like INTA#
	PCI_CLK_IN	PCI_CLK_IN	Clock Distributor, or Clock synthesizer for MSC8144
UTP2-8/16[a]			
	RxADDR0	PC15(TxAddr[0])	
	RxADDR1	PC13(TxAddr[1])	

Table 5-32. MSC8144 to MPC8560 Ports Interconnection (Continued)

Port	MSC8144 Signal	MPC8560 Signal	Comment
	RxADDR2	PC7(TxAddr[2])	
	RxADDR3	PD7(TxAddr[3])	
	—	PD19(TxAddr[4])	SPI_SEL
	RxDATA0	PC8(TxD[0])	UTP-16
	RxDATA1	PC9(TxD[1])	
	RxDATA2	PC10(TxD[2])	
	RxDATA3	PD21(TxD[3])	
	RxDATA4	PD6(TxD[4])	
	RxDATA5	PD22(TxD[5])	
	RxDATA6	PD25(TxD[6])	
	RxDATA7	PD28(TxD[7])	
	RxDATA8	PA25(TxD[8])	UTP-8/16
	RxDATA9	PA24(TxD[9])	
	RxDATA10	PA23(TxD[10])	
	RxDATA11	PA22(TxD[11])	
	RxDATA12	PC21(TxD[12])	
	RxDATA13	PC20(TxD[13])	
	RxDATA14	PA19(TxD[14])	
	RxDATA15	PA18(TxD[15])	
	RxSOC	PA29(TxSOC)	
	RxPRTY	PD16(TxPrty)	SPI_MISO
	RxENB	PA31(TxEnb)	
	RxCLAV	PA30(TxClav)	
	RCLK	PC20(CLK12-TxCLK)	Driven from PTMC exp. card
	TxADDR0	PC14(RxAddr[0])	
	TxADDR1	PC12(RxAddr[1])	
	TxADDR2	PC6(RxAddr[2])	
	TxADDR3	PD29(RxAddr[3])	
	—	PD18(RxAddr[4])	SPI_SLK

Table 5-32. MSC8144 to MPC8560 Ports Interconnection (Continued)

Port	MSC8144 Signal	MPC8560 Signal	Comment
	TxDATA0	PD14(RxD[0])	UTP-8/16
	TxDATA1	PD15(RxD[1])	
	TxDATA2	PD20(RxD[2])	
	TxDATA3	PD21(RxD[3])	
	TxDATA4	PD23(RxD[4])	
	TxDATA5	PD24(RxD[5])	
	TxDATA6	PD26(RxD[6])	
	TxDATA7	PD27(RxD[7])	
	TxDATA8	PA10(RxD[8])	UTP-16
	TxDATA9	PA11(RxD[9])	
	TxDATA10	PA12(RxD[10])	
	TxDATA11	PA13(RxD[11])	
	TxDATA12	PA14(RxD[12])	
	TxDATA13	PA15(RxD[13])	
	TxDATA14	PA16(RxD[14])	
	TxDATA15	PA17(RxD[15])	
	TxSOC	PA27(RxSOC)	
	TxPRTY	PD17(RxPrty)	SPI_MOSI
	TxENB	PA28(RxEnb)	
	TxCLAV	PA26(RxClav)	
	TCLK	PC21(CLK11-RxCLK)	Driven from the host or PTMC exp. card
TDM[b]			
	Fxdata0[c](TDM0RDAT)	PA8(A1L1RXD)	
	TDM0RCLK	PC31(CLK1-TDMA1RXCLK)	
	TDM0RSYN	PA6(A1L1RSYNC)	
	Fxdata3(TDM0TDAT)	PA9(A1L1TXD)	
	TDM0TCLK	PC30(CLK2-TDMA1TXCLK)	
	TDM0TSYN	PA7(A1L1TSYNC)	
	Fxdata4[c](TDM1RDAT)	PD12(B1L1RXD)	
	TDM1RCLK	PC29(CLK3-TDMB1RXCLK)	
	TDM1RSYN	PD10(B1L1RSYNC)	
	Fxdata7(TDM1TDAT)	PD13(B1L1TXD)	
	TDM1TCLK	PC28(CLK4-TDMB1TXCLK)	
	TDM1TSYN	PD11(B1L1TSYNC)	
	Fxdata8[c](TDM2RDAT)	PB14(C1L1RXD)	
	TDM2RCLK	PC27(CLK5-TDMC1RXCLK)	

Table 5-32. MSC8144 to MPC8560 Ports Interconnection (Continued)

Port	MSC8144 Signal	MPC8560 Signal	Comment
	TDM2RSYN	PB12(C1L1RSYNC)	
	Fxdata11(TDM2TDAT)	PB15(C1L1TXD)	
	TDM2TCLK	PC26(CLK6-TDMC1TXCLK)	
	TDM2TSYN	PB13(C1L1TSYNC)	
	Fxdata12[c](TDM3RDAT)	PB10(D1L1RXD)	
	TDM3RCLK	PC25(CLK7-TDMD1RXCLK)	
	TDM3RSYN	PB8(D1L1RSYNC)	
	Fxdata15(TDM3TDAT)	PB11(D1L1TXD)	
	TDM3TCLK	PC24(CLK8-TDMD1TXCLK)	
	TDM3TSYN	PB9(D1L1TSYNC)	
	Fxdata16[c](TDM4RDAT)	PB7(A2L1TXD)	
	TDM4RCLK	PC18(CLK14-TDMA2TXCLK)	
	TDM4RSYN	PB5(A2L1TSYNC)	
	Fxdata19(TDM4TDAT)	PB6(A2L1RXD)	
	TDM4TCLK	PC19(CLK13-TDMA2RXCLK)	
	TDM4TSYN	PB4(A2L1RSYNC)	
	Fxdata20[c](TDM5RDAT)	PB31(B2L1TXD)	
	TDM5RCLK	PC16(CLK16-TDMB2TXCLK)	
	TDM5RSYN	PB25(B2L1TSYNC)	
	Fxdata23(TDM5TDAT)	PB30(B2L1RXD)	
	TDM5TCLK	PC21(CLK15-TDMB2RXCLK)	
	TDM5TSYN	PB29(B2L1RSYNC)	
	Fxdata24[c](TDM6RDAT)	PB27(C2L1TXD)	
	TDM6RCLK	PB16(CLK18 -TDMC2TXCLK)	
	TDM6RSYN	PB25(C2L1TSYNC)	
	Fxdata27(TDM6TDAT)	PB26(C2L1RXD)	
	TDM6TCLK	PB17(CLK17-TDMC2RXCLK)	
	TDM6TSYN	PB24(C2L1RSYNC)	
	Fxdata28[c](TDM7RDAT)	PB23(D2L1TXD)	
	TDM7RCLK	PA2(CLK20 -TDMD2TXCLK)	
	TDM7RSYN	PB21(D2L1TSYNC)	
	Fxdata31(TDM7TDAT)	PB22(D2L1RXD)	
	TDM7TCLK	PA3(CLK19 -TDMD2RXCLK)	
	TDM7TSYN	PB20(D2L1RSYNC)	

Table 5-32. MSC8144 to MPC8560 Ports Interconnection (Continued)

Port	MSC8144 Signal	MPC8560 Signal	Comment
MII[d] MAC-to-MAC			
	GE1_RD0	PB22(TXD0)	Shared with TDM-D2(8560)
	GE1_RD1	PB23(TXD1)	
	GE1_RD2	PB24(TXD2)	Shared with TDM-C2(8560)
	GE1_RD3	PB25(TXD3)	
	GE1_RXCLK	CLK13(TxCLK)	25MHz shared for TDM4 RXCLK Clocked from an external clock source via PTMC I/F
	GE1_RX_DV	PB29(TX_EN)	Shared with TDM-B2(8560)
	GE1_RX_ER	PB31(TX_ER)	
	GE1_TD0	PB21(RXD0)	Shared with TDM-D2(8560)
	GE1_TD1	PB20(RXD1)	
	GE1_TD2	PB19(RXD2)	Shared with TDM-A2(8560)
	GE1_TD3	PB18(RXD3)	
	GE1_TXCLK	CLK14(RxCLK)	25MHz shared for TDM4 TXCLK Clocked from an external clock source via PTMC I/F
	GE1_TX_ER	PB28(RX_ER)	Shared with TDM-B2(8560)
	GE1_TX_EN	PB30(RX_DV)	
	GE1_COL	—	Tied to ground for MAC-MAC Mode. Presented on PTMC for MAC-phy test
	GE1_CRS	—	
	—	PB27(MII_COL)	Tied to ground for MAC-MAC Mode.
	—	PB26(MII_CRS)	

a. UTP signals are driven over FCC1 MPC8560, MSC8144 UTP Port serves as Slave, MPC8560 as UTP Master

b. TDM[0–7] clock and sync are driven from clock distributor with enable. TDM[4:7] clock and sync are isolated for Mode 3. The MSC8144 TDM[0–3] ports connected directly to appropriated host TDM port, the upper multiplexed ports TDM[4–7] are connected to the host as transmit-to-receive cross.

c. Configured as output for testing against the host CPM

d. Over FCC2 MPC8560, MSC8144 is configured in Mode 1

Expansion Options 6

The MSC8144ADS has two options that provide for more expanded work:

- A PTMC expansion card allows expanded ethernet and video connections and serves as a verification tool for the MSC8144ADS.
- The AMC edge connector, with the appropriate connecting device, allows two MSC8144ADS boards to be connected back-to-back, or alternatively, allows an MSC8144ADS to be connected to a TUNDRA device or any other ATCA system.

6.1 PTMC Expansion Card

The PTMC expansion card allows expanded ethernet and video connections and serves as a verification tool for the MSC8144ADS. It has the following features:

- Compliance with PT3MC PMC configuration pinout and form-factor. PT5MC can also be made available
- Available configurations:
  - RMII-to-MAC and RMII-to-PHY connectivity
  - SMII-to-MAC and SMII-to-PHY connectivity
  - MII-to-MII PHY
- Includes clock sources for eight MSC8144 TDM ports
- Manually set for RMII and SMII configuration
- All PTMC signals on test headers are visible with a 0.1-inch separation between them
- UTOPIA-2 Master Connector by Adtech (adapter for the Slave connector)
- LEDs indicate the different available configurations
- I^2C bus for configuration switch programmingn

Table 6-1. PT3MC Cross-Interconnection

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J1-1	TCK	—	—	—	
J1-2	–12 V	—	—	—	
J1-3	GND	GND	—	—	
J1-4	INTA#	—	—	I,PU	To $\overline{IRQ2}$ MPC8560 Pull-Up on ADS

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J1-5	INTB#	—	—	I,PU	To $\overline{\text{IRQ3}}$ MPC8560 Pull-Up on ADS
J1-6	INTC#	—	—	I,PU	To $\overline{\text{IRQ4}}$ MPC8560 Pull-Up on ADS
J1-7	BUSMODE1#	—	—	I	“Card Present”, Pull-Up on the ADS, GND on PMC
J1-8	+5V	—	—	—	+5V Power
J1-9	INTD#	—	I,PU	—	To $\overline{\text{IRQ5}}$ MPC8560 Pull-Up on ADS
J1-10	RSRV	—	—	—	
J1-11	GND	GND	—	—	
J1-12	3.3Vaux	—	—	—	
J1-13	CLK	—	—	O	Common PCI_CLK
J1-14	GND	GND	—	—	
J1-15	GND	GND	—	—	
J1-16	GNT#	—	—	O	Connect to $\overline{\text{PCI\_GNT1}}$ of MPC8560
J1-17	REQ#	—	—	I	Connect to $\overline{\text{PCI\_REQ1}}$ of MPC8560
J1-18	+5V	—	—	—	+5V Power
J1-19	V(I/O)	—	—	—	+3.3V Power
J1-20	AD31	AD31/GE1_TXCLK/RxDATA0	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J1-21	AD28	AD28/GE1_TD1/RxDATA9	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J1-22	AD27	AD27/GE1_TD0/RxDATA2	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J1-23	AD25	AD25	PCI	I/O	Mode3/Mode1/Mode0
J1-24	GND	GND	—	—	
J1-25	GND	GND	—	—	
J1-26	C/BE3#	CBE3/GE1_RD1/RxDATA3	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J1-27	AD22	AD22/TDM6TCLK	PCI/TDM6	I/O	Mode3/Mode2 or Mode0
J1-28	AD21	AD21/TDM6RSYN or IDSEL/TDM7TCLK[b]	PCI/TDM6	I/O	Mode3/Mode2 or Mode0
J1-29	AD19	AD19/TDM6RCLK	PCI/TDM6	I/O	Mode3/Mode2 or Mode0
J1-30	+5V	—	—	—	+5V Power
J1-31	V(I/O)	—	—	—	+3.3V Power
J1-32	AD17	AD17/TDM5TDAT	PCI/TDM5	I/O	Mode3/Mode2 or Mode0
J1-33	FRAME#	FRAME/GE1_RD2/RxDATA4	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J1-34	GND	GND	—	—	
J1-35	GND	GND	—	—	
J1-36	IRDY#	IRDY/GE1_RD3/RxDATA5	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J1-37	DEV_SEL	DEVSEL/GPIO31	PCI	I/O	Mode3 or Mode2
J1-38	+5V	—	—	—	+5V Power
J1-39	GND	GND	—	—	
J1-40	LOCK#	—	—	O,PU	Pull-Up on the ADS
J1-41	RSRV	UTP_SRP/GPIO18	UTP2-16-POS	I	Mode7
J1-42	RSRV	UTP_IR/GPIO17	UTP2-16-POS	I	Mode7
J1-43	PAR	PAR/GE1_RX_CLK/RxDATA6	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J1-44	GND	GND	—	—	
J1-45	V(I/O)	—	—	—	+3.3V Power
J1-46	AD15	AD15/TDM5RSYN	PCI/TDM5	I/O	Mode3/Mode2 or Mode0
J1-47	AD12	AD12/TDM4TSYN	PCI/TDM4	I/O	Mode3/Mode2 or Mode0
J1-48	AD11	AD11/TDM4TDAT	PCI/TDM4	I/O	Mode3/Mode2 or Mode0
J1-49	AD09	AD9/TDM4RSYN	PCI/TDM4	I/O	Mode3/Mode2 or Mode0
J1-50	+5V	—	—	—	+5V Power
J1-51	GND	GND	—	—	
J1-52	C/BE0#	$\overline{\text{CBE0}}$/GE1_TX_EN/TxDATA6	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J1-53	AD06	AD6/GE1_RX_ER	PCI/GE1-MII	I/O	Mode3/Mode1
J1-54	AD05	AD5/GE1_CRS	PCI/GE1-MII	I/O	Mode3/Mode1
J1-55	AD04	AD4/TDM7TSYN	PCI/TDM7	I/O	Mode3 or Mode2/Mode1
J1-56	GND	GND	—	—	
J1-57	V(I/O)	—	—	—	+3.3V Power
J1-58	AD03	AD3/TDM7TDAT	PCI/TDM7	I/O	Mode3 or Mode2/Mode1
J1-59	AD02	AD2/TDM7RSYN	PCI/TDM7	I/O	Mode3 or Mode2/Mode1
J1-60	AD01	AD1/TDM7RDAT	PCI/TDM7	I/O	Mode3 or Mode2/Mode1
J1-61	AD00	AD0/TDM7RCLK	PCI/TDM7	I/O	Mode3 or Mode2/Mode1
J1-62	+5V	—	—	—	+5V Power
J1-63	GND	GND	—	—	
J1-64	REQ64#	—	—	—	Pull-Up on the ADS
J2-1	+12V	—	—	—	
J2-2	TRST#	—	—	—	
J2-3	TMS	—	—	—	
J2-4	TDO	—	—	—	
J2-5	TDI	—	—	—	
J2-6	GND	GND	—	—	
J2-7	GND	GND	—	v	
J2-8	RSRV	UTP_REOP	UTP2-16-POS	I	Mode7
J2-9	RSRV	GE1_RX_COL/RxDATA1	GE1MII/UTP2-16	I/O	Mode1/Mode0
J2-10	RSRV	UTP_TEOP	UTP2-16-POS	O	Mode7

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J2-11	BUSMODE 2#	—	—	O	ADS drives square pulse at PORESET to identify available CMC(PTMC) card presence
J2-12	+3.3V	—	—	—	+3.3V Power
J2-13	RST#	—	—	O	nHRST on ADS
J2-14	BUSMODE 3#	—	—	O	GND on the ADS
J2-15	+3.3V	—	—	—	+3.3V Power
J2-16	BUSMODE 4#	—	—	O	GND on the ADS
J2-17	PME#	—	—	O.D.	Pull-Up on ADS
J2-18	GND	GND	—	—	
J2-19	AD30	AD30/GE1_TD3/TxDATA5	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J2-20	AD29	AD29/GE1_TD2/TxDATA4	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J2-21	GND	GND	—	—	PTMC ID Pull-Down
J2-22	AD26	AD26	PCI	I/O	Mode3
J2-23	AD24	AD24/TDM6TSYN	PCI/TDM6	I/O	Mode3/Mode2 or Mode0
J2-24	+3.3V	—	—	—	+3.3V Power
J2-25	IDSEL	-[c]/TDM6TDAT	PCI/TDM7	I/O	Mode3 or Mode2/Mode0
J2-26	AD23	AD23/TDM6TSYN	PCI/TDM6	I/O	Mode3/Mode2 or Mode0
J2-27	+3.3V	—	—	—	+3.3V Power
J2-28	AD20	AD20/TDM6RDAT	PCI/TDM6	I/O	Mode3/Mode2 or Mode0
J2-29	AD18	AD18/TDM5TSYN	PCI/TDM5	I/O	Mode3/Mode2 or Mode0
J2-30	GND	GND	—	—	
J2-31	AD16	AD16/TDM5TCLK	PCI/TDM5	I/O	Mode3/Mode2 or Mode0
J2-32	C/BE2#	$\overline{\text{CBE2}}$/GE1_RD0/RxDATA2	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J2-33	GND	GND	—	—	
J2-34	RSRV	GE2_RD0	GE2-RMII[e]	I/O	Mode3 or Mode2
J2-35	TRDY#	TRDY	PCI	I/O	Mode3 or Mode2
J2-36	+3.3V	—	—	—	+3.3V Power
J2-37	GND	GND	—	—	
J2-38	STOP#	STOP/GPIO30	PCI	I/O	Mode3 or Mode2
J2-39	PERR#	$\overline{\text{PERR}}$/TxDATA1	PCI/UTP2-16	I/O	Pull-Up on ADS
J2-40	GND	GND	—	—	
J2-41	+3.3V	—	—	—	+3.3V Power
J2-42	SERR#	$\overline{\text{SERR}}$/TxDATA0	PCI/UTP2-16	—	Pull-Up on ADS
J2-43	C/BE1#	$\overline{\text{CBE1}}$/GE1_TX_ER/TxDATA7	PCI/GE1-MII/UTP2-16	I/O	Mode3/Mode1/Mode0
J2-44	GND	GND	—	—	
J2-45	AD14	AD14/TDM5RDAT	PCI/TDM5	I/O	Mode3/Mode2 or Mode0

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J2-46	AD13	AD13/TDM5RCLK	PCI/TDM5	I/O	Mode3/Mode2 or Mode0
J2-47	M66EN	—	—	—	To ADS MODCK Logic
J2-48	AD10	AD10/TDM4TCLK	PCI/TDM4	I/O	Mode3/Mode2 or Mode0
J2-49	AD08	AD8/TDM4RDAT	PCI/TDM4	I/O	Mode3/Mode2 or Mode0
J2-50	+3.3V	—	—	—	+3.3V Power
J2-51	AD07	AD7/TDM4RCLK	PCI/TDM4	I/O	Mode3/Mode2 or Mode0
J2-52	RSRV	GE2_RD1	GE2-RMII[e]	I/O	Mode3 or Mode2
J2-53	+3.3V	—	—	—	+3.3V Power
J2-54	RSRV	GE2_RX_DV	GE2-RMII[e]	I/O	Mode3 or Mode2
J2-55	RSRV	GE2_TD0	GE2-RMII[e]	I/O	Mode3 or Mode2
J2-56	GND	GND	—	—	
J2-57	RSRV	GE2_RX_ER	GE2-RMII[e]	I/O	Mode3 or Mode2
J2-58	RSRV	GE2_TD1	GE2-RMII[e]	I/O	Mode3 or Mode2
J2-59	GND	GND	—	—	
J2-60	RSRV	GE2_TX_EN	GE2-RMII[e]	I/O	Mode3 or Mode2
J2-61	ACK64#	—	—	—	Pull-Up on ADS
J2-62	+3.3V	—	—	—	+3.3V Power
J2-63	GND	GND	—	—	
J2-64	RSRV	GE2_CLK	GE2-RMII[e]	I/O	Mode3 or Mode2
J3-1	MDIO	GE1_MDIO	GE1[d]	I/O	RMII/SMII[e] Mode
J3-2	GND	GND	—	—	
J3-3	GND	GND	—	—	
J3-4	STX	UTXD/GPIO15	UART	I/O	
J3-5	MDC	GE1_MDC	GE1	I/O	RMII/SMII[e] Mode
J3-6	SRX	URXD/GPIO14	UART	I/O	On board RS232 transc. has enable
J3-7	RxER	GE1_RX_ER	GE1	I/O	RMII/SMII[e] Mode
J3-8	GND	GND	—	—	
J3-9	PTID2	—	—	—	PTMC ID Pull-Down
J3-10	TxD0	GE1_TD0/TxDATA2	GE1/UTP2-16	I/O	RMII/SMII[e] Mode
J3-11	PTGNDZ	—	—	—	Special Purpose GND
J3-12	TxD1	GE1_TD1/TxDATA3	GE1/UTP2-16	I/O	RMII[e] Mode
J3-13	REFCLK	GE1_TX_CLK/RxDATA0	GE1/UTP2-16	I/O	RMII/SMII[e] Mode
J3-14	GND	GND	—	—	
J3-15	GND	GND	—	—	
J3-16	RxD0	GE1_RD0/RxDATA2	GE1/UTP2-16	I/O	RMII/SMII[e] Mode
J3-17	CT_FA	TDM0TSYN	TDM0	O	Main TDM SYNC[f]

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J3-18	RxD1	GE1_RD1/RxDATA3	GE1/UTP2-16	I/O	RMII[e] Mode
J3-19	CT_FB	TDM1TSYN	TDM1	I	Add. SYNC1[g]
J3-20	GND	GND	-	-	
J3-21	PTID0	-	-	-	PTMC ID Pull-Down
J3-22	TXEN	G1_TX_EN/TxDATA6	GE1/UTP2-16	I/O	RMII[e] Mode
J3-23	PTGNDZ	-	-	-	Special Purpose GND
J3-24	CAS_DV	GE1_RX_DV/RxDATA7	GE1/UTP2-16	I/O	RMII[e] Mode
J3-25	CT_C8A	TDM0TCLK	TDM0	O	Main TDM CLOCK
J3-26	GND	GND	-	-	
J3-27	GND	GND	-	-	
J3-28	CT_D19	TDM4TDAT	TDM4	I/O	Mode 2, PCI pin for Mode 3
J3-29	CT_D18	TDM4RCLK	TDM4	I/O	Mode 2, PCI pin for Mode 3
J3-30	CT_D17	TDM4RSYN	TDM4	I/O	Mode 2, PCI pin for Mode 3
J3-31	CT_D16	TDM4RDAT	TDM4	I/O	Mode 2, PCI pin for Mode 3
J3-32	GND	GND	-	-	
J3-33	GND	GND	-	-	
J3-34	NETREF2	TDM2TSYN	TDM2	I	Misc. Master SYNC[h]
J3-35	CT_D14	TDM3RCLK	TDM3	I/O	Any Mode
J3-36	USER1Z	TDM3TSYN	TDM3	I/O	Any Mode
J3-37	CT_D12	TDM3RDAT	TDM3	I/O	Any Mode
J3-38	GND	GND	-	-	
J3-39	PTENB#[i]	-	-	-	PTMC Enable (low) BCSR bit Pull-Up 47k
J3-40	USER2Z	TDM3TCLK	TDM3	I/O	Any Mode
J3-41	PTGNDZ	-	-	-	Special Purpose GND
J3-42	NETREF1	TDM2TCLK	TDM2	I	Misc. Master CLOCK[h]
J3-43	CT_C8B	TDM1TCLK	TDM1	I	Secondary Master Clock[j]
J3-44	GND	GND	-	-	
J3-45	GND	GND	-	-	
J3-46	CT_D15	TDM3TDAT	TDM3	I/O	Any Mode
J3-47	CT_D10	TDM2RCLK	TDM2	I/O	Any Mode
J3-48	CT_D13	TDM3RSYN	TDM3	I/O	Any Mode
J3-49	CT_D8	TDM2RDAT	TDM2	I/O	Any Mode
J3-50	CT_D11	TDM2TDAT	TDM2	I/O	Any Mode
J3-51	GND	GND	-	-	
J3-52	CT_D9	TDM2RSYN	TDM2	I/O	Any Mode
J3-53	CT_D6	TDM1RCLK	TDM1	I/O	Any Mode
J3-54	CT_D7	TDM1TDAT	TDM1	I/O	Any Mode

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J3-55	CT_D4	TDM1RDAT	TDM1	I/O	Any Mode
J3-56	GND	GND	-	-	
J3-57	PTID1	-	-	O	PTMC ID Pull-Down
J3-58	CT_D5	TDM1RSYN	TDM1	I/O	Any Mode
J3-59	CT_D2	TDM0RCLK	TDM0	I/O	Any Mode
J3-60	CT_D3	TDM0TDAT	TDM0	I/O	Any Mode
J3-61	CT_D0	TDM0RDAT	TDM0	I/O	Any Mode
J3-62	GND	GND	-	-	
J3-63	GND	GND	-	-	
J3-64	CT_D1	TDM0RSYN	TDM0	I/O	Any Mode
J4-1	TxSOC	RxSOC	UTP2-8/16	I/O	Mode3/Mode0/Mode2
J4-2	GND	GND	-	-	
J4-3	GND	GND	-	-	
J4-4	RxADR4	TxADDR4	UTP2-8/16	I/O	Mode3/Mode0
J4-5	TxCLAV	RxCLAV	UTP2-8/16	I/O	Mode3/Mode0[l]
J4-6	TxADR4	RxADDR4	UTP2-8/16	I/O	Mode3/Mode0
J4-7	RxADR3	TxADDR3	UTP2-8/16	I/O	Mode3/Mode0
J4-8	GND	GND	-	-	
J4-9	USER	-	-	O	FPGA CTRL1
J4-10	GND	GND	-	-	
J4-11	GND	GND	-	-	
J4-12	RxREF	RCLK	UTP2-8/16	-	Driven from the host or PTMC Card
J4-13	TxREF	TCLK	UTP2-8/16	-	Driven from the host or PTMC Card
J4-14	GND	GND	-	-	
J4-15	GND	GND	-	-	
J4-16	RxENB#	TxENB	UTP2-8/16	I/O	Mode3/Mode0[k]
J4-17	TxADR3	RxADDR3	UTP2-8/16	I/O	Mode3/Mode0
J4-18	RxCLAV	TxCLAV	UTP2-8/16	I/O	Mode3/Mode0[l]
J4-19	TxADR2	RxADDR2	UTP2-8/16	I/O	Mode3/Mode0
J4-20	GND	GND	-	I/O	
J4-21	USER	-	-	I/O	FPGA CTRL2
J4-22	TxENB#	RxENB	UTP2-8/16	I/O	Mode3/Mode0[k]
J4-23	GND	GND	-	I/O	
J4-24	RxADR2	TxADDR2	UTP2-8/16	I/O	Mode3/Mode0
J4-25	GND	GND	UTP2-8/16	I/O	Mode3/Mode0
J4-26	TxCLK	RxCLK	UTP2-8/16	I/O	Mode3/Mode0

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J4-27	GND	GND	-	I/O	
J4-28	TxADR1	RxADDR1	UTP2-8/16	I/O	Mode3/Mode0
J4-29	TxADR0	RxADDR0	UTP2-8/16	I/O	Mode3/Mode0
J4-30	RxADR1	TxADDR1	UTP2-8/16	I/O	Mode3/Mode0
J4-31	TxPRTY	RxPRTY and SPI_MISO/GPIO23 over serial resistor	UTP2-8/16/PCI	I/O	Mode3/Mode0/Mode2
J4-32	GND	GND		-	
J4-33	GND	GND		-	
J4-34	RxADR0	TxADDR0	UTP2-8/16	I/O	Mode3/Mode0
J4-35	TxD7	RxDATA15	UTP2-8/16	I/O	Mode3/Mode0
J4-36	RxPRTY	TxPRTY and SPI_MOSI/GPIO22 over serial resistor	UTP2-8/16	I/O	Mode3/Mode0
J4-37	TxD6	RxDATA14	UTP2-8/16	I/O	Mode3/Mode0
J4-38	GND	GND	-	-	
J4-39	USER2	SDA/GPIO27	I^2C	I/O,O. D.	Pull-Up on ADS
J4-40	RxD7	TxDATA15	UTP2-8/16	I/O	Mode3/Mode0
J4-41	GND	GND	-	-	
J4-42	RxD6	TxDATA14	UTP2-8/16	I/O	Mode3/Mode0
J4-43	RxCLK	TxCLK	UTP2-8/16	I/O	Mode3/Mode0
J4-44	GND	GND	-	-	
J4-45	GND	GND	-	-	
J4-46	RxD5	TxDATA13	UTP2-8/16	I/O	Mode3/Mode0
J4-47	TxD5	RxDATA13	UTP2-8/16	I/O	Mode3/Mode0
J4-48	RxD4	TxDATA12	UTP2-8/16	I/O	Mode3/Mode0
J4-49	TxD4	RxDATA12	UTP2-8/16	I/O	Mode3/Mode0
J4-50	GND	GND	-	-	
J4-51	GND	GND	-	-	
J4-52	RxD3	TxDATA11	UTP2-8/16	I/O	Mode3/Mode0
J4-53	TxD3	RxDATA11	UTP2-8/16	I/O	Mode3/Mode0
J4-54	RxD2	TxDATA10	UTP2-8/16	I/O	Mode3/Mode0
J4-55	TxD2	RxDATA10	UTP2-8/16	I/O	Mode3/Mode0
J4-56	GND	GND	-	-	
J4-57	USER3	SCL/GPIO26	I^2C	I/O,O. D.	Pull-Up on ADS
J4-58	RxD1	TxDATA9	UTP2-8/16	I/O	Mode3/Mode0
J4-59	TxD1	RxDATA9	UTP2-8/16	I/O	Mode3/Mode0
J4-60	RxD0	TxDATA8	UTP2-8/16	I/O	Mode3/Mode0
J4-61	TxD0	RxDATA8	UTP2-8/16	I/O	Mode3/Mode0
J4-62	GND	GND	-	-	

Table 6-1. PT3MC Cross-Interconnection (Continued)

Connector	Signal Name	MSC8144 Signal[a]	MSC8144 Port	DIR to ADS	Comment
J4-63	GND	GND	-	-	
J4-64	RxSOC	TxSOC	UTP2-8/16	I/O	Mode3/Mode0

a. MSC8144 UTP8/16 acts as Slave by default at address “0”, on-PTMC UTP Slave gets address “1” for UTP multiphy mode
b. Select by nTDMx4 BCSR control signal.
c. Serves as IDSEL for PCI bus over PTMC. Connect to AD20.
d. Not available in ext. signals mode 3
e. RMII/SMII I/F has become available after moving h/w bridges on the ADS in proper position.
f. To support CT-bus over PTMC TDM ports 0 to 3 should be configured in “Shared Frame Sync, Clock, and Data Links” Mode.
g. Acts as Rxsync for Shared Modes
h. Use for TDM Independent Mode
i. PCI Telecom Enable PTENB#. This signal should prevent available circuit damage for combinations with PTCC cards.
j. Acts as Rxclk for Shared Modes
k. 10k pull-up on ADS for UTP MultiPhy Mode
l. 470OHM pull-down on ADS for UTP MultiPhy Mode

Table 6-2. Interface Multiplexing

MSC8144 Port	MSC8144 pin mode	Host Port	PTMC configured as		AMC	Comment
			PT3MC	PT5MC[a]		
PCI 32 bit (planar)	3	PCI host	Connect to MSC8144 & host	Connect to the host PCI	—	—
PCI 32 full	2	Isolated	Presented on non-PCI pins		—	—
Utopia-16 Slave	3	Utopia-16 Master	Utopia-8 Slave	—	—	—
TDMx4 ports: TDM[0–3]	3	TDM[A,B,C,D]-1	20-lane CT-bus		20-lane CT-bus	20-lane CT-bus
TDMx8 ports: TDM[0–7]	2	TDM[A,B,C,D]-1 TDM[A,B,C,D]-2	20-lane CT-bus	32-lane CT-bus	32-lane CT-bus	32-lane CT-bus
GE1-MII	1	CPM	—	—	—	Test Mode h/w setting
GE1-RMII/SMII	2	CPM	RMII	—	—	
GE2-RMII/SMII	2	—	GE2-RMII over reserved pins	—	—	

a.Reached with hw production setting

6.2 AMC in ATCA Environment

The AMC edge connector, with the appropriate connecting device, allows two MSC8144ADS boards to be connected back-to-back, or alternatively, allows an MSC8144ADS to be connected to a TUNDRA device, or any other ATCA system.

The AMC connecting module is shown in Figure 6-1. Fasten the connecting module (by hand) to the AMC edge connector as shown in **Figure 6-2**. Two MSC8144ADS boards are shown connected to each other via the AMC connecting module in **Figure 6-3**.

Figure 6-1. AMC Connecting Module

Figure 6-2. Fastening the AMC Module to the Edge Connector

Figure 6-3. Two MSC8144ADS Boards Connected, Back-to-back

Table 6-3 below describes the signals that are routed to the AMC edge connector.

Table 6-3. AMC Edge Connector Assignment

Pin #	AMC Name	Connection to MSC8144	ATCA Carrier Board Signal
3	PS1		Power Sense 1 Connect to 83 on the ADS
11,12	TX0+/-	GE1 through SGMII Switch 88E6152 Port 9	
14,15	RX0+/-		
29,30	TX2+/-	GE2 through SGMII Switch 88E6152 Port 7	
32,33	RX2+/-		
41	ENABLE#	—	PU. To MMC on ADS
44,45	TX6+/-	SRIO_TX0+/-	sRIO 1x
47,48	RX6+/-	SRIO_RX0+/-	
50,51	TX7+/-	SRIO_TX1+/-	
53,54	RX7+/-	SRIO_RX1+/-	
56	SCL_L	—	I^2C to ADS MMC (optional)
59,60	TX6+/-	SRIO_TX2+/-	Muxed with GE1 SGMII on MSC8144ADS
62,63	RX6+/-	SRIO_RX2+/-	
65,66	TX7+/-	SRIO_TX3+/-	Muxed with GE2 SGMII on MSC8144ADS
68,69	RX7+/-	SRIO_RX3+/-	
71	SCA_L	—	I^2C to ADS MMC (optional)
83	PS0		Power Sense 0 Connect to 3 on the ADS
163	TX20+	Fxclk (TDM0TCLK)[a]	RTM01 - ST_8A
162	TX20-	Fxsync (TDM0TSYN)	RTM02 - ST_FA
160	RX20+	—	RTM03 - ST_8B
159	RX20-	—	RTM04 - ST_FB
157	TX19+	Fxdata31(TDM7TDAT)	RTM05 - ST_D31
156	TX19-	Fxdata30(TDM7RCLK)	RTM06 - ST_D30
148	RX19+	Fxdata29(TDM7RSYN)	RTM07 - ST_D29
147	RX19-	Fxdata28(TDM7RDAT)	RTM08 - ST_D28
151	TX18+	Fxdata27(TDM6TDAT)	RTM09 - ST_D27
150	TX18-	Fxdata26(TDM6RCLK)	RTM10 - ST_D26
148	RX18+	Fxdata25(TDM6RSYN)	RTM11 - ST_D25
147	RX18-	Fxdata24(TDM6RDAT)	RTM12 - ST_D24
145	TX17+	Fxdata23(TDM5TDAT)	RTM13 - ST_D23
144	TX17-	Fxdata22(TDM5RCLK)	RTM14 - ST_D22
142	RX17+	Fxdata21(TDM5RSYN)	RTM15 - ST_D21
141	RX17-	Fxdata20(TDM5RDAT)	RTM16 - ST_D20

Table 6-3. AMC Edge Connector Assignment (Continued)

Pin #	AMC Name	Connection to MSC8144	ATCA Carrier Board Signal
139	TX16+	Fxdata19(TDM4TDAT)	RTM17 - ST_D19
138	TX16-	Fxdata18(TDM4RCLK)	RTM18 - ST_D18
136	RX16+	Fxdata17(TDM4RSYN)	RTM19 - ST_D17
135	RX16-	Fxdata16(TDM4RDAT)	RTM20 - ST_D16
133	TX15+	Fxdata15(TDM3TDAT)	RTM21 - ST_D15
132	TX15-	Fxdata14(TDM3RCLK)	RTM22 - ST_D14
130	RX15+	Fxdata13(TDM3RSYN)	RTM23 - ST_D13
129	RX15-	Fxdata12(TDM3RDAT)	RTM24 - ST_D12
127	TX14+	Fxdata11(TDM2TDAT)	RTM25 - ST_D11
126	TX14-	Fxdata10(TDM2RCLK)	RTM26 - ST_D10
124	RX14+	Fxdata9(TDM2RSYN)	RTM27 - ST_D09
123	RX14-	Fxdata8(TDM2RDAT)	RTM28 - ST_D08
121	TX13+	Fxdata7(TDM1TDAT)	RTM29 - ST_D07
120	TX13-	Fxdata6(TDM1RCLK)	RTM30 - ST_D06
118	RX13+	Fxdata5(TDM1RSYN)	RTM31 - ST_D05
117	RX13-	Fxdata4(TDM1RDAT)	RTM32 - ST_D04
115	TX12+	Fxdata3(TDM0TDAT)	RTM33 - ST_D03
114	TX12-	Fxdata2(TDM0RCLK)	RTM34 - ST_D02
112	RX12+	Fxdata1(TDM0RSYN)	RTM35 - ST_D01
111	RX12-	Fxdata0(TDM0RDAT)	RTM36 - ST_D00

a. MSC8144 TDM ports is in “Shared Frame,Sync,Clock and Data Link” mode

Replacing the MSC8144 DSP 7

To remove the MSC8144 processor, follow the instructions in **Figure 7-1** to **Figure 7-5** below. To replace the MSC8144 processor, align the chip properly as shown in **Figure 7-6**, then follow the instructions in **Figure 7-5** to **Figure 7-1** below (in that order).

Note: The Allen wrench is provided in the tool kit.

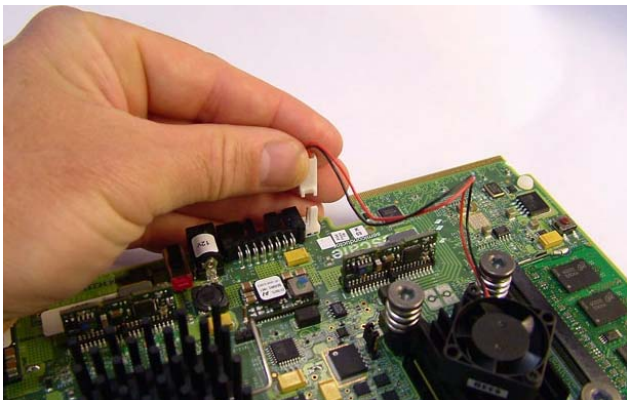


Figure 7-1. Disconnect Fan

Figure 7-2. Loosen Allen screws

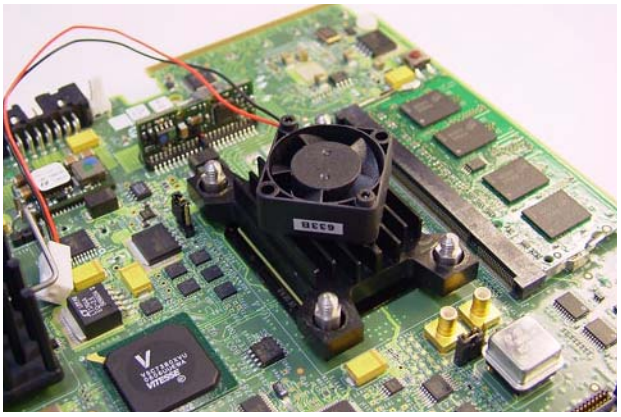


Figure 7-3. Remove Allen Screws

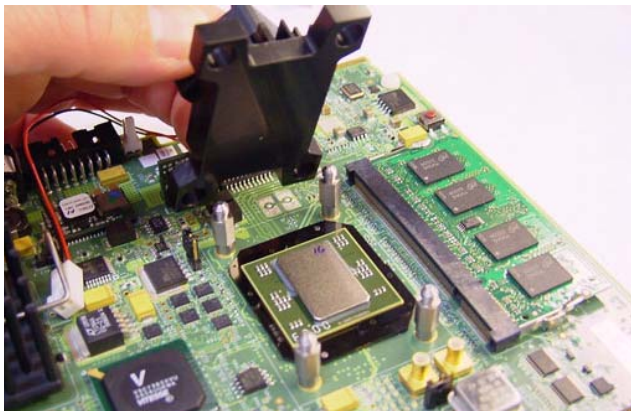


Figure 7-4. Remove Heat Sink

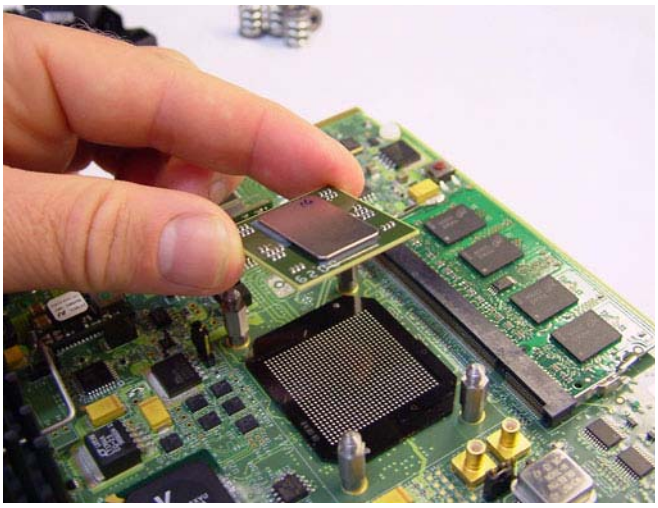


Figure 7-5. Remove Chip

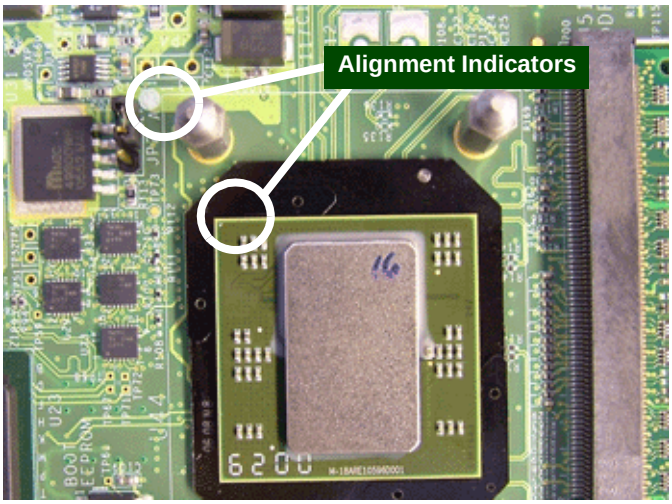


Figure 7-6. Chip Alignment: Correct

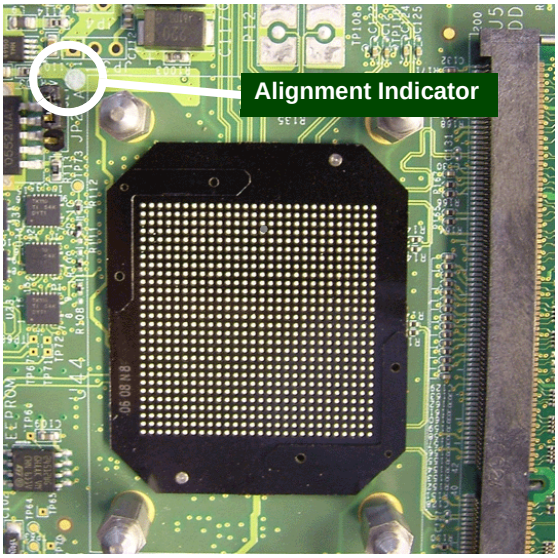


Figure 7-7. Chip Alignment: Indicator on Board

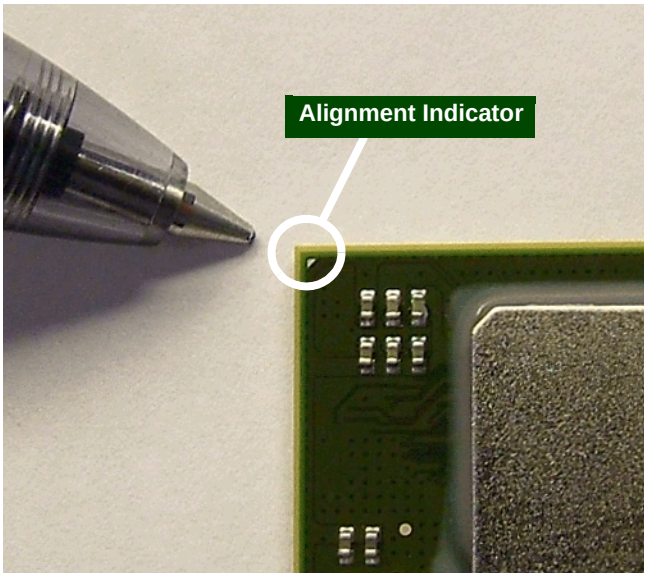


Figure 7-8. Chip Alignment: Indicator on Chip