I.MX 6ULL, 6SLL, 7D产品深入探讨

EXTERNAL

SECURE CONNECTIONS
FOR A SMARTER WORLD

i.MX Processor Roadmap

i.MX 6 QuadPlus
↓
i.MX 6 Quad
↓
i.MX 6 DualPlus
↓
i.MX 6 Dual
↓
i.MX 6 DualLite
↓
i.MX 6 Solo
↓
i.MX 6 SoloX
↓
i.MX 6 SoloLite
↓
i.MX 6SLL
↓
i.MX 6 UltraLite
↓
i.MX 6ULL

ARM® v7-A

i.MX 8 family
Advanced Graphics & Performance

i.MX 8M family
Advanced Audio & Video

i.MX 8X family
Safety Certifiable & Efficient Performance

ARM® v8-A
(32-bit/ 64-bit)

i.MX 7 family
Flexible Efficient Connectivity

i.MX 7ULP family
Ultra Low Power with Graphics

ARM® v7-A
(32-bit)

I.MX 6ULL

i.MX 6 Series: Supreme Scalability and Flexibility
Leverage One Design into Diverse Product Portfolio

Scalable series of **Eleven** ARM-based SoC Families

i.MX 6ULL	i.MX 6UltraLite	i.MX 6SoloLite	i.MX 6SoloLite	i.MX 6SoloX	i.MX 6Solo	i.MX 6DualLite	i.MX 6Dual	i.MX 6DualPlus	i.MX 6Quad	i.MX 6QuadPlus
i.MX 6 ULL Family	i.MX 6UltraLite Family	i.MX 6 SLL Family	i.MX 6SoloLite Family	i.MX 6SoloX Family	i.MX 6Solo Family	i.MX 6DualLite Family	i.MX 6Dual Family	i.MX 6DualPlus Family	i.MX 6Quad Family	i.MX 6QuadPlus Family

Pin-to-pin Compatible

Pin-to-pin Compatible

Pin-to-pin Compatible

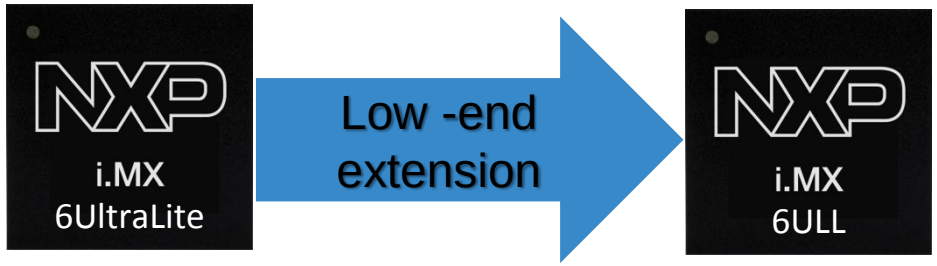
Software Compatible

Expanded series for performance, power efficiency and lower BOM

i.MX 6ULL Objective

Offer a lower power and lower price i.MX 6 family member

- “i.MX 6UL is great but I need something that is below $3 for consumer applications.”
- “My customers are always looking for lower power processors”.
- “I need an upgrade for my i.MX2x design and I don’t need the full security of i.MX 6UL.”
- “The distribution margin on i.MX 6 G0 is very low, the distributors are not pushing hard.”



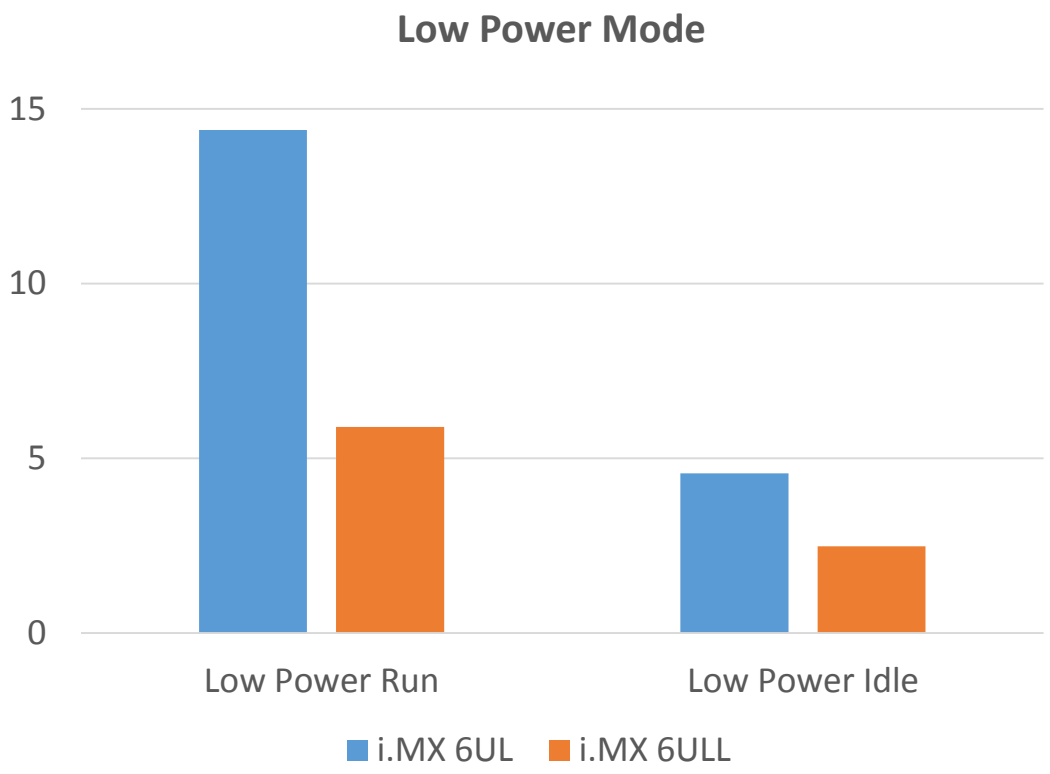
i.MX 6ULL

- ARM Cortex-A7 @ up to 900MHz
- 128 KB L2 cache
- 16-bit LPDDR2/DDR3
- Linux, FreeRTOS

Key Changes:

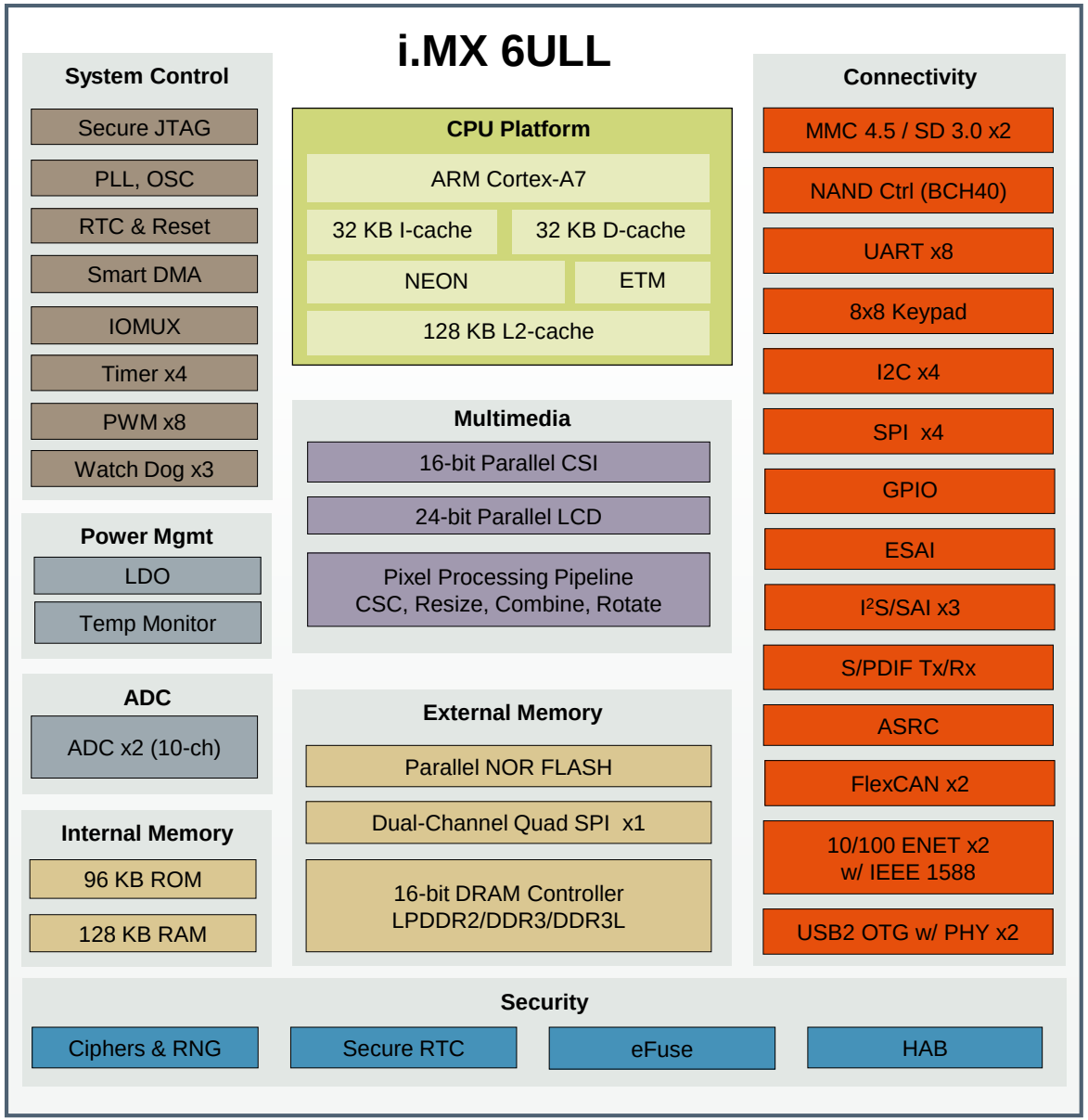
1. No Automotive grade
2. No G3 Security options
3. Up to 900MHz
4. Lower Power
5. Lower Price

i.MX 6ULL Power Consumption



i.MX 6ULL Application Processor

- **Specifications**
  - **Core voltage:** 1.1V
  - **Package:** 289 MAPBGA, 14x14mm, 0.8mm pitch
    272 MAPBGA, 9x9mm, 0.5mm pitch
  - **Temperature:** -40C to 105C (Tj)
- **Key Features and Advantages**
  - ARM Cortex-A7 @ up to 900 MHz, 128 KB L2 cache
  - Parallel LCD Display up to WXGA (1366x768)
  - 8/10/16/24-bit Parallel Camera Sensor Interface
  - 16-bit LP-DDR2, DDR3/DDR3L
  - 8/16-bit Parallel NOR FLASH / PSRAM
  - Dual-channel Quad-SPI NOR FLASH
  - 8-bit Raw NAND FLASH with 40-bit ECC
  - 2x MMC 4.5/SD 3.0/SDIO Port
  - 2x USB 2.0 OTG, HS/FS, Device or Host with PHY
  - Audio Interfaces include ESAI, 3x I2S/SAI, S/PDIF Tx/Rx
  - 2x 10/100 Ethernet with IEEE 1588
  - 2x 12-bit ADC, up to 10 input channel total, with resistive touch controller
  - Partial PMU Integration
- **Enablement**
  - Linux BSP from NXP
  - FreeRTOS BSP from NXP



I.MX 7

i.MX 7Solo

- Single ARM® Cortex®-A7 up to 800 MHz
- Cortex-M4 up to 200 MHz
- 512KB L2 cache
- 16/32-bit DDR3/DDR3L and LPDDR2/3 at 533 MHz
- Single Gigabit Ethernet (AVB)
- **Full security with tamper resist**

i.MX 7Dual

- Dual ARM® Cortex®-A7 up to 1.0 GHz
- Cortex-M4 up to 200 MHz
- 512 KB L2 cache
- 16/32-bit DDR3/DDR3L and LPDDR2/3 at 533 MHz
- Dual Gigabit Ethernet (AVB)
- **Full security with tamper resist**
- EPD controller
- PCIe (x1 lane)

Red indicates change from column to the left

Pin-to-pin and power compatible

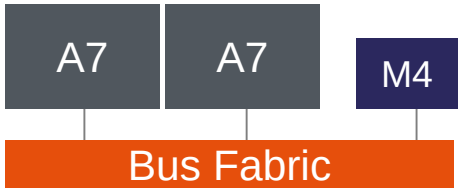
Software compatible

Consumer

Extended Consumer

Advanced Heterogeneous Architecture

- Up to Dual Cortex-A7 @ 1GHz
- Cortex-M4 @ 200MHz
  - Offload Tasks
  - Optimize Power
  - Increase Security



Unmatched Power Efficiency

- 3x improvement in Power Efficiency vs i.MX 6
- 100 uW/MHz for Cortex-A7
- 70 uW/MHz for Cortex-M4
- One third the power consumed in the Low Power suspend mode (250uW) vs i.MX 6

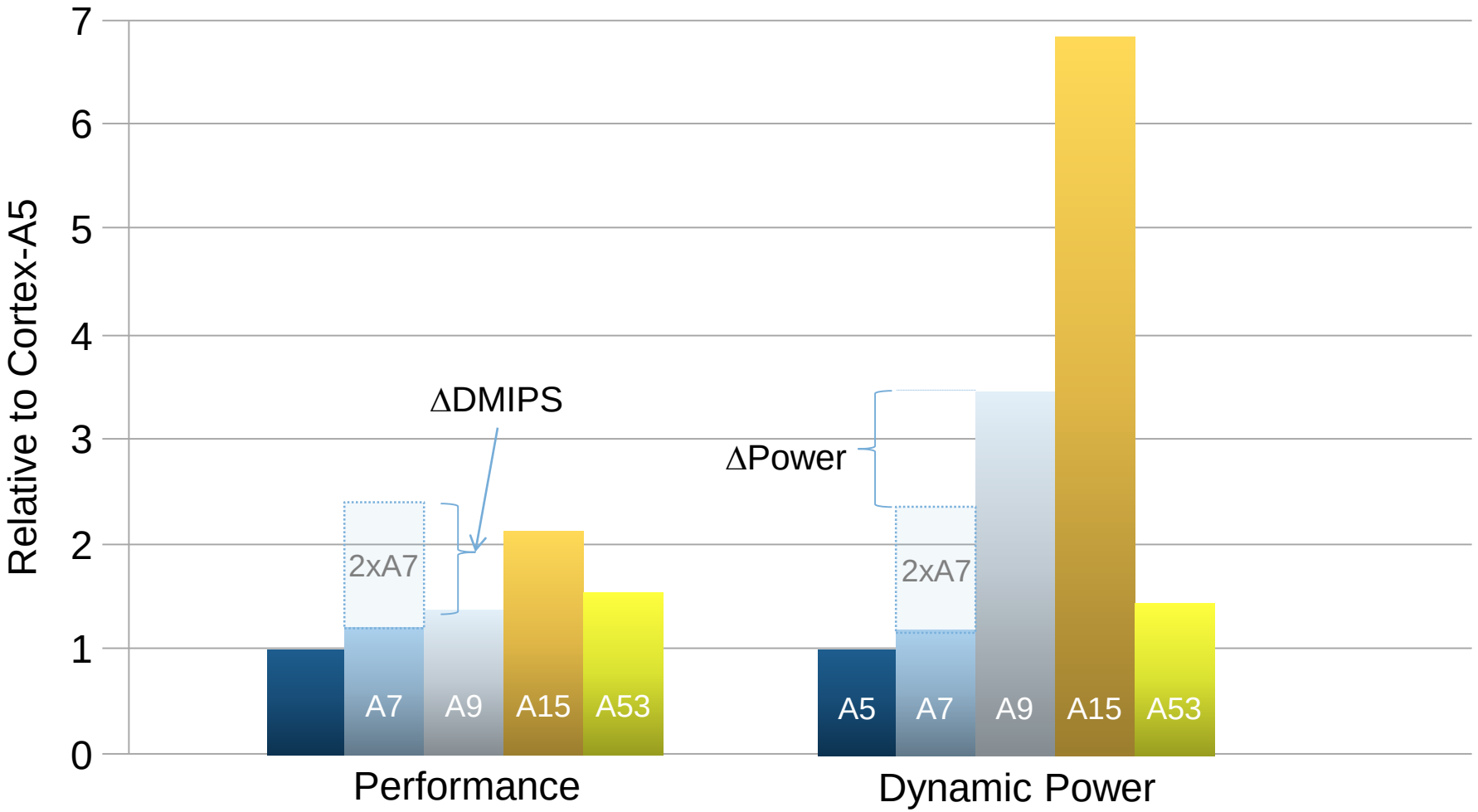
Enabling Flexible High Speed Connectivity

- PCI-e v2.1
- Dual Gbit Ethernet with AVB
- DDR QuadSPI support
- eMMC 5.0

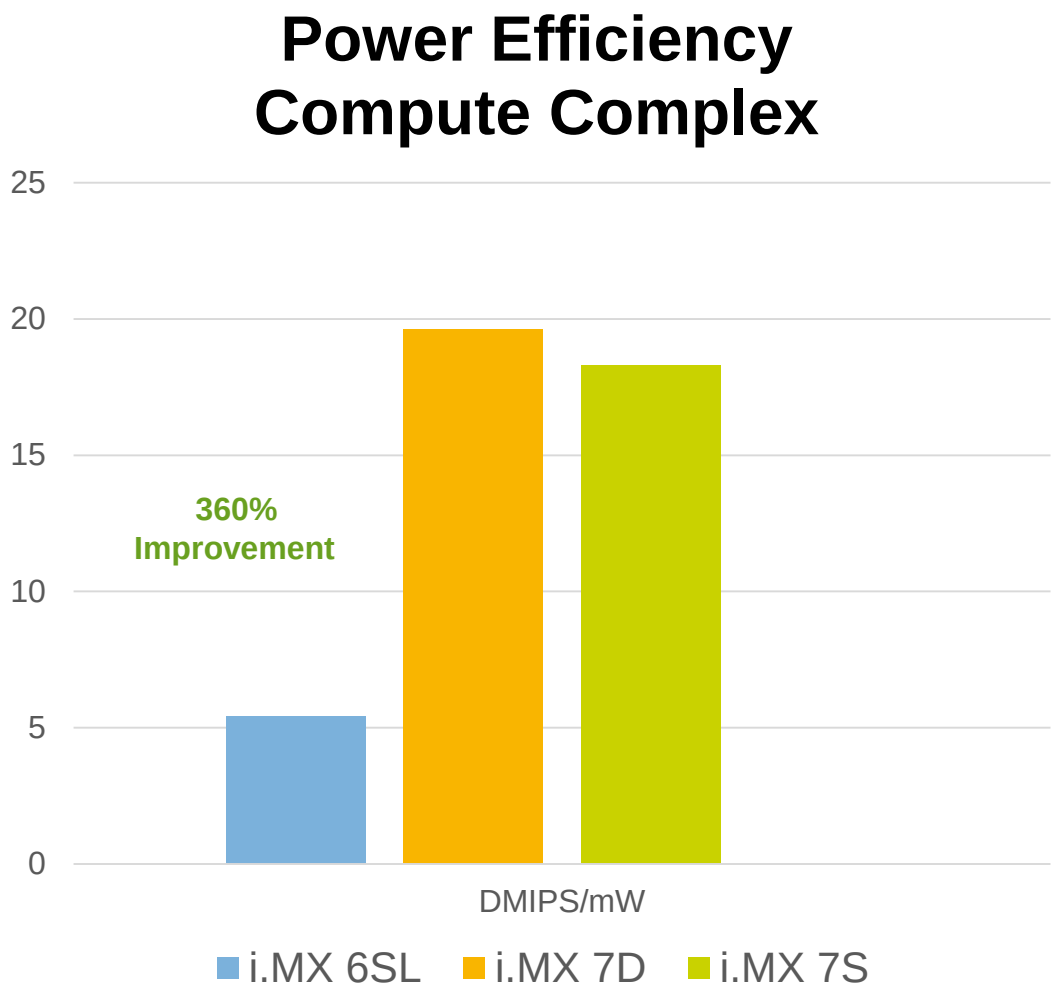
Complete Security Infrastructure

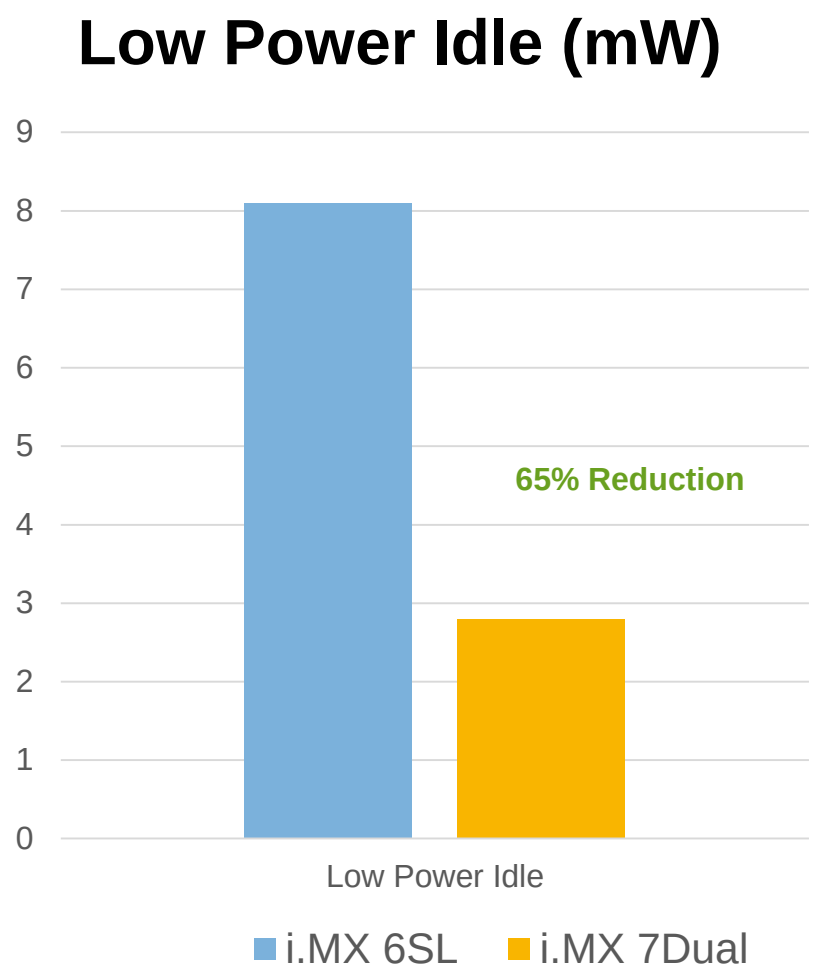
- Secure Boot
- Crypto H/W Acceleration
- Internal and External Tamper Detection
- Secure RAM
- DPA attack Resistance
- Secure JTAG

Comparison (2xCortex-A7 vs 1xCortexA9)

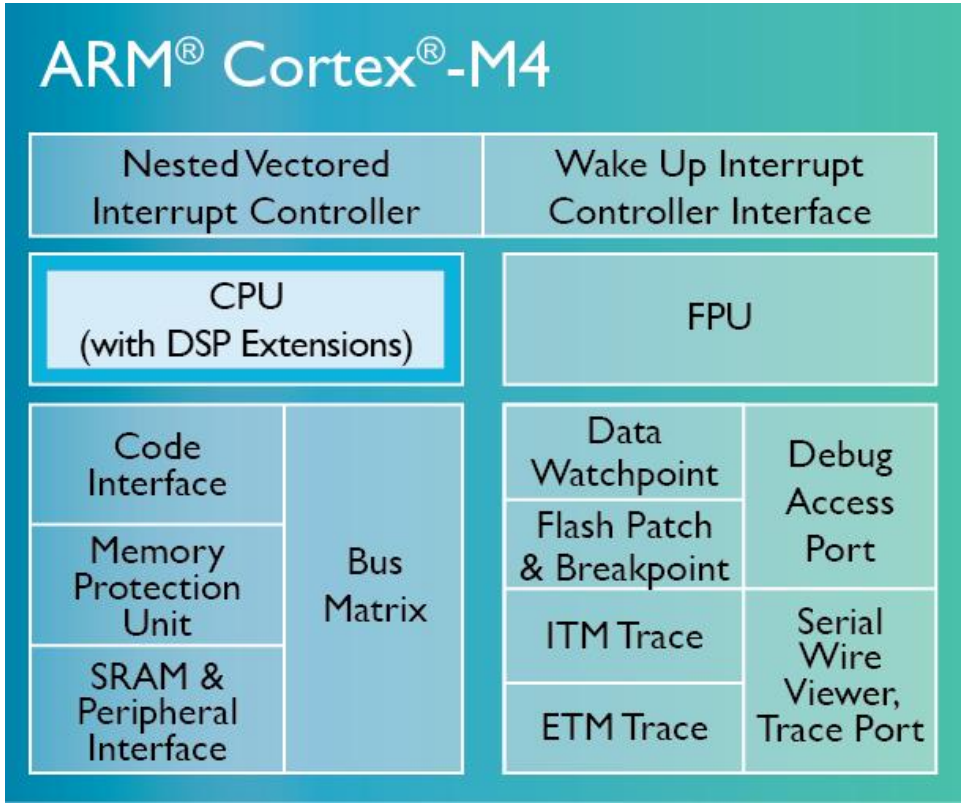


Performance is Specint2000 at synthesized frequency
Area is core with Neon + L1 cache, with L2 controller, MP1 configuration, no L2 RAM included
Power measured as Dhrystone at nominal voltage


Power Efficiency
Compute Complex
25
20
15
10
5
0
360%
Improvement
DMIPS/mW
i.MX 6SL
i.MX 7D
i.MX 7S

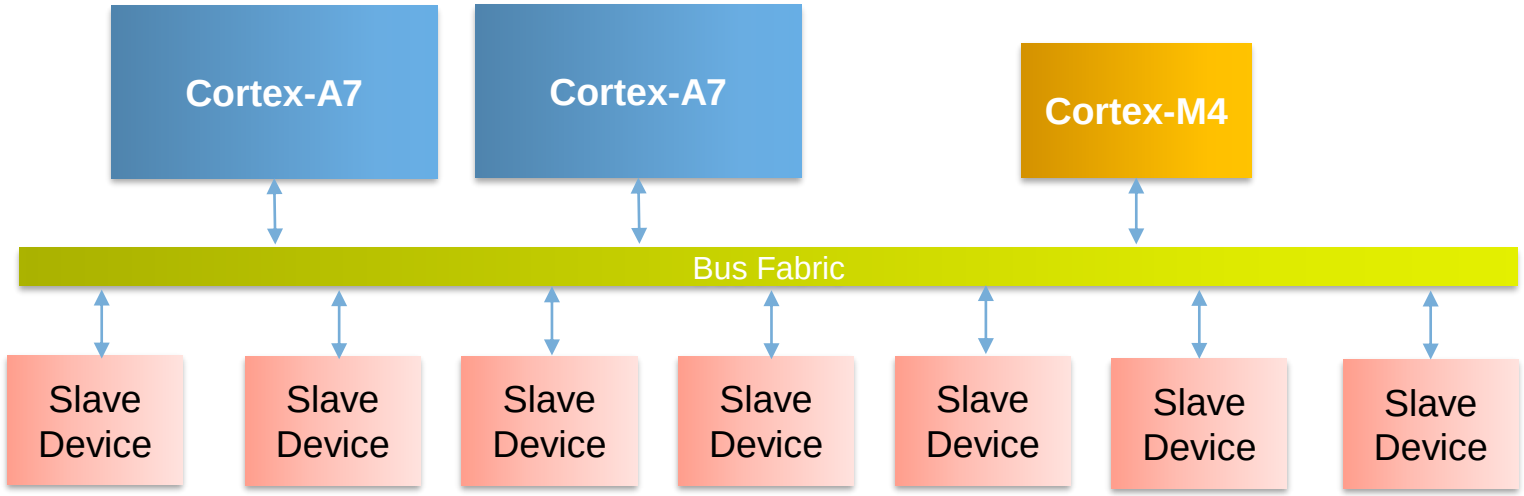

Low Power Idle (mW)
9
8
7
6
5
4
3
2
1
0
65% Reduction
Low Power Idle
i.MX 6SL
i.MX 7Dual

- ARMv7-M
- Thumb-2
- DSP Extensions & SIMD arithmetic
- FPU - Single precision floating point unit, IEEE 754 compliant
- 3.40 CoreMark/MHz



Heterogeneous Multicore Processing (HMP)

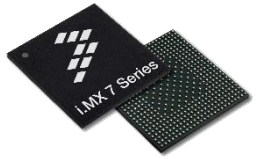
Shared Topology



i.MX 7Dual/Solo Family Target Applications

MOBILE DEVICES

LPDDR2/3
Small Package



- Healthcare / Patient Monitoring
- HMI Control / Security
- Point of Sale
- Printing
- Home Control
- Wearables
- eReaders
- General Embedded Control
- Embedded Board Solutions
- IoT

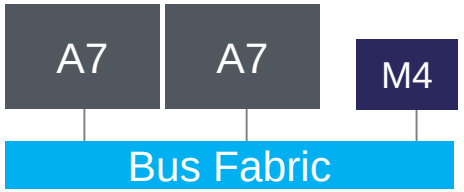
CONNECTED DEVICES

Low Cost DDR3
Larger Pitch Package

i.MX 7 Series Advantages

Advanced Heterogeneous Architecture

- Up to Dual Cortex-A7 @ 1GHz
- Cortex-M4 @ 200MHz
  - Offload Tasks
  - Optimize Power
  - Increase Security



Unmatched Power Efficiency

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- 70 uW/MHz for Cortex-M4
- One third the power consumed in the Low Power suspend mode (250uW) versus i.MX 6

Enabling Flexible High Speed Connectivity

- PCI-e v2.1
- Dual Gbit Ethernet with AVB
- DDR QuadSPI support
- eMMC 5.0

Complete Security Infrastructure

- Secure Boot
- Crypto Hardware Acceleration
- Internal and External Tamper Detection
- Secure RAM
- DPA attack Resistance
- Secure JTAG

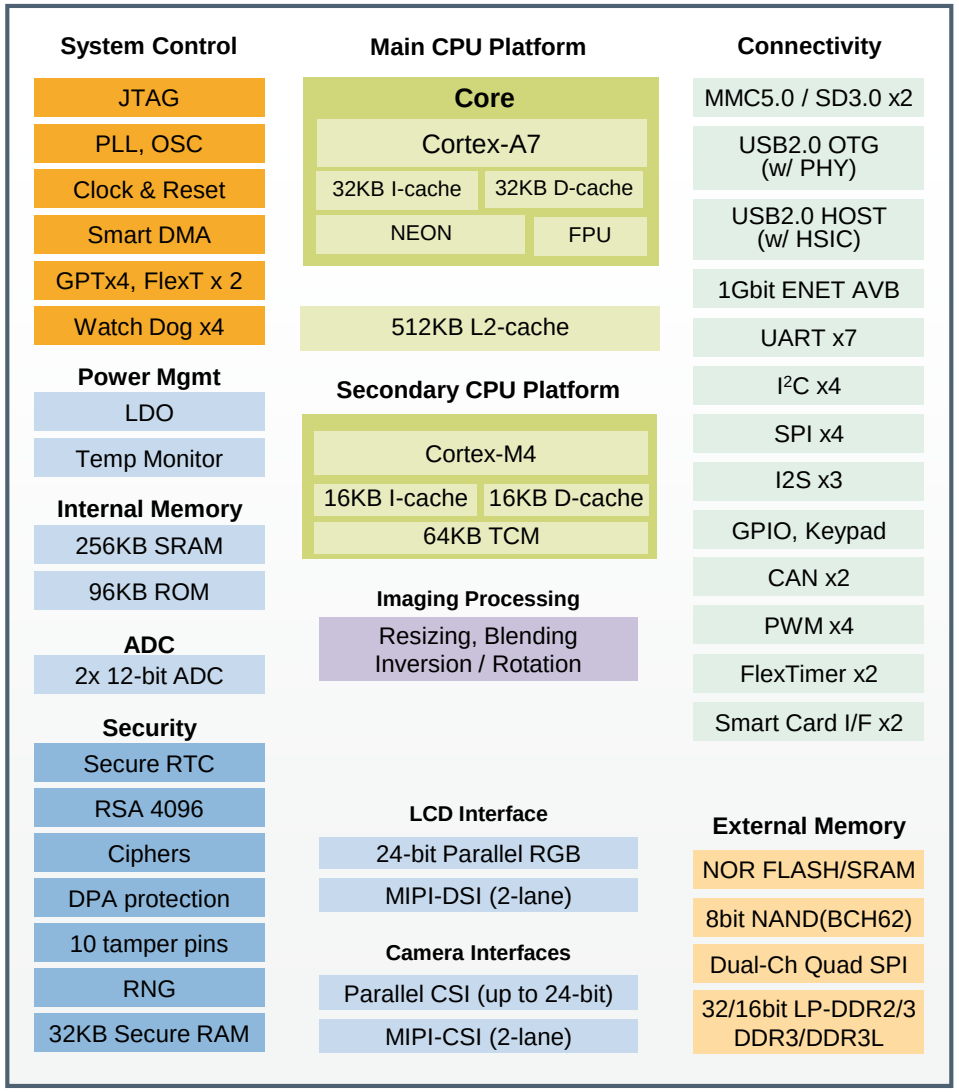
i.MX 7Solo Processor

Specifications:

- **Package:** 19x19 BGA @ 0.75mm pitch BGA
  12x12 BGA @ 0.4mm pitch BGA*
- **Qualification**
  - Consumer (0C to +95C Tj), 5 year operation at 50% duty cycle
  - Industrial (-20C to +105C Tj), 10 year operation at 100% duty cycle

Key Features and Advantages

- **800 MHz AMR Cortex-A7, 32 KB I/D, 512 KB L2 Cache**
- **200 MHz ARM Cortex-M4, 16 KB I/D, 64 KB tightly-coupled memory**
- **Memory Support**
  - 16/32-bit LP-DDR2/3, DDR3/L @ 533 MHz
  - Total of 256 KB on-chip SRAM
  - 2x SDIO3.0/eMMC5.0, 8-bit NAND (BCH62)
- **Display / Camera**
  - 24-bit Parallel LCD and MIPI-DSI (2-lane) display
  - Parallel (up to 24-bit) and MIPI-CSI (2-lane) camera
- **I/O**
  - 1x USB 2.0 OTG w/ PHY + 1xUSB 2.0 HOST/HSIC
  - 1x GigE Ethernet Ports with Audio Video Bridging (AVB)
- **Security module - enabling PCI 4.0 compliance**



* Feature limited (1 ADC, 4 tamper pins)

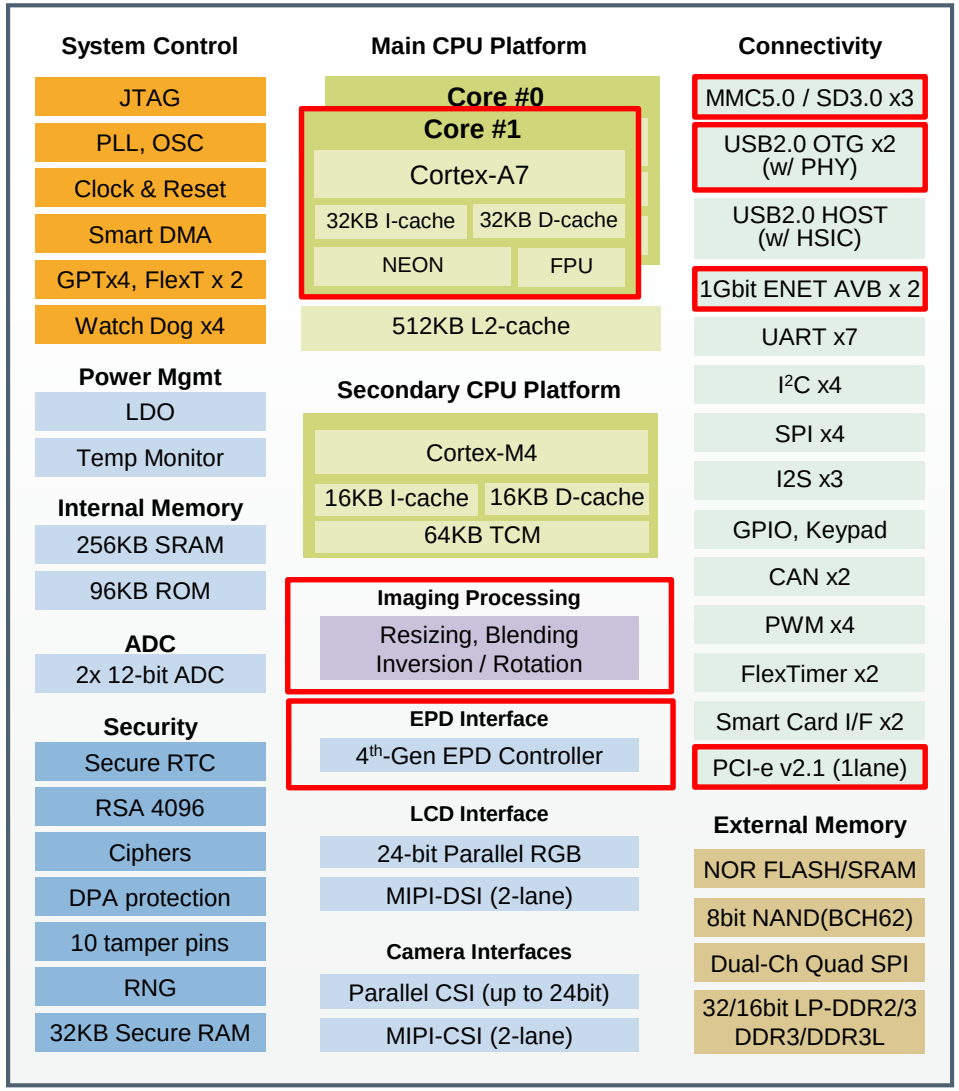
i.MX 7Dual Processor

Specifications:

- **Package:** 19x19 BGA @ 0.75mm pitch BGA
  12x12 BGA @ 0.4mm pitch BGA*
- **Qualification**
  - Consumer (0C to +95C Tj), 5 year operation at 50% duty cycle
  - Industrial (-20C to +105C Tj), 10 year operation at 100% duty cycle

Key Features and Advantages

- **1 GHz, ARM Cortex-A7, 32 KB I/D, 512 KB L2 Cache**
- **200 MHz Cortex M4, 16 KB I/D, 64 KB tightly-coupled memory**
- **Memory Support**
  - 16/32-bit LP-DDR2/3, DDR3/L @ 533 MHz
  - Total of 256 KB on-chip SRAM
  - 3x SDIO3.0/eMMC5.0, 8-bit NAND (BCH62)
- **Display / Camera**
  - 24-bit Parallel LCD and MIPI-DSI (2-lane) display
  - Parallel (up to 24-bit) and MIPI-CSI (2-lane) camera
  - **EPDC (e-ink) display**
- **I/O**
  - 2x USB 2.0 OTG w/ PHY + 1xUSB 2.0 HOST/HSIC
  - 2x GigE Ethernet Ports with Audio Video Bridging (AVB)
  - PCIe 2.1
- **Security module - enabling PCI 4.0 compliance**



Updated from i.MX 7Solo

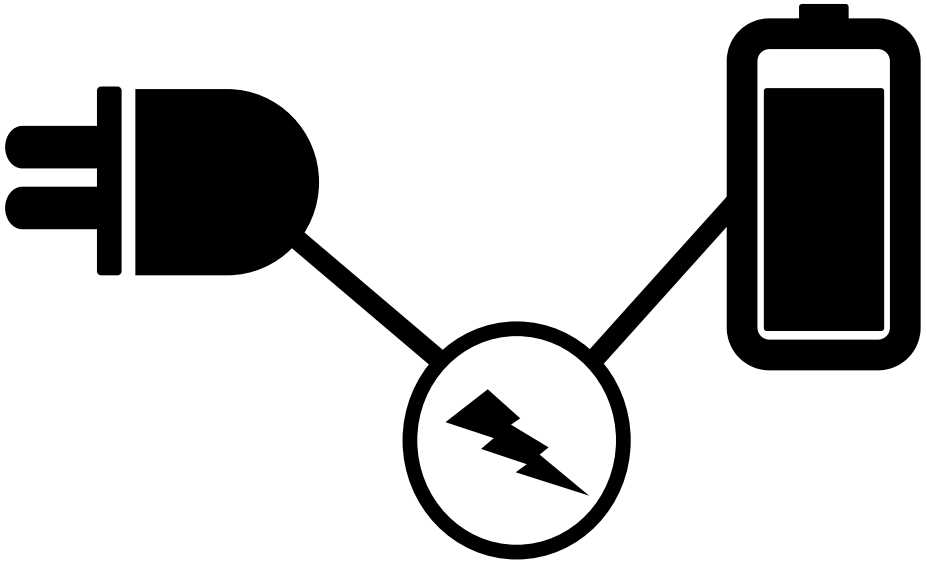
* Feature limited (1 ADC, 4 tamper pins)

i.MX non-GPU/VPU Product Lineup

Feature	i.MX25x	i.MX28x	i.MX 6UL	i.MX 7Solo	i.MX 7Dual
Core	ARM9	ARM9	**Cortex-A7 @ 528 MHz**	Cortex-A7 @**800 MHz**	**Dual** Cortex-A7 @**1GHz**
L2 Cache	-	-	128KB	**512KB**	512KB
RAM	128KB	128KB	128KB	**256KB**	256KB
2nd Core	-	-	-	**Cortex-M4**	Cortex-M4
Flash Interface	MLC/SLC NAND Flash w/ 8-bit RS, NOR Flash	SLC/MLC/Managed NAND Flash w/ 20-bit BCH	SLC/MLC/Managed NAND Flash w/ 40-bit BCH	SLC/MLC/Managed NAND **Flash 60-bit BCH**, 8-bit RS	SLC/MLC/Managed NAND Flash 60-bit BCH, 8-bit RS
DRAM Interface	150 MHz 16-bit DDR2, mDDR, SDRAM	**200 MHz** 16-bit DDR2, LV-DDR2, mDDR	**400 MHz 16-bit DDR3/L, LPDDR2**	**533 MHz 32-bit** DDR3/L, LPDDR2, **LPDDR3**	**533 MHz 32-bit** DDR3/L, LPDDR2, **LPDDR3**
Display	24-bit Parallel-640x480	24-bit Parallel RGB-640x480	24-bit Parallel RGB-**1366x768**	24-bit Parallel RGB-**1920x1080 MIPI-DSI (2 lane) 1.5Gbps**	24-bit Parallel RGB-1920x1080 MIPI-DSI (2 lane) 1.5Gbps **EPDC**
Imaging	1 overlay, alpha blending, panning	**8 overlays**, alpha blending, scaling, rotation, CSC	PXP – Scaling, Alpha Blending, CSC, Dithering	PXP – Scaling, Alpha Blending, CSC, Dithering.	PXP – Scaling, Alpha Blending, CSC, Dithering
Camera Interface	Parallel Camera I/F	-	Parallel Camera I/F	Parallel Camera I/F, **MIPI-CSI**	Parallel Camera I/F, **MIPI-CSI**
CAN	x2	x2	x2	x2	x2
Ethernet	Single 10/100	Dual 10/100 **and L2 Switch**	Dual 10/100	Single **1Gb (AVB)**	**Dual** 1Gb (AVB)
Audio	I2S	I2S, S/PDIF	I2S, S/PDIF	**MQS**, I2S	MQS, I2S
USB	HS port (Host/Device) HS PHY x1,HS Host with FS PHY x1	HS port (Host/Device) with PHY x1, HS port Host with PHY x1	OTG with PHY x2	OTG with PHY x1 **HOST with HSIC**	OTG with PHY **x2** Host with HSIC
SIM	x2	-	x2	x2	x2
PCIe	-	-	-	-	**Yes**
Security	Tamper Detection, RNG	HAB4, PRNG	**Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins, OTF**	Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins,	Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins,
Power	External	**Integrated PMIC w/ Charger**	Analog LDOs	Analog LDOs	Analog LDOs

BOM Advantage

Performance Advantage

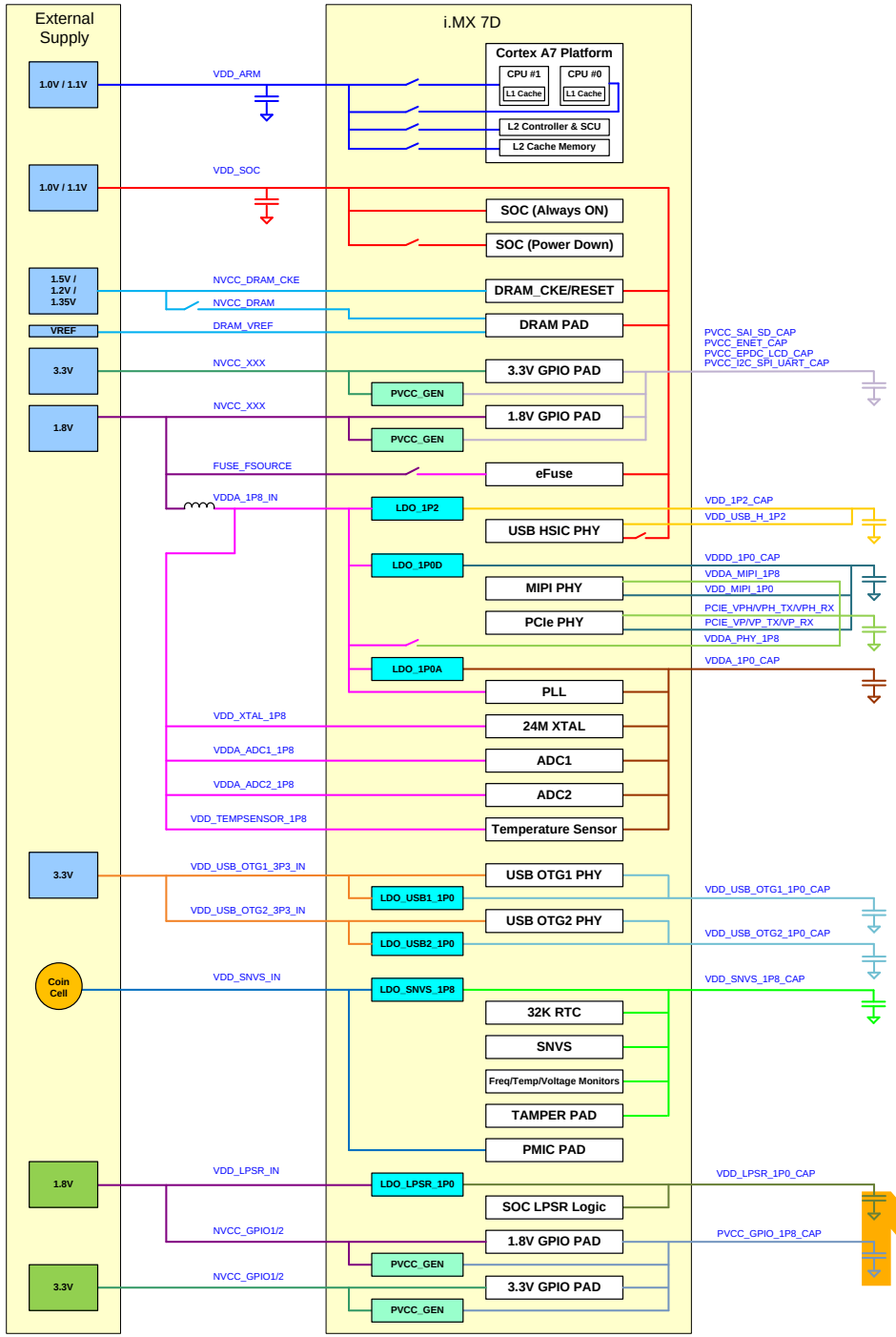


i.MX 7: Power Architecture

i.MX 7: Power Diagram

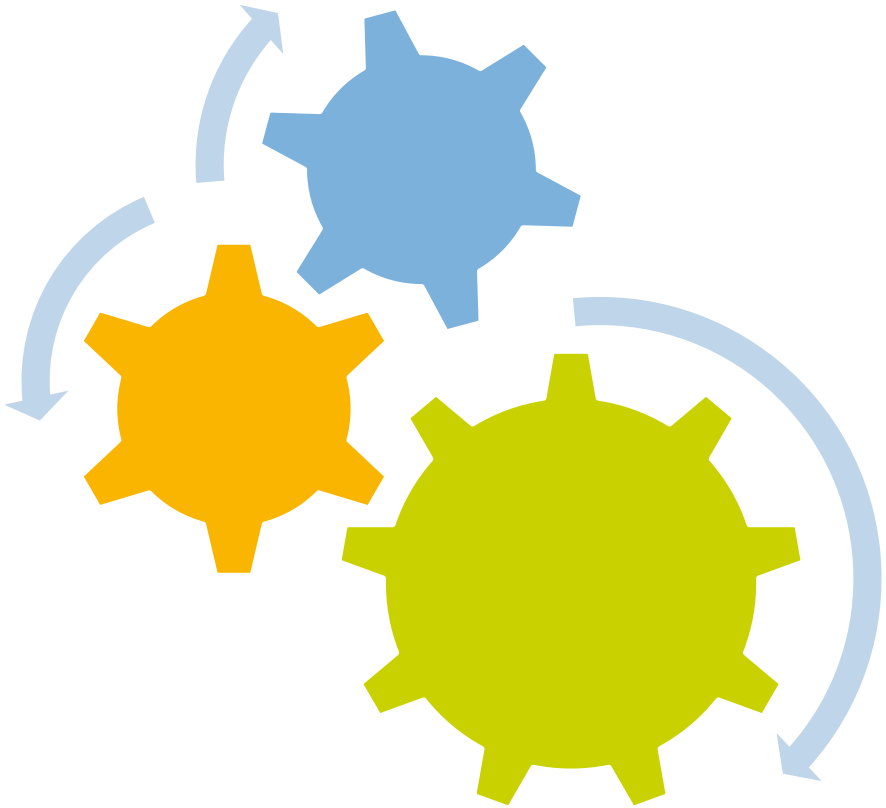
Full configuration

- **External Supply**
  - 1.0V **ARM CPU**
  - 1.0V **SOC**
  - 1.2/1.5/1.35 **DRAM IO**
  - 1.8V **Analog**
  - 1.8V / 3.3V **I/O**
  - 3.3V **USB**
  - 1.8V **LPSR**
  - 1.8V / 3.3V **IO in LPSR**
  - 2.8V – 3.6V **SNVS / Coin Cell**
- **Integrated LDO**
  - **Analog Modules (bypass allowed)**
  - **MIPI PHY and PCIe PHY.**
  - **USB HSIC PHY.**
  - **USB PHY1.**
  - **USB PHY2.**
  - **LPSR logic.**
  - **SNVS and 32K RTC.**



Low Power Mode Definition

System Idle	• CPU can automatically enter this mode when no thread running • CPU clock gated and have its state retained so the interrupt response can be very short • All the peripherals can still keep working and most of PLL are shut off • DRAM enters auto-refresh mode when there is no access
Low Power Idle	• Lower power than System Idle mode with longer exit time • CPU power gated and all PLL are shut off • All high-speed peripherals are power gated, low speed peripherals are running at low frequency • DRAM put into self-refresh by software
Suspend	• Much power saving mode with longer exit time • CPU power gated and all clock are off except 32KHz RTC • All peripherals are power gated • DRAM put into self-refresh by software
LPSR	• The new kind of power mode • An extension of SNVS mode with 16 GPIO in low power state retention mode • VDD_LPSR/NVCC_GPIO1/2 remains on besides VDD_SNVS • Keep CKE pad in correct state to hold DRAM device in self-refresh mode
SNVS	• All power supply are shut off except VDD_SNVS • All SOC digital logic, analog module are shut off only except SNVS domain • 32KHz RTC and Tamper Detection are alive



i.MX 7: Enablement

Enablement

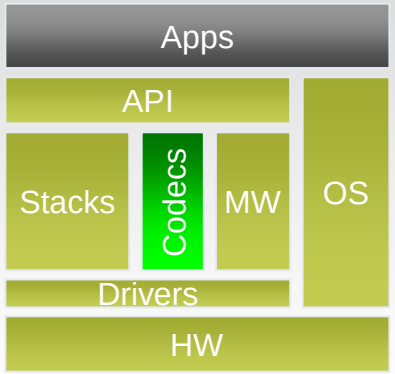
Hardware Platform

PDKs, EVKs, SABRE, Quick Start Board

- Ease of Use – BSP and demo images, development environment build demonstration, video tutorials, schematic and layout, documentation
- Ranging from $149 development board to $999 full reference platform.

Full Hardware evaluation and Development Platforms

+ Software



- Full-featured, scalable, optimized and proven OS – Linux, Windows, Android
- Software codecs for video, audio, graphics and communications.
- Product-worthy software for reference platforms and product development

Complete software package to streamline software development

+ Ecosystem

- Tool chains
- Software – RTOS, OS, codecs, middleware/applications
- Hardware – embedded board solutions
- Design services
- System integrators
- Training

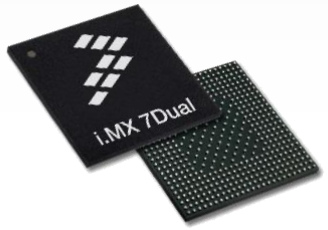
Technology alliances for building smarter, better

www.imxcommunity.org

NXP Hardware Solutions

i.MX7

- **1 GHz** ARM® Cortex™-A7
  - **NEON™ coprocessor**
- ARM® Cortex™-M4,
- **Electronic Paper Display (EPD)** in addition to LCD.
- Targeting a broad range of applications including many **low power**, **portable** consumer devices



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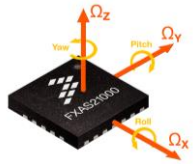
PMIC

- Integration of Freescale's PMIC chip set with i.MX processor for optimization of power efficiency and software/hardware integration
- One-stop customer service and support during development phase to enable the design process

+

Sensors

- MEMS gyroscopes for reliable sensing and measuring
- Magnetometers: measuring the magnitude and direction of magnetic fields
- Pressure Sensing Devices, composed of single silicon, piezoresistive devices



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i.MX7 SABRE Board

Development platform:

- Single-board evaluation kit
- Linux® and Android™ Board Support Packages are available out of box and updates through Freescale.com

A Single Solution for Streamlined Performance

i.MX 7: SABRE Platform Planned Key Features

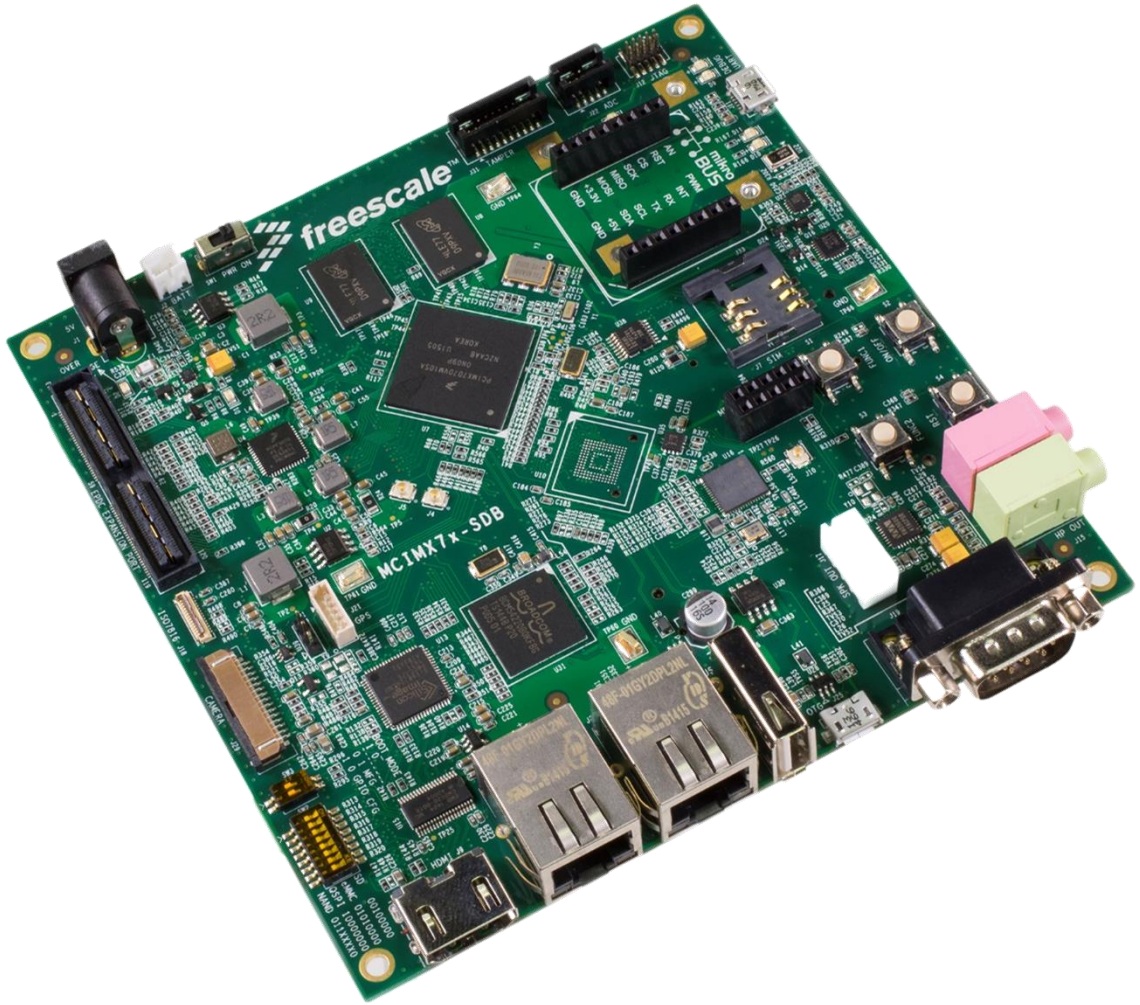
Processor
- Freescale i.MX 7Dual
  - Dual Cortex™-A7 @1GHz
  - 512KB L2 Cache
- Freescale PF3000 PMIC

Memory
- 1 GB DDR3
- eMMC5.0 footprint
- QuadSPI Flash
- SD/MMC socket
- NAND footprint

Display/Camera Connectors
- HDMI
- Parallel LCD
- MIPI-DSI
- Electronic Paper Display
- MIPI-CSI (camera)

Wireless
- Wifi (802.11ac) onboard
- BT4.0 / BLE onboard

Audio
- Audio HP Jack
- External speaker connection

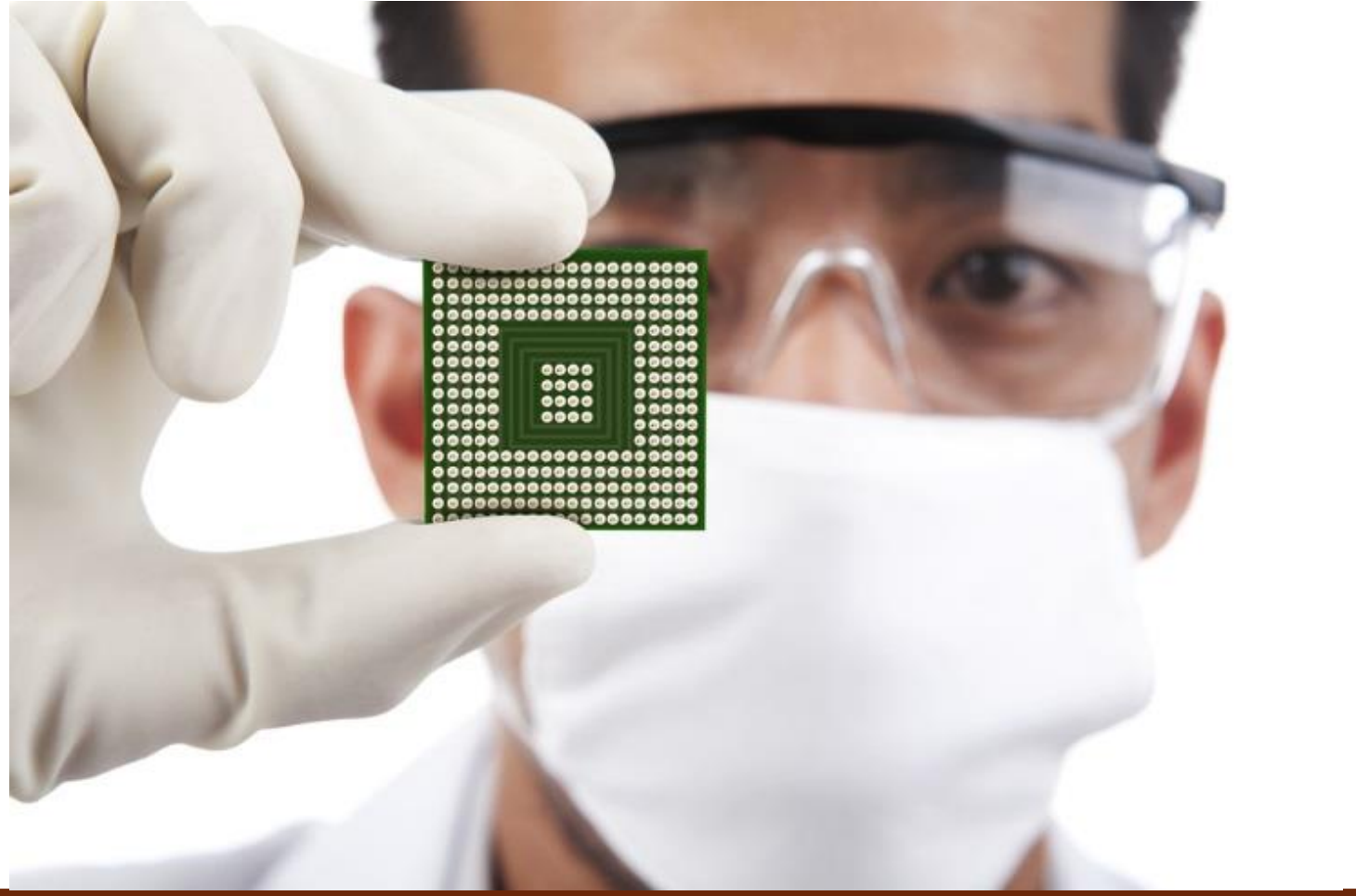


Connectivity
- USB Host connectors
- microUSB OTG connector
- ETH (1Gbit) Receptacle
- ETH (10/100) Receptacle
- Full Mini PCIe socket
- SIM Card slot
- CAN (DB-9)
- GPIO
- MFi Module support
- MikroBus expander

Debug
- JTAG connector
- UART via USB

Sensors
- **FXOS8700** three-axis digital accelerometer/Magnetometer
- **MPL3115A2R** Altimeter/Pressure sensor
- **FXAS21000** three-axis digital Gyroscope

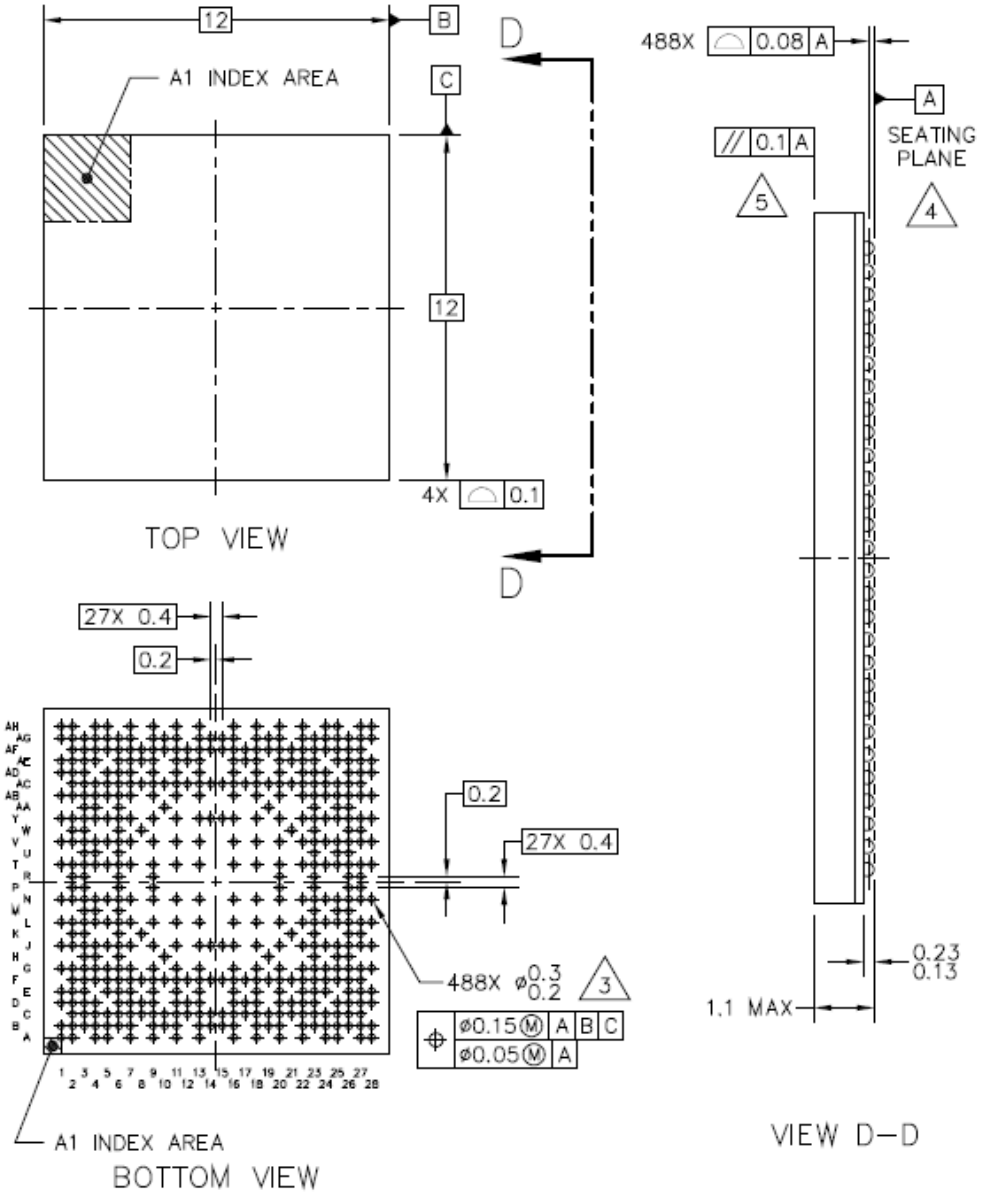
Tools & OS Support
- Linux®
- Android™
- FreeRTOS



i.MX 7 Package Options

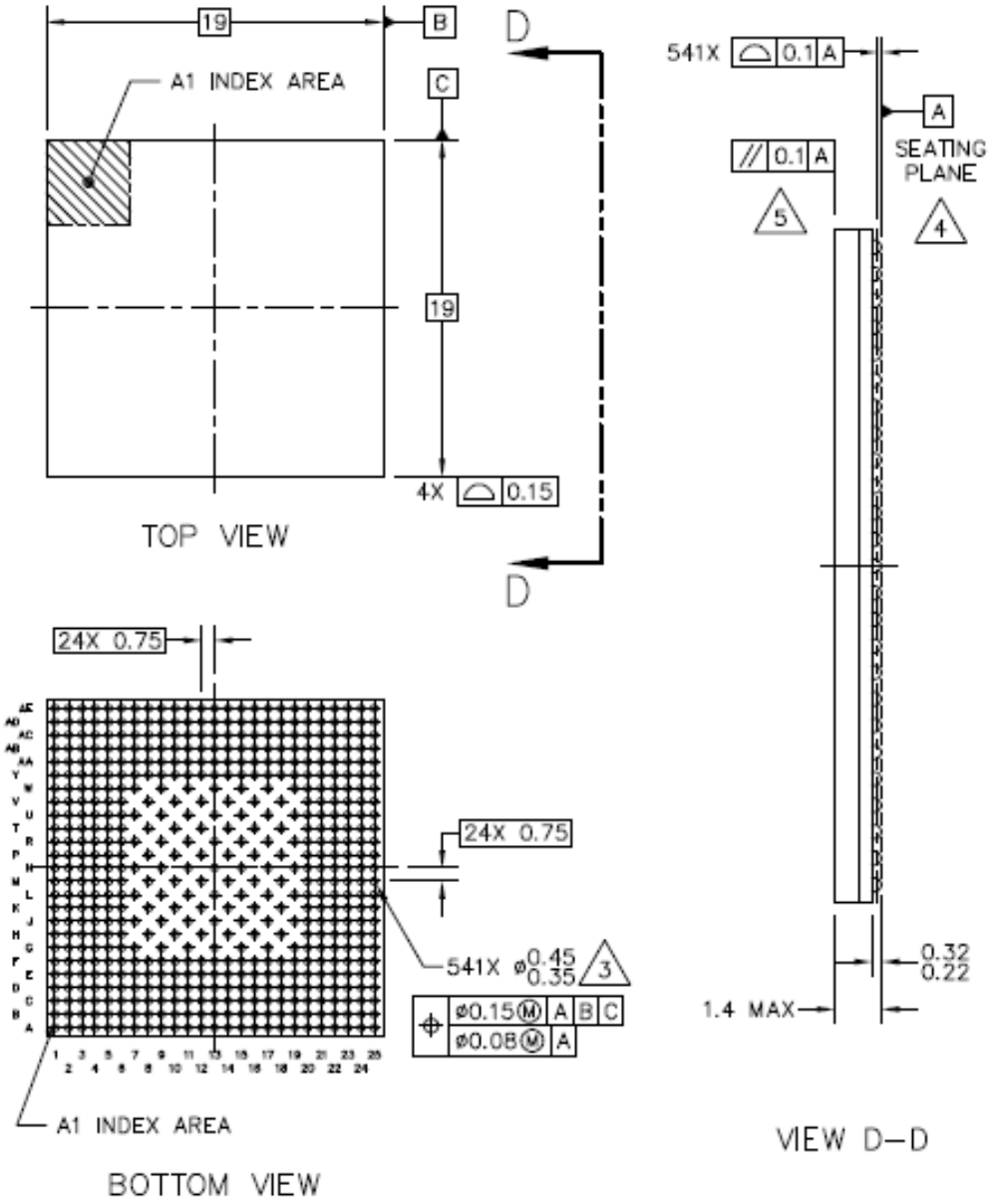
i.MX 7: 12mm x 12mm, .4mm Pitch

- Targeted at small form factor designs
- LPDDR3 escape routing optimized
- 6-layer PCB capable with HDI



i.MX 7: 19mm x 19mm, .75mm Pitch

- Targeted at non-HDI designs
- DDR3/L escape routing optimized
- 6-layer PCB capable,



I.MX 6SLL

i.MX 6 Series: Supreme Scalability and Flexibility
Leverage One Design into Diverse Product Portfolio

Scalable series of **Eleven** ARM-based SoC Families

i.MX 6ULL	i.MX 6UltraLite	i.MX 6SoloLite	i.MX 6SoloLite	i.MX 6SoloX	i.MX 6Solo	i.MX 6DualLite	i.MX 6Dual	i.MX 6DualPlus	i.MX 6Quad	i.MX 6QuadPlus
i.MX 6 ULL Family	i.MX 6UltraLite Family	i.MX 6 SLL Family	i.MX 6SoloLite Family	i.MX 6SoloX Family	i.MX 6Solo Family	i.MX 6DualLite Family	i.MX 6Dual Family	i.MX 6DualPlus Family	i.MX 6Quad Family	i.MX 6QuadPlus Family

Pin-to-pin Compatible

Pin-to-pin Compatible

Pin-to-pin Compatible

Software Compatible

Expanded series for performance, power efficiency and lower BOM

i.MX 6SLL Applications Processor

► Specifications

- **Process:** SMIC 40LL
- **Core Voltage:** 1.1V
- **Package:** 13x13 MAPBGA, 0.5mm pitch
- **Temperature:** 0C to 95C (Tj)
- **Qual Tiers:** Commercial

► Key Features and Advantages

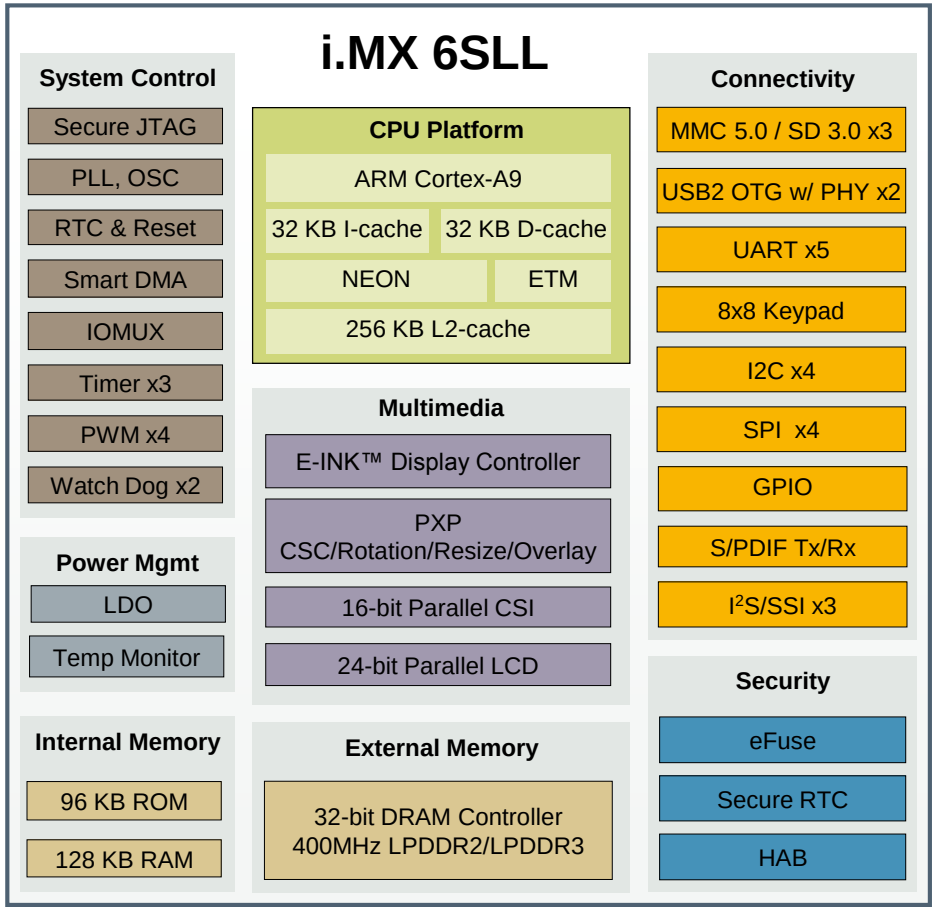
- ARM Cortex-A9 @ 1GHz, 256 KB L2 cache
- 32-bit LPDDR2/LPDDR3
- E-INK™ Display Controller
- 24-bit Parallel LCD Display
- 8/10/16-bit Parallel Camera Sensor Interface
- 3x MMC 5.0/SD 3.0/SDIO Port
- Audio: 3x I2S/SSI, 1x S/PDIF Tx/Rx
- Partial PMU Integration
- HAB Support

► Enablement

- Linux BSP from Freescale
- Android*

► Compatibility

- Pin-to-pin compatible with i.MX6SL*
- SW compatible with i.MX6SL*



*There may be small differences in IO and performance due to fab changes. There is potential minor system or SW tweaks are needed
*Separate cost/schedule/agreement on Android.

Feature Summary (1/2)

	i.MX 6SoloLite	i.MX 6ULL	i.MX 6SLL	i.MX 7Dual
Primary CPU	Cortex-A9 x1 1GHz, 2500 DMIPS	Cortex-A7 x1 528MHz, 1000 DMIPS	Cortex-A9 x1 1GHz, 2500 DMIPS	Cortex-A7 x2 1GHz, 3800 DMPIS
Cache	32KB/32KB L1 256KB L2	32KB/32KB L1 128KB L2	32KB/32KB L1 256KB L2	32KB/32KB L1 512KB L2
Secondary CPU	-	-	-	Cortex-M4, 266MHz
On-Chip RAM	128KB	128KB	128KB	160KB
DRAM	LPDDR2 / DDR3 400MHz, 32-bit	LPDDR2 / DDR3 400MHz, 16-bit	LPDDR2 / LPDDR3 400MHz, 32-bit	LPDDR2 / LPDDR3 / DDR3, 533MHz, 32-bit
SD/MMC	SD/eMMC x4 SD3.0, eMMC4.4	SD/eMMC x2 SD3.0, eMMC4.5	SD/eMMC x3 SD3.0, eMMC5.0	SD/eMMC x3 SD3.0, eMMC5.0
Raw NAND	-	8-bit, 40-bit ECC	-	8-bit, 62-bit ECC
QSPI	-	Dual Channel QSPI	-	Dual Channel QSPI
Parallel NOR	8/16-bit	8/16-bit	-	8/16-bit
USB	2x USB2.0 OTG w/PHY 1x HSIC	2x USB2.0 OTG w/PHY	2x USB2.0 OTG w/PHY	2x USB2.0 OTG w/PHY 1x HSIC
Ethernet	1x 10/100Mbps	2x 10/100Mpbs	-	2x 1Gbps
PCIe	-	-	-	PCIe 2.0, 1-lane

Feature Summary (2/2)

	i.MX 6SoloLite	i.MX 6ULL	i.MX 6SLL	i.MX 7Dual
EPD Display	8/16-bit Panel 2332x1650@106Hz	8/16-bit Panel 2048x1536@106Hz	8/16-bit Panel 2332x1650@106Hz	8/16-bit Panel 2332x1650@106Hz
LCD Display	24-bit Parallel RGB	24-bit Parallel RGB	24-bit Parallel RGB	24-bit Parallel RGB MIPI DSI 2-lane
Image Processing	CSC, Resize, Rotation, Alpha-Blending	CSC, Resize, Rotation, Alpha-Blending, Dithering	CSC, Resize, Rotation, Alpha-Blending, Dithering	CSC, Resize, Rotation, Alpha-Blending, Dithering
EPD Waveform Processing	Gen-I	Gen-II (REAGL/-D) Single Engine	Gen-II (REAGL/-D) Single Engine	Gen-II (REAGL/-D) Dual Engine
Camera Input	16-bit Parallel	24-bit Parallel	24-bit Parallel	24-bit Parallel MIPI CSI 2-lane
Audio	I2S x3 SPDIF TX/RX	I2S x3 SPDIF TX/RX ESAI x1, ASRC	I2S x3 SPDIF TX/RX	I2S x3
12-bit ADC	x2	x2	x2	x2
Touch Controller	-	4/5-wire resistive touch	-	-
UART, SPI, I2C	5, 4, 3	8, 4, 4	5, 4, 3	7, 4, 4
Package	13x13mm, 0.5mm pitch	9x9mm, 0.5mm pitch	13x13mm, 0.5mm pitch	12x12mm, 0.4mm pitch

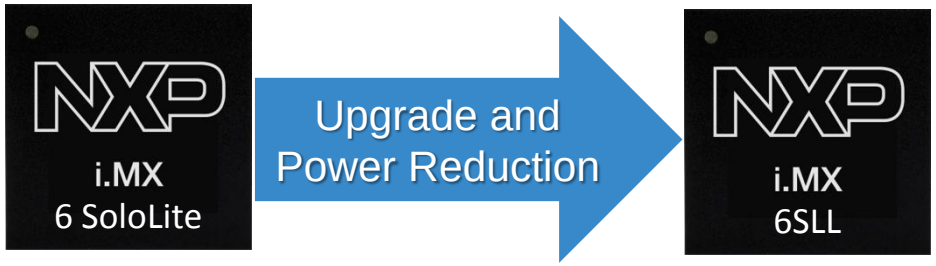
i.MX 6SLL vs i.MX6SL

Red indicates the feature removed from i.MX6SL
Green indicates the feature added on i.MX6SLL

Feature	i.MX 6SL*	i.MX 6SLL
Core	ARM Cortex-A9	ARM Cortex-A9
Speed	1GHz	1GHz
Cache	32 KB-I, 32KB-D 256KB L2	32 KB-I, 32KB-D 256KB L2
OCRAM	128 KB	128 KB
DRAM	32-bit LP-DDR2, DDR3/DDR3L	32-bit LPDDR2, LPDDR3
eMMC	eMMC4.4	eMMC5.0
SD/eMMC Port	4	3
Parallel Nor/EBI	Yes	None
Ethernet	10/100 MB x 1	None
USB with PHY	OTG, HS/FS x 2	OTG, HS/FS x 2
USB with HSIC	1	None
Security	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot	TRNG, Crypto Engine (AES/TDES/SHA), Secure Boot
eFuse	2K-bit	2K-bit
E-INK Display	EPDC (8-bit / 16-bit)	EPDC (8-bit)
SiPix Display	SPDC	None
Image Processing	PXP	PXP
Graphic	GPU2D, OpenVG	None
CSI	16-bit Parallel CSI	16-bit Parallel CSI
LCD	24-bit Parallel LCD	24-bit Parallel LCD
UART	5	5
IIC	4	4
SPI	4	4
I2S/SSI	3	3
S/PDIF	1	1
Timer	3	3
PWM	4	4
Keyboard (8x8)	Yes	Yes
Digital LDO	ARM/SOC/PU	None
Analog LDO	1.1V/2.5V	1.1V/2.5V
Temperature	0C to 95C (Tj)	0C to 95C (Tj)

*Part Number: MCIMX6L8DVN10AA

i.MX 6SLL Key Changes



i.MX 6SLL

- ARM Cortex-A9 @ 800MHz/ 1GHz
- 256 KB L2 cache
- 32-bit LPDDR2/LPDDR3
- Linux

IP Changes:

- Latest ARM Cortex A9 revision
- Support LPDDR3, remove DDR3
- Latest EPDC / PXP
- eMMC5.0
- Remove IPs including GPU, ENET

Power Reduction

- Remove digital LDO
- Support low power run
- Support megamix power down (high-speed IP modules)
- 50% lower on suspend power

Design updates

- PINMUX
- Ball Map
- Memory Map
- IRQ assignment
- Less boot device

Memory Map

Start Address	End Address	i.MX6SL Region	i.MX6SLL Region	Size
00E0_0000	00EF_FFFF	Reserved	GPV_3	1MB
020E_8000	020E_BFFF	SiPix IP	CSI	16KB
020E_4000	020E_7FFF	CSI	IOMUXC_GPR	16KB
020B_0000	020B_3FFF	Reserved	GPIO6	16KB
0209_4000	0209_7FFF	QoSC	Reserved	16KB
0209_0000	0209_3FFF	AXI_MON	Reserved	16KB
0201_8000	0201_BFFF	UART5	Reserved	16KB
021F_4000	021F_7FFF	Reserved	UART5	16KB
021C_8000	021C_BFFF	PERFMON2	IOMUXC_SNVS	16KB
021C_4000	021C_7FFF	PERFMON1	IOMUXC_GPR_SNVS	16KB
021B_8000	021B_BFFF	WEIM Registers	Reserved	16KB
0219_C000	0219_FFFF	uSDHC4	Reserved	16KB
0218_C000	0218_FFFF	MSHC	Reserved	16KB
0218_8000	0218_BFFF	FEC	Reserved	16KB
0220_4000	0220_7FFF	GC355 Registers	Reserved	16KB
0220_0000	0220_3FFF	GC320 Registers	Reserved	16KB
0800_0000	0FFF_FFFF	WEIM	Reserved	128MB

Interrupt

IRQ	i.MX6SL		i.MX6SLL	
	Module	Signal	Module	Signal
3	mshc	ipi_memstick_xint	Reserved	
6	tcon	INTERRUPT_TCON	Reserved	
10	gpu2d	gc320_xaq2_intr	Reserved	
11	gpu2d	gc355_V2D_xaq2_intr	Reserved	
14	weim	~ipi_weim_int_b	Reserved	
25	usdhc4	~ipi_usdhc_irq_b	Reserved	
40	usb	ipi_int_uh	anatop	irq_ana5
41	Reserved		anatop	irq_ana6

Boot Device

	i.MX 6SL	i.MX 6SLL
SD	Supported	Supported
MMC	Supported	Supported
Parallel NOR FLASH	Supported	-
OneNAND	Supported	-
Serial NOR FLASH (I2C)	Supported	Supported
Serial NOR FLASH (SPI)	Supported	Supported
USB	Supported	Supported

i.MX 6SLL - Power Optimization

Power Rail	i.MX 6SL			i.MX 6SLL			Reduction	
	Voltage	Current	Power	Voltage	Current	Power	Power	Ratio
	(V)	(mA)	(mW)	(V)	(mA)	(mW)	(mW)	%
VDD_ARM_IN	0	0	0	0	0	0	-	-
VDD_SOC_IN	0.9	0.75	0.675	0.9	0.5	0.45	0.225	18%
VDD_PU_IN	0.9	0.1	0.09	-	-	-	0.09	7%
VDD_HIGH_IN	3	0.15	0.45	3.0	0.03	0.09	0.36	28%
VDD_SNVS_IN	3	0.015	0.045	3.0	0.015	0.045	-	-
Total			1.26			0.585	0.675	53%

- Power reduction on both analog & digital
- Power gate high speed digital logic to reduce leakage
- Strict control the LVT usage during physical implementation

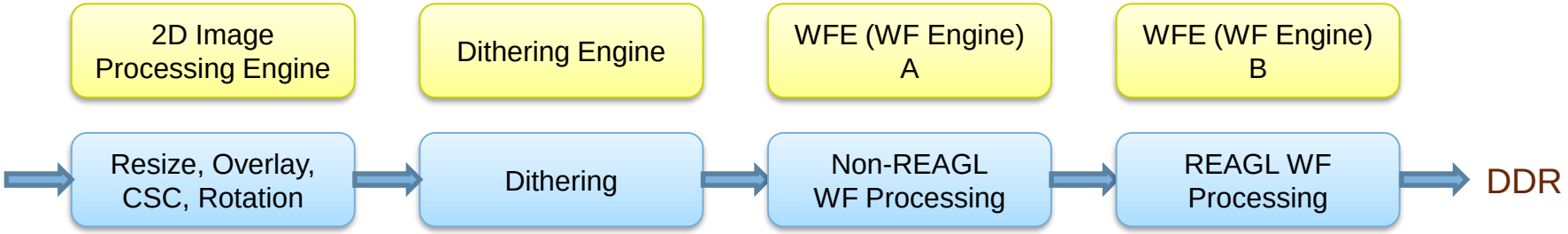
EPD Feature Comparisons

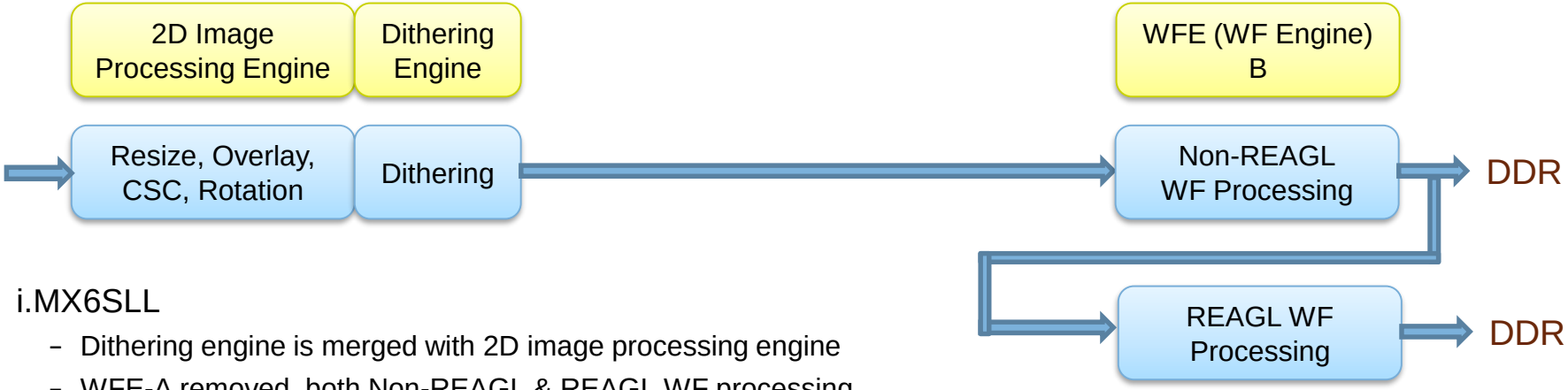
Feature	i.MX 6SL	i.MX 6SLL/6ULL	i.MX 7D
Max Resolution*	2332x1650@106Hz	2332x1650@106Hz	2332x1650@106Hz
Pixel Depth	Up to 5-bit	Up to 5-bit	Up to 5-bit
Panel Interface	8/16-bit	8/16-bit	8/16-bit
Dual Scan	Yes	No	Yes
LUT Entry	64 or 16	64	64
LUT Index	14-bit	**16-bit**	**16-bit**
LUT Memory	64KB	64KB	**128KB**
Histogram Statistic based on Update Pixel	Yes	Yes	Yes
Collision Detection	Yes	Yes	Yes
Dry-Run Mode For Collision Detection	Yes	Yes	Yes
HW Dithering Engine (Ordered Dithering)	No	**Yes**	**Yes**
HW Dithering Engine (Floyd-Steinberg or Atkinson)	No	No	**Yes**
Per-Pixel Update Support	No	**Yes**	**Yes**
E-INK Gen-I Waveform Processing in HW	Yes	Yes	Yes
E-INK Gen-II Waveform Processing (REAGL/-D) in HW	No	**Yes**	**Yes**
Programmable Engine for Waveform Processing	No	**Single Engine**	**Dual Engine**
Cortex M4 for Waveform Processing	No	No	**Yes**

*Max resolution on ULL is limited to 2048x1536 because of 16-bit DRAM

PXP Processing Flow

i.MX7D – Four separate processing engines working in pipeline





i.MX6SLL

- Dithering engine is merged with 2D image processing engine
- WFE-A removed, both Non-REAGL & REAGL WF processing done by WFE-B

Waveform Processing Time

		i.MX 7D				i.MX 6SLL			
Resolution		Non-Reagl/-D Processing Time (ms)		Reagl/-D Processing Time (ms)		Non-Reagl/-D Processing Time (ms)		Reagl/-D Processing Time (ms)	
Horizontal	Vertical	Single Pass	Two Pass	Single Pass	Two Pass	Single Pass	Two Pass	Single Pass	Two Pass
1024	758	5	10	8	16	6	13	-	19
1448	1072	10	21	16	31	13	26	-	39
1728	1296	15	30	22	45	19	37	-	56
2880	2160	41	83	62	124	52	104	-	156

- PXP runs at 333MHz in i.MX7D while 266MHz in i.MX6SLL, so the processing time in i.MX6SLL is 25% longer.
- The single pass flow for REAG/-D is not supported in i.MX6SLL because it only has one waveform engine.

SECURE CONNECTIONS
FOR A SMARTER WORLD