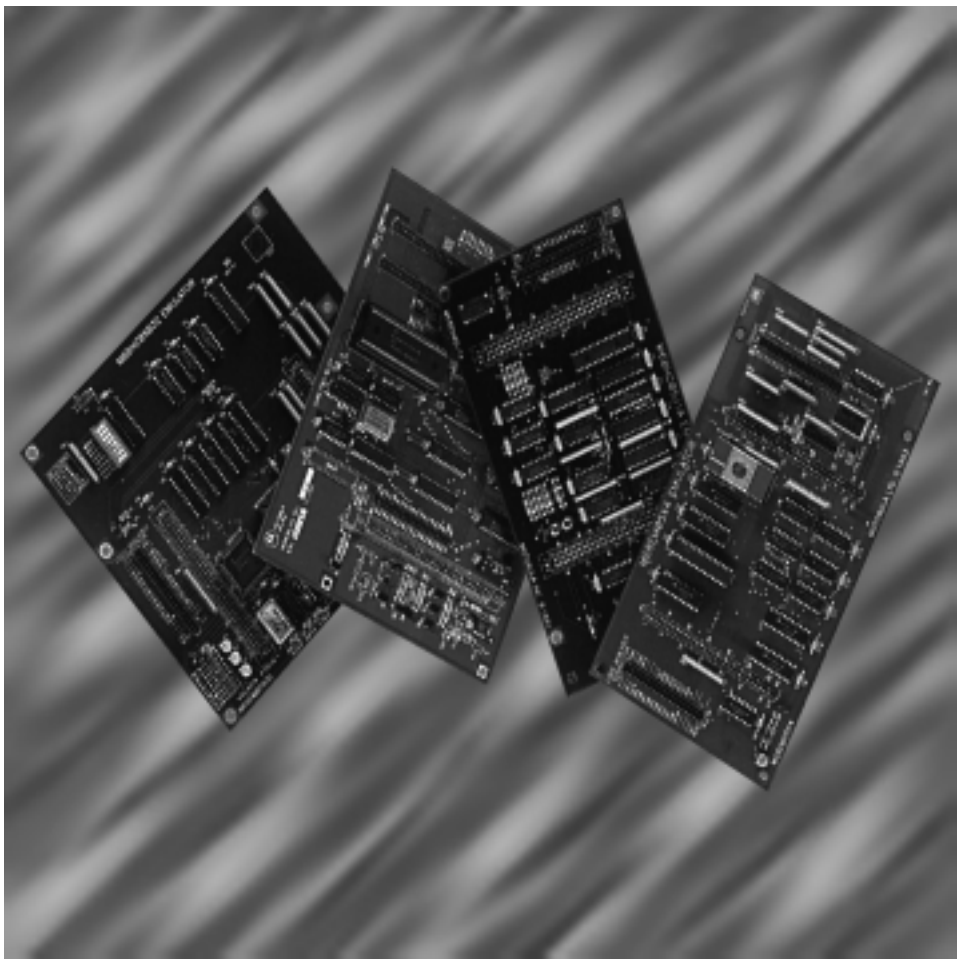
M68EML08AB32UM/D
REV. 1

M68EML08AB32

EMULATION MODULE
USER'S MANUAL



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Section 1. General Description

1.1 Contents

1.2 Introduction

This user's manual explains connection, configuration, and operation information specific to the M68EML08AB32 emulator module (AB32EM). The AB32EM lets you emulate and debug target systems based on the MC68HC08AB16A and MC68HC908AB32 microcontroller units:

This section describes Motorola's two development systems that use the AB32EM, and it explains the AB32EM's layout.

1.3 Development Systems

The AB32EM can be part of two Motorola development systems:

- MMDS0508 Motorola Modular Development System (MMDS)
- MMEVS0508 Motorola Modular Evaluation System (MMEVS)

1.3.1 Motorola Modular Development System (MMDS)

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows. The unit's integrated design environment includes an editor, an assembler, user interface, and source-level debug.

A complete MMDS consists of:

- Station module — The metal MMDS enclosure containing the control board and the internal power supply
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of microcontroller units
- Two logic clip cable assemblies — Twisted-pair cables that connect the station module to the target system, a test fixture, a clock, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies.
- 9-lead RS-232 serial cable — Cable that connects the station module to the host computer RS-232 port
- 9- to 25-pin adapter — A molded assembly that connects the 9-pin cable to a 25-pin serial port
- System software — MCUez™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMDS documentation — *MMDS Operations Manual*, Motorola document order number MMDS0508OM/D; the MCUez software manual, included with the MCUez software package; a system software manual, included with the P&E Microcomputer System, Inc.'s MMDS0508 software package; and this EM user's manual (this manual)

MMDS baud rates are selected by the user at 2400, 4800, 9600, 19,200, 38,400, or 57,600.

As mentioned, the AB32EM gives the MMDS the ability to emulate target systems based on MC68HC08AB16A and MC68HC908AB32 microcontroller units. By substituting a different EM, MMDS can be enabled to emulate target

systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.3.2 Motorola Modular Evaluation System (MMEVS)

An MMEVS is an economical, two-board tool for designing, debugging, and evaluating target systems based on MC68HC05 or MC68HC08 MCUs.

A complete MMEVS consists of:

- Platform board (PFB) — The bottom board, which supports the emulator module; has connectors for power and for a terminal or host computer
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs; fits onto the PFB
- RS-232 serial cable — A separately purchased cable that connects the PFB to the host computer RS-232 port
- System software — MCUez™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMEVS documentation — *MMEVS Operations Manual*, Motorola document order number MMEVSOM/D; the MCUez software manual, included with the MCUez software package; a system software manual, included with the P&E Microcomputer System, Inc.'s MMDS0508 software package; and this emulator user's manual

An MMEVS features automatic selection of the communication baud rate from these choices: 2400, 4800, 9600, 19,200, 38,400, or 57,600.

With a AB32EM, the MMEVS emulates target systems based on MC68HC908AB32 MCUs. By substituting a different EM, the MMEVS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

Section 2. Configuration and Operation explains how to configure and use the AB32EM as part of an MMDS or MMEVS system.

1.4 EM Layout

Figure 1-1 shows the layout of the AB32EM.

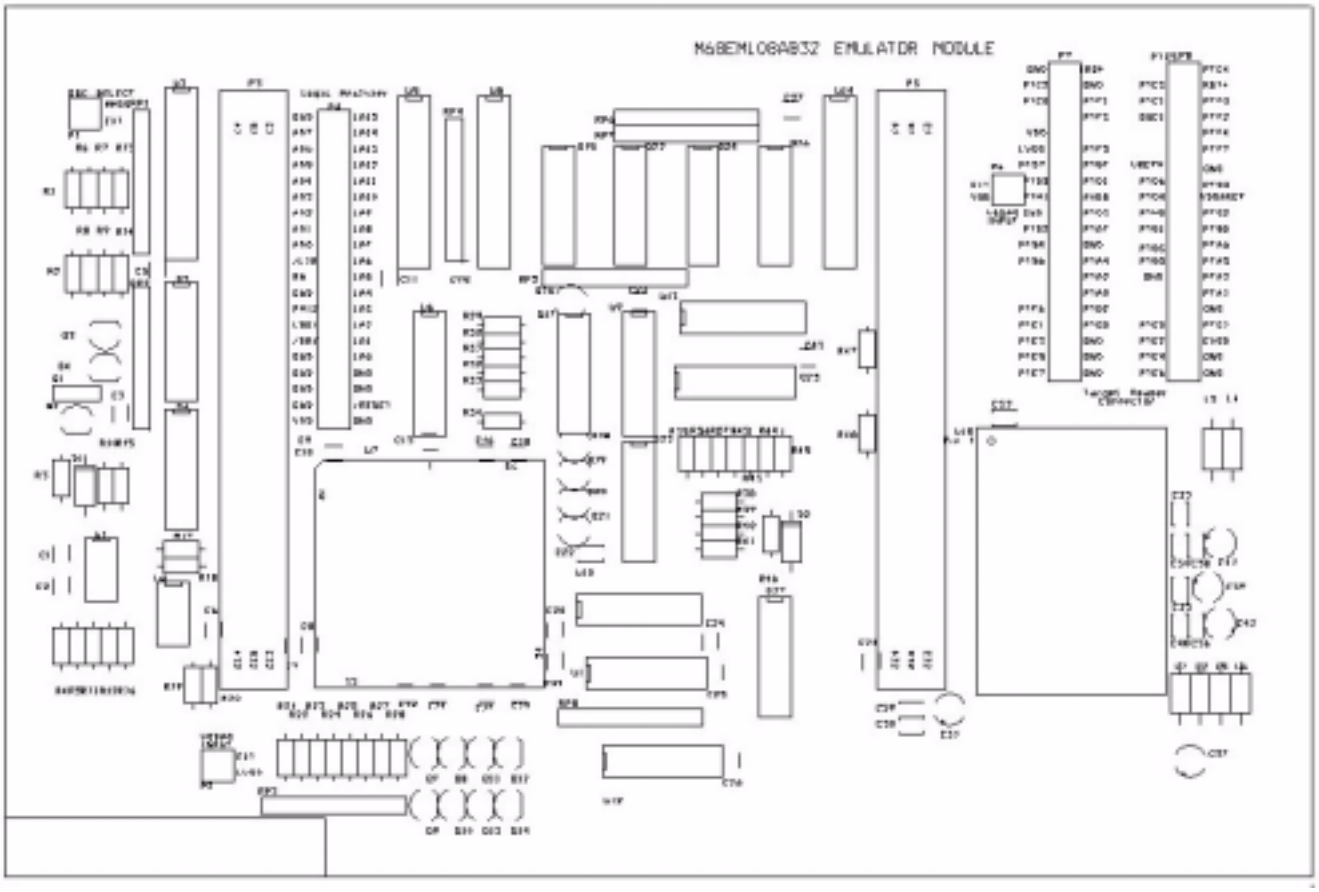


Figure 1-1. M68EML08AB32 Emulator Module

The main elements of the AB32EM are:

- DIN connectors P3 and P5 — Connect the EM to the MMDS control board or the MMEVS platform board
- Connector P4 — Permits connection to a logic analyzer
- Jumper header P2 and P6 — Select the analog voltage supply for the ADC module of the MC68HC908AB32.
- Jumper header P1 — Selects the MCU clock source

- Connectors P7 and P8 — Customer-specific interfaces to the target system

The AB32EM requires a user-supplied 80-lead target cable and target head adapter to connect the target system to connectors P7 and P8.

1.5 Specifications

Table 1-1 lists AB32EM specifications.

Table 1-1. M68EML08AB32 Specifications

Characteristics	Specifications
MCU extension I/O ports	HCMOS compatible
Operating temperature	0° to 40°C
Storage temperature	–40° to +85°C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 V dc and +12 V dc (charge pump), provided from the MMDS control board or MMEVS platform board
Dimensions	8.2 x 5.5 inches; 207 x 140 mm
Weight	7.62 ounces; 216 grams

General Description

Section 2. Configuration and Operation

2.1 Contents

2.2 Introduction

This section explains configuration and operation of the AB32EM when it is installed in an MMDS (Motorola modular development system) or MMEVS (Motorola modular evaluation system). For other parts of system installation or configuration, see the MMDS or MMEVS hardware manuals.

NOTE: *An AB32EM already installed in an MMDS station module can be reconfigured. To do so, switch off station-module power, then follow the guidance in this section. Similarly, AB32EM that is already installed on the MMEVS platform board can be reconfigured, provided that platform-board power is disconnected.*

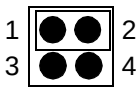
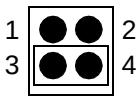
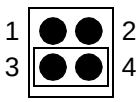
CAUTION: *Be sure to switch off or disconnect power when reconfiguring an installed EM. Reconfiguring EM jumper headers with the power on can damage system circuits.*

ESD CAUTION: *Ordinary amounts of static electricity from clothing or the work environment can damage or degrade electronic devices and equipment. For example, the electronic components installed on printed circuit boards are extremely sensitive to electrostatic discharge (ESD). Wear a ground wrist strap whenever handling any printed circuit board. This strap provides a conductive path for safely discharging static electricity to ground.*

2.3 Setting Jumper Headers

The AB32EM has three jumper headers. **Table 2-1** contains a summary of settings for these headers. Paragraphs **2.3.1 Clock Source Header (P1)** and **2.3.2 ADC Module Voltage Selector (P2 & P6)** give additional information about each jumper header.

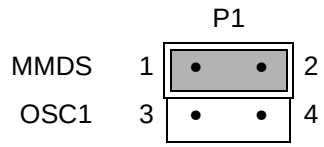
Table 2-1. Jumper Headers

Jumper Header	Type	Description
P1		Jumper between pins 1 and 2 (factory default); selects the clock signal from the MMDS control board or MMEVS platform board as the OSC1 input signal Jumper between pins 3 and 4; selects the target system clock as the OSC1 input signal
P2		Jumper between pins 1 and 2; selects the target system as the analog voltage source, VDDAREF, as input for the MC68HC908AB32 ADC module Jumper between pins 3 and 4 (factory default); selects on-board, isolated analog voltage source, LVDD, as input for the MC68HC908AB32 ADC module
P6		Jumper between pins 1 and 2; selects the target system as the analog ground source, AVSS/VREFL, as input for the MC68HC908AB32 ADC module Jumper between pins 3 and 4 (factory default); selects on-board ground, GND, as input for the MC68HC908AB32 ADC module

2.3.1 Clock Source Header (P1)

Use jumper header P1 (shown in **Figure 2-1**) to determine the clock signal source. The factory configuration (the fabricated jumper between pins 1 and 2) selects the clock signal from the MMDS control board or MMEVS platform board.

Figure 2-1. Jumper Header P1



Alternately, the target system clock signal source can be selected, as shown in **Figure 2-1**. To select the target system as the clock source, install the fabricated jumper between pins 3 and 4. Ensure that the clock source (OSC1) is connected to the EM via the target cable, connector P8 pin 7.

NOTE: *Only one jumper should be inserted on jumper header P1 at a time. Inserting multiple jumpers in P1 may damage the AB32EM.*

2.3.2 ADC Module Voltage Selector (P2 & P6)

Use jumper header P2 to select the on-board LVDD or an external analog voltage supply as the supply connection for the MC68HC908AB32 ADC convertor.

Figure 2-2 shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header P2 between pins 3 and 4.

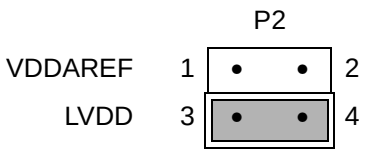


Figure 2-2. Jumper Header P2

Use jumper header P6 to select the on-board GND or the external analog ground as the ground connection for the MC68HC908AB32 ADC convertor.

Figure 2-3 shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header P6 between pins 3 and 4.

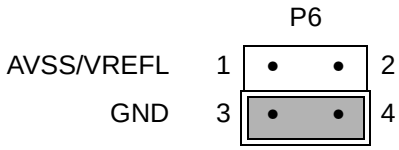


Figure 2-3. Jumper Header P6

2.4 Remaining System Installation

When all jumper headers are configured, follow these steps to complete the AB32EM installation:

- To install the AB32EM in an MMDS station module, remove the entire top half of the station-module enclosure. Fit together EM connectors P3 and P5 (on the bottom of the board) and control-board connectors P1 and P2. Snap the corners of the EM onto the plastic standoffs.
- To install the AB32EM on an MMEVS platform board, fit together EM connectors P3 and P5 (on the bottom of the board) and platform-board connectors P3 and P4. Snap the corners of the EM onto the plastic standoffs.
- Copy the personality file from the provided P&E CD-ROM or the CD-ROM that contains the technical documentation, M69EML08AB32/CD, to the directory that contains the debugging software. The personality files for the AB32EM are:
  - AB16AVxx.MEM - MC68HC908AB16A MCU (MCUez/P&E)
  - 00C58Vxx.MEM - MC68HC908AB32 MCU (MCUez)
  - 00458Vxx.MEM - MC68HC908AB32 MCU (P&E)

At this point, make any system cable connections and restore power. For instructions, consult the MMDS or MMEVS operations manuals.

Section 3. Connector Information

3.1 Contents

3.2 Introduction

This section consists of pin assignments and signal descriptions for M68EML08AB32 target and logic analyzer connectors.

3.3 Logic Analyzer Connector (P4)

Connector P4 is the AB32EM logic analyzer connector.

Figure 3-1 shows the pin assignments for connector P4. **Table 3-1** gives the signal descriptions.

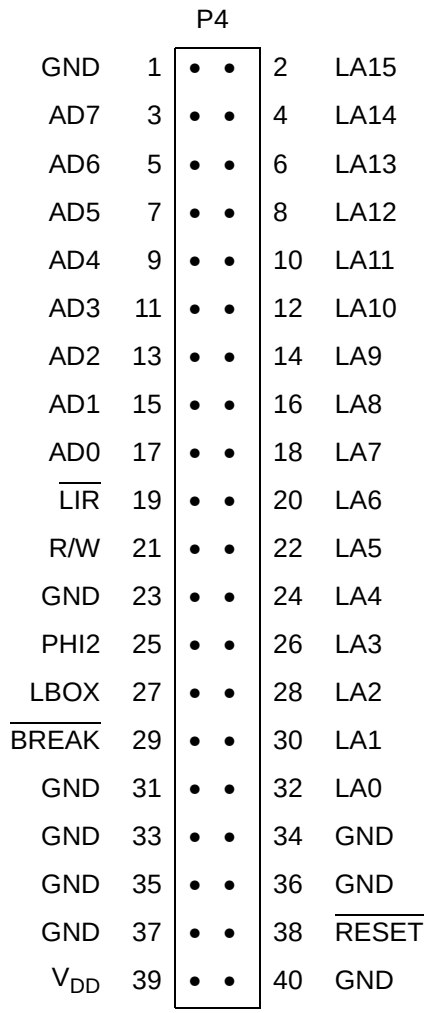


Figure 3-1. Logic Analyzer Connector P4 Pin Assignments

Table 3-1. Logic Analyzer Connector P4 Signal Descriptions

Pin	Mnemonic	Signal
1	GND	GROUND
2	LA15	Address bus bit 15 — MCU output address bus
3	AD7	Data bus bit 7 — MCU bidirectional data bus
4	LA14	Address bus bit 15 — MCU output address bus
5	AD6	Data bus bit 6 — MCU bidirectional data bus
6	LA13	Address bus bit 13 — MCU output address bus
7	AD5	Data bus bit 5 — MCU bidirectional data bus
8	LA12	Address bus bit 12 — MCU output address bus
9	AD4	Data bus bit 4 — MCU bidirectional data bus
10	LA11	Address bus bit 11 — MCU output address bus
11	AD3	Data bus bit 3 — MCU bidirectional data bus
12	LA10	Address bus bit 10 — MCU output address bus
13	AD2	Data bus bit 2 — MCU bidirectional data bus
14	LA9	Address bus bit 9 — MCU output address bus
15	AD1	Data bus bit 1 — MCU bidirectional data bus
16	LA8	Address bus bit 8 — MCU output address bus
17	AD0	Data bus bit 0 — MCU bidirectional data bus
18	LA7	Address bus bit 7 — MCU output address bus.
19	$\overline{\text{LIR}}$	Load instruction register — Active-low output signal, asserted when an instruction starts
20	LA6	Address bus bit 6 — MCU output address bus
21	R/W	Read/Write — Output signal that indicates the direction of data transfer
22	LA5	Address bus bit 5 — MCU output address bus
23	GND	GROUND
24	LA4	Address bus bit 4 — MCU output address bus
25	PHI2	PHI2 clock — Internally generated output clock signal used as a timing reference
26	LA3	Address bus bit 3 — MCU output address bus

Table 3-1. Logic Analyzer Connector P4 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
27	LBOX	Last bus cycle — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction
28	LA2	Address bus bit 2 — MCU output address bus
29	$\overline{\text{BREAK}}$	$\overline{\text{BREAK}}$ — Active low signal that the EM asserts to stop the target system MCU from running user code
30	LA1	Address bus bit 1 — MCU output address bus
31	GND	GROUND
32	LA0	Address bus bit 0 — MCU output address bus
33	GND	GROUND
34	GND	GROUND
35	GND	GROUND
36	GND	GROUND
37	GND	GROUND
38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional signal for starting an EVS reset
39	V_{DD}	+5 Vdc power — Input voltage (+5 Vdc @ 1A (max)) used by the EM logic circuits
40	GND	GROUND

3.4 Target Connectors (P7 and P8)

AB32EM has two target connectors: P7 and P8, each a 2-row by 20-pin connector.

Figure 3-2, **Table 3-2**, and **Table 3-3** give the pin assignments and signal descriptions for these connectors.

P7

GND	1	2	$\overline{IRQ}$	
PTC2	3	4	GND	
PTC0	5	6	PTF1	
NC	7	8	PTF3	
V_{DD}	9	10	NC	
LV_{DD}	11	12	PTF5	
PTD7	13	14	PTB7	
PTD5	15	16	PTD1	
PTH1	17	18	AV_{SS}/VREFL	
GND	19	20	PTD3	
PTB2	21	22	PTA7	
PTB4	23	24	GND	
PTB6	25	26	PTA4	
NC	27	28	PTA2	
NC	29	30	PTA0	
PTF6	31	32	PTG2	
PTE1	33	34	PTG0	
PTE3	35	36	GND	
PTE5	37	38	GND	
PTE7	39	40	GND	

P8

PTC5	1	2	PTC4	
PTC3	3	4	$\overline{RESET}$	
PTC1	5	6	PTF0	
OSC1	7	8	PTF2	
GND	9	10	PTF4	
GND	11	12	PTF7	
VREFH	13	14	GND	
PTD6	15	16	PTD0	
PTD4	17	18	VDDAREF	
PTH0	19	20	PTD2	
PTB1	21	22	PTB0	
PTB3	23	24	PTA6	
PTB5	25	26	PTA5	
GND	27	28	PTA3	
NC	29	30	PTA1	
NC	31	32	GND	
PTE0	33	34	PTG1	
PTE2	35	36	EVDD	
PTE4	37	38	GND	
PTE6	39	40	GND	

Figure 3-2. Target Connectors P7 and P8 Pin Assignments

Table 3-2. Target Connectors P7 Signal Description

Pin	Mnemonic	Signal
1	GND	EM GROUND — Ground signal of the EM board
2	$\overline{\text{IRQ}}$	INTERRUPT REQUEST — Active-low input line for requesting MCU asynchronous non-maskable interrupt
3	PTC2	PORT C (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
4	GND	EM GROUND — Ground signal of the EM board
5	PTC0	PORT C (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
6	PTF1	PORT F (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
7	NC	No connect
8	PTF3	PORT F (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
9	V_{DD}	MMDS +5 V — Used for factory testing
10	NC	No connect
11	LV_{DD}	AB32 EM Voltage high — Used for factory testing
12	PTF5	PORT F (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
13	PTD7	PORT D (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
14	PTB7	PORT B (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
15	PTD5	PORT D (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
16	PTD1	PORT D (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
17	PTH1	PORT H (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
18	AV_{SS}/VREFL	Analog ground pin for ADC convertor and the ADC voltage referance low
19	GND	EM GROUND — Ground signal of the EM board
20	PTD3	PORT D (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-2. Target Connectors P7 Signal Description (Continued)

Pin	Mnemonic	Signal
21	PTB2	PORT B (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
22	PTA7	PORT A (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
23	PTB4	PORT B (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
24	GND	EM GROUND — Ground signal of the EM board
25	PTB6	PORT B (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
26	PTA4	PORT A (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
27	NC	No connect
28	PTA2	PORT A (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTA0	PORT A (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
31	PTF6	PORT F (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
32	PTG2	PORT G (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
33	PTE1	PORT E (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
34	PTG0	PORT G (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
35	PTE3	PORT E (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
36	GND	EM GROUND — Ground signal of the EM board
37	PTE5	PORT E (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
38	GND	EM GROUND — Ground signal of the EM board
39	PTE7	PORT E (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-2. Target Connectors P7 Signal Description (Continued)

Pin	Mnemonic	Signal
40	GND	EM GROUND — Ground signal of the EM board

Table 3-3. Target Connectors P8 Signal Descriptions

Pin	Mnemonic	Signal
1	PTC5	PORT C (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
2	PTC4	PORT C (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
3	PTC3	PORT C (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
4	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional control line that initializes the MCU
5	PTC1	PORT C (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
6	PTF0	PORT F (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
7	OSC1	OSCILLATOR — Crystal oscillator amplifier input signal
8	PTF2	PORT F (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
9	GND	EM GROUND — Ground signal of the EM board
10	PTF4	PORT F (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
11	GND	EM GROUND — Ground signal of the EM board
12	PTF7	PORT F (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
13	VREFH	ADC voltage reference high
14	GND	EM GROUND — Ground signal of the EM board
15	PTD6	PORT D (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
16	PTD0	PORT D (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
17	PTD4	PORT D (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
18	VDDAREF	Analog supply pin for ADC convertor
19	PTH0	PORT H (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
20	PTD2	PORT D (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-3. Target Connectors P8 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
21	PTB1	PORT B (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
22	PTB0	PORT B (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
23	PTB3	PORT B (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
24	PTA6	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
25	PTB5	PORT B (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
26	PTA5	PORT A (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
27	GND	EM GROUND — Ground signal of the EM board
28	PTA3	PORT A (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTA1	PORT A (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
31	NC	No connect
32	GND	EM GROUND — Ground signal of the EM board
33	PTE0	PORT E (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
34	PTG1	PORT G (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
35	PTE2	PORT E (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
36	EVDD	Target system Voltage high
37	PTE4	PORT E (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
38	GND	EM GROUND — Ground signal of the EM board
39	PTE6	PORT E (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
40	GND	EM GROUND — Ground signal of the EM board

3.5 Target Cable Assembly

To connect the AB32EM to a target system, a separately purchased target cable assembly is needed, plus the appropriate target head and target-head/adapter package.

Figure 3-3 shows how one end of the flex cable plugs into the AB32EM module, and it also shows how the target head connects into the target system.

If the AB32EM is installed in the MMDS station module, run the flex cable through the slit in the station-module enclosure.

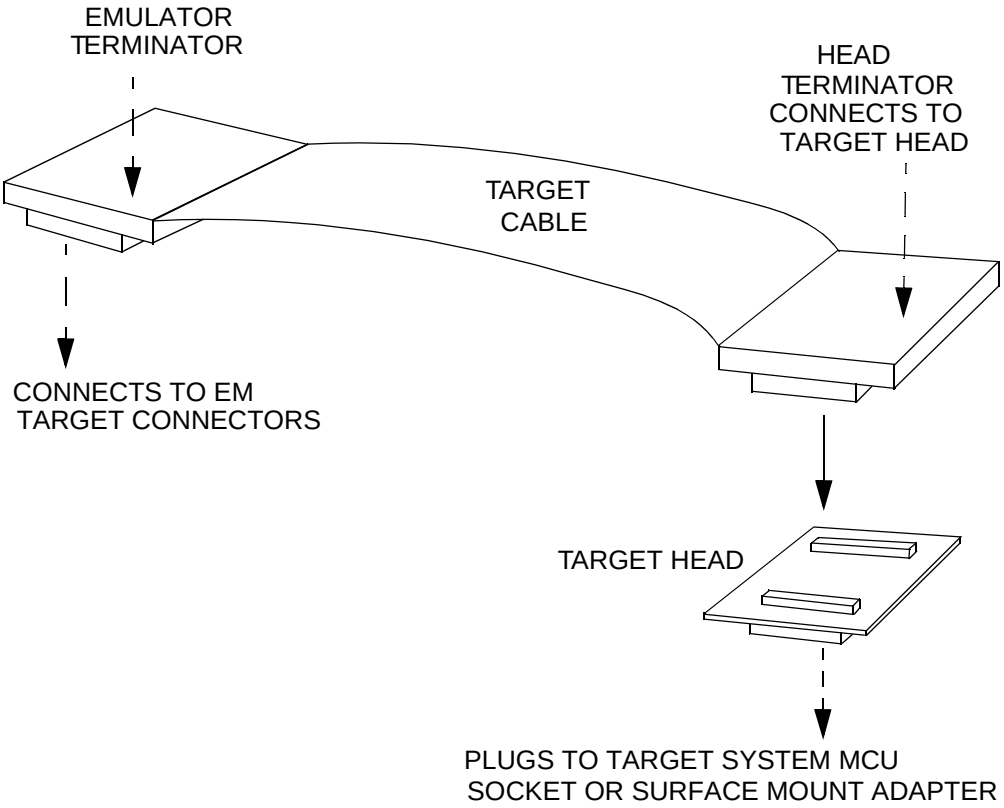


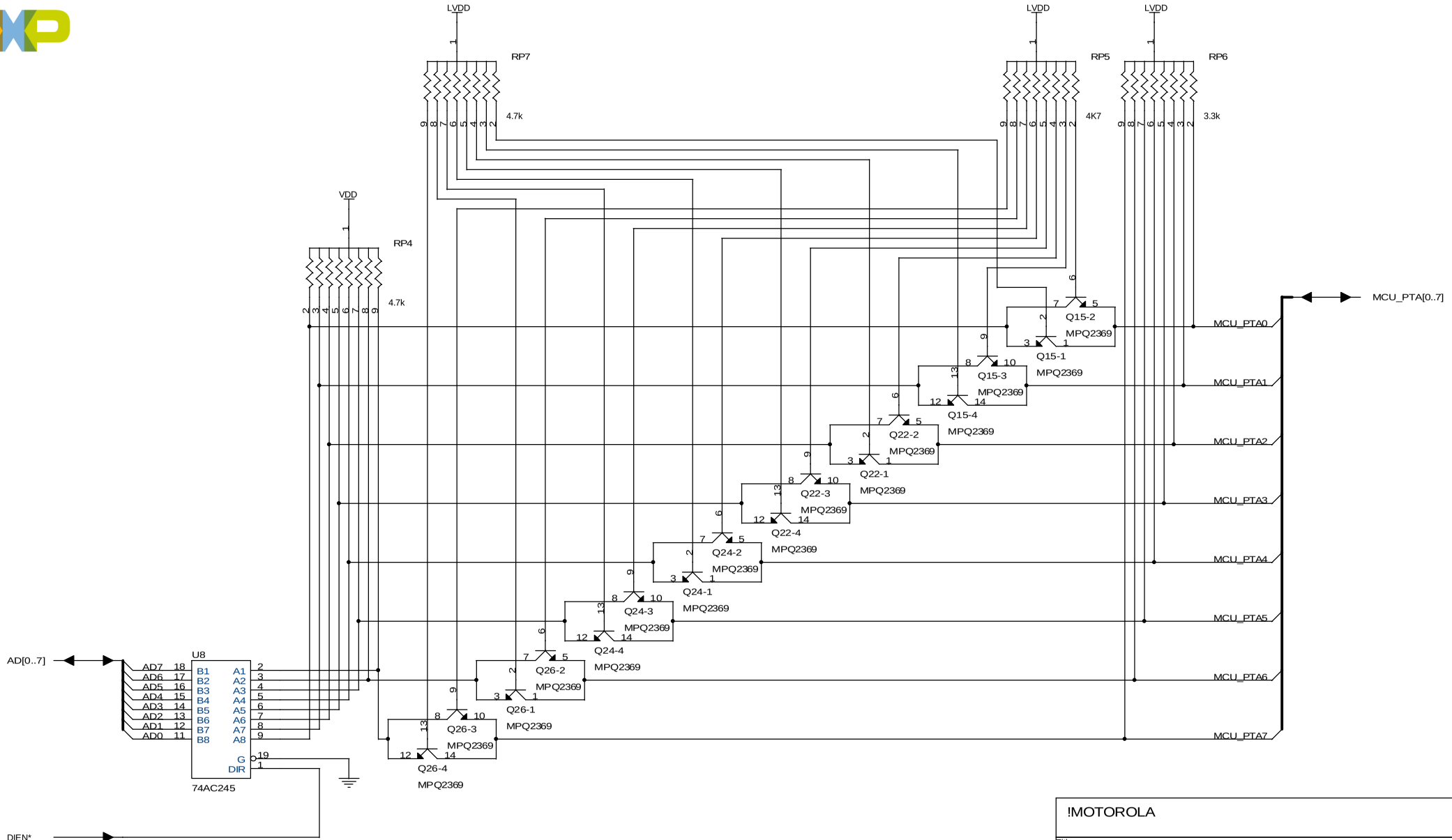
Figure 3-3. Target Cable Assembly

Connector Information

Section 4. Schematics

This chapter contains the M68EML08AB32 emulator module schematic diagrams.

These schematic diagrams are for reference only and may deviate slightly from the circuits on the AB32EM.

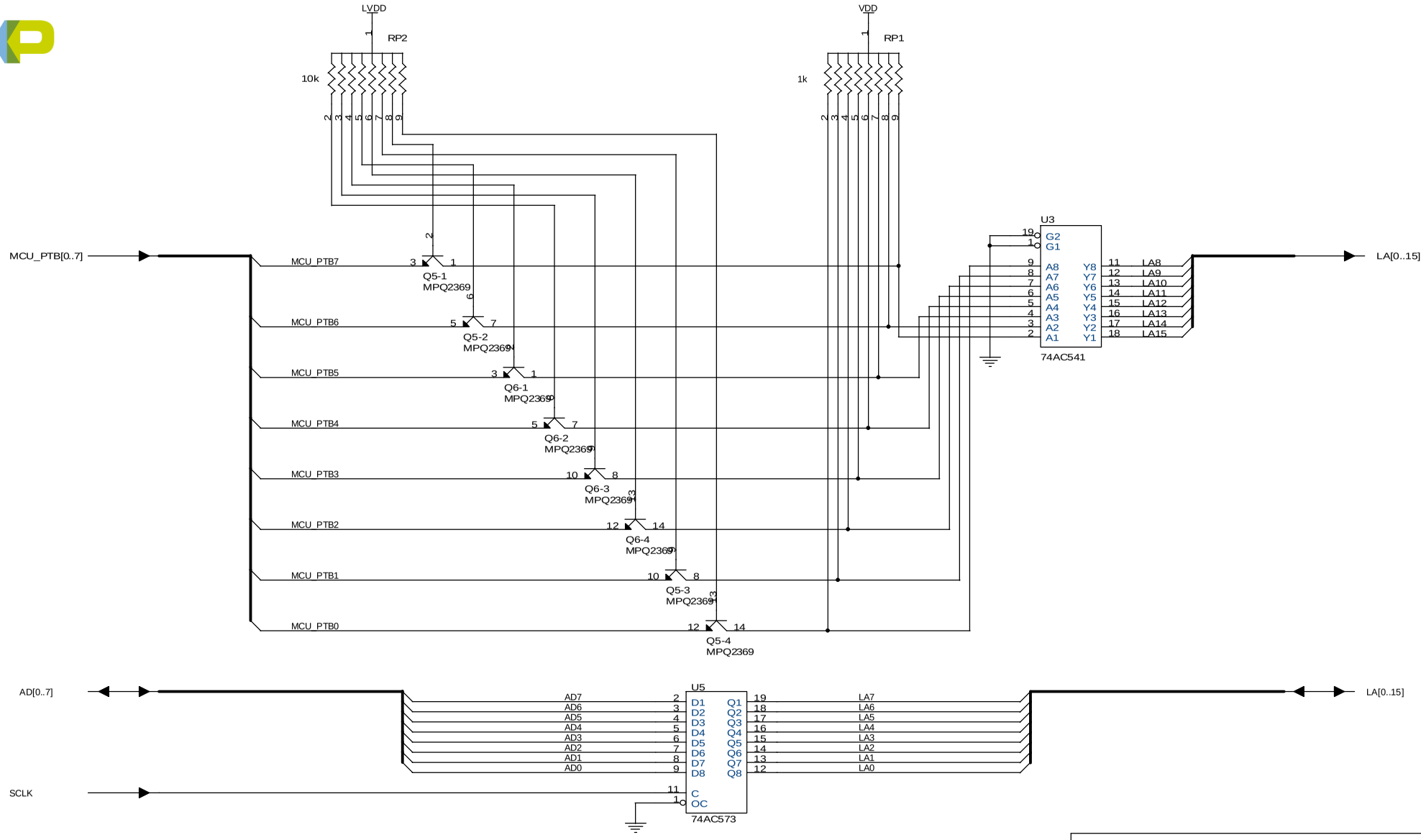


!MOTOROLA

Title: M68EML08AB32 EMULAOTR MODULE (AD bus buffer)

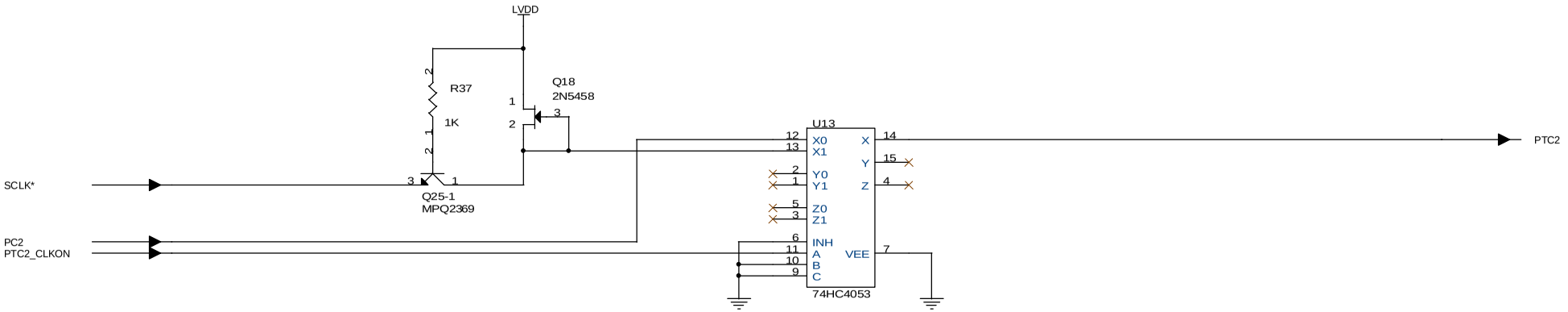
Size	Designed By:	Approved By:	Rev
B	Kelvin Tse	Edward Chui	A

Date: Tuesday, February 22, 2000 Sheet 1 of 13



!MOTOROLA

Title: M68EM08AB32 EMULATOR MODULE (Address bus buffer)			
Size: B	Designed By: KELVIN TSE	Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000	Sheet 2 of 13		

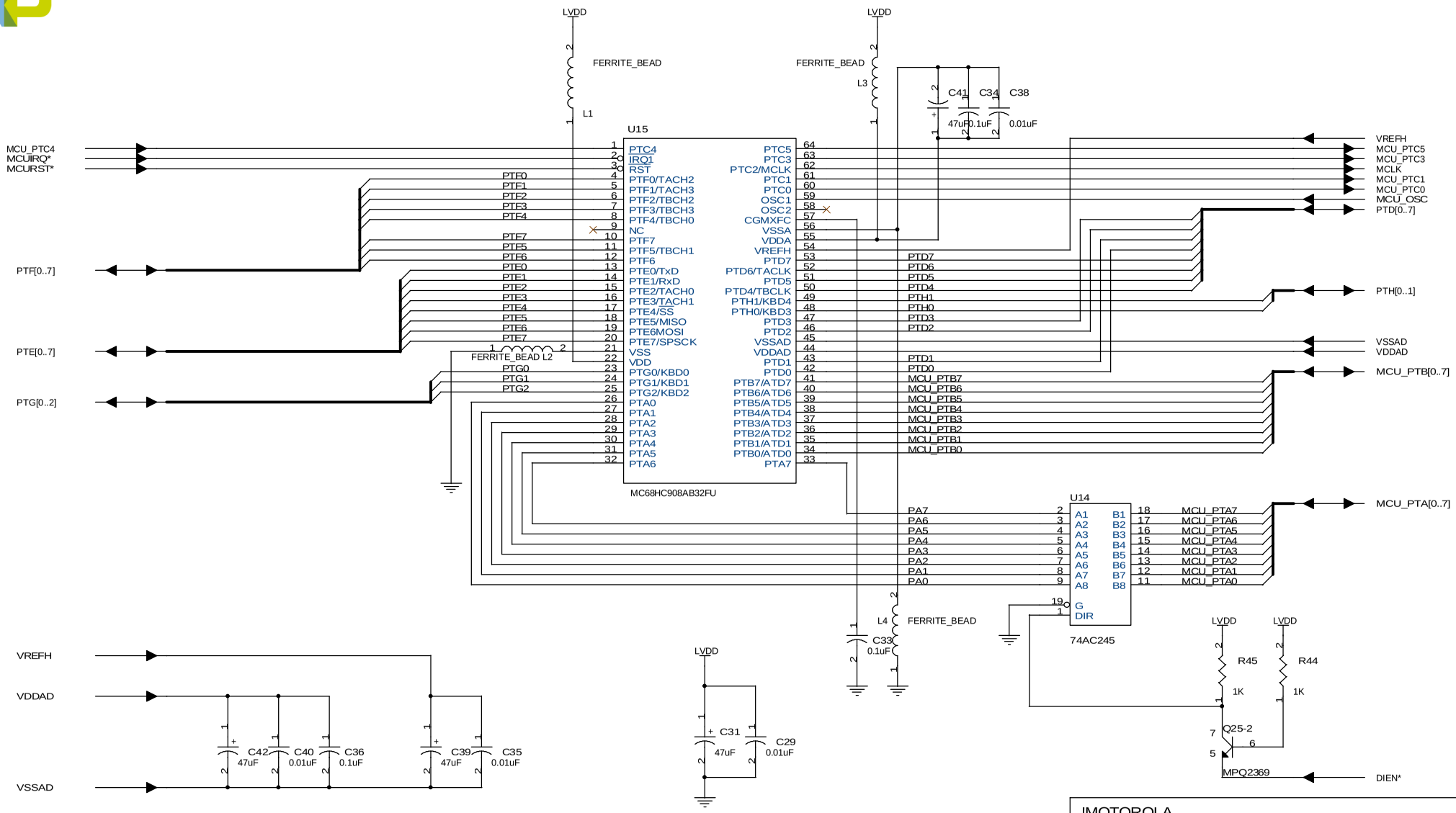


!MOTOROLA

Title: M68EML08AB32 EMULATOR MODULE (CLOCK INPUT)

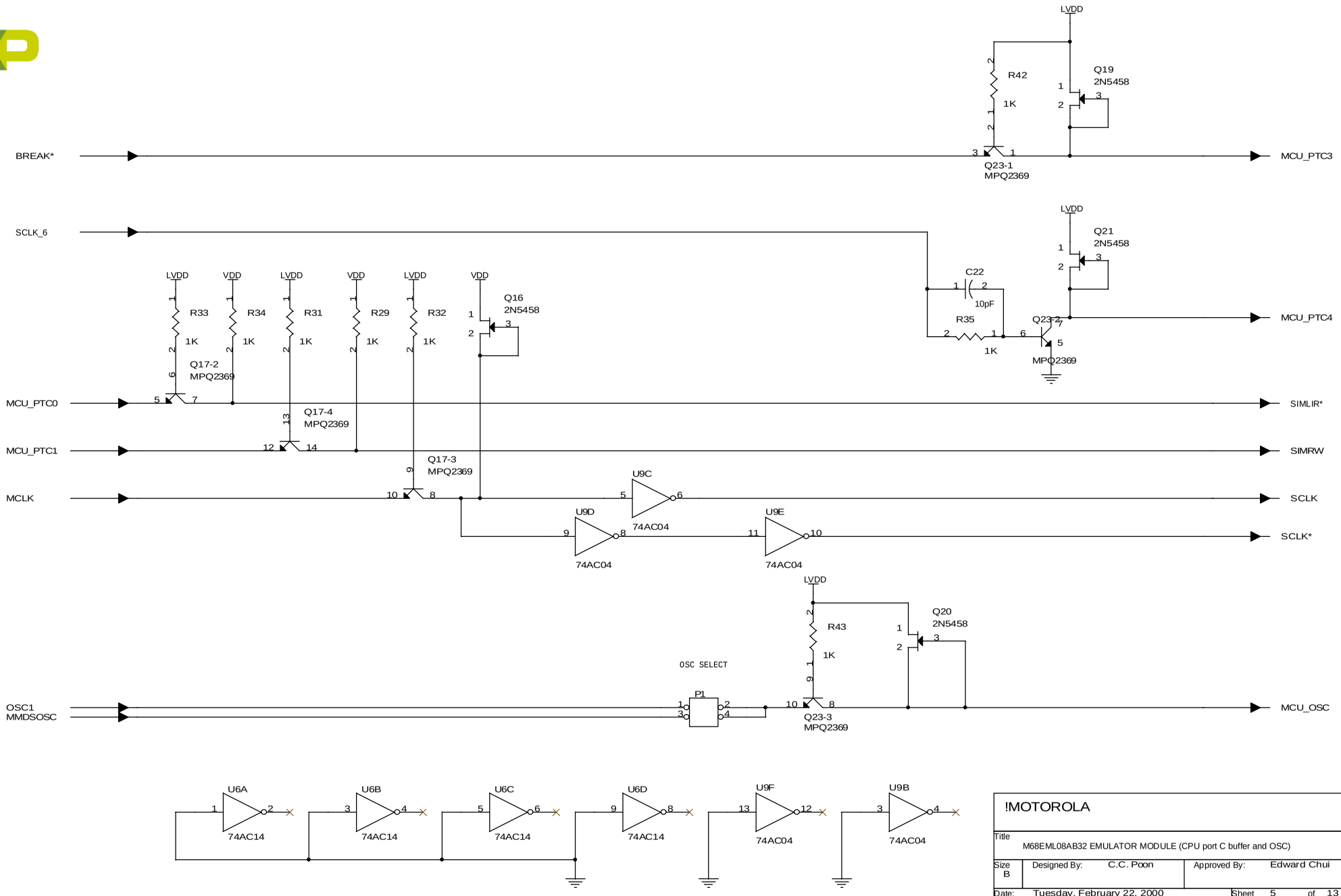
Size	Designed By:	Approved By:	Rev
B	Kelvin Tse	Edward Chui	A

Date: Tuesday, February 22, 2000 Sheet 3 of 13



!MOTOROLA

Title	M68EML08AB32 EMULATOR MODULE (CPU)			
Size B	Designed By: Kelvin Tse		Approved By: Edward Chui	Rev A
Date: Tuesday, February 22, 2000		Sheet 4 of 13		

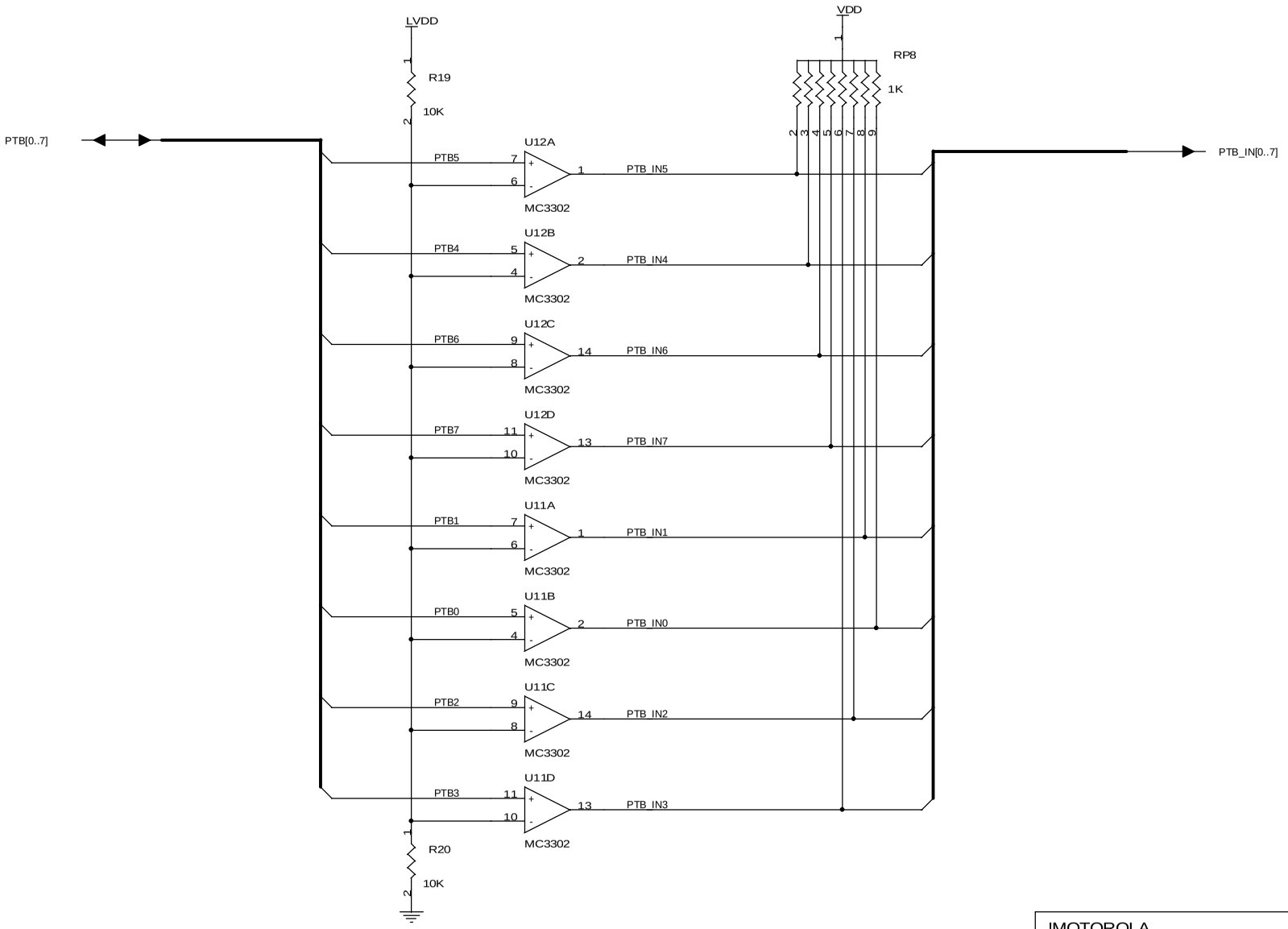


!MOTOROLA

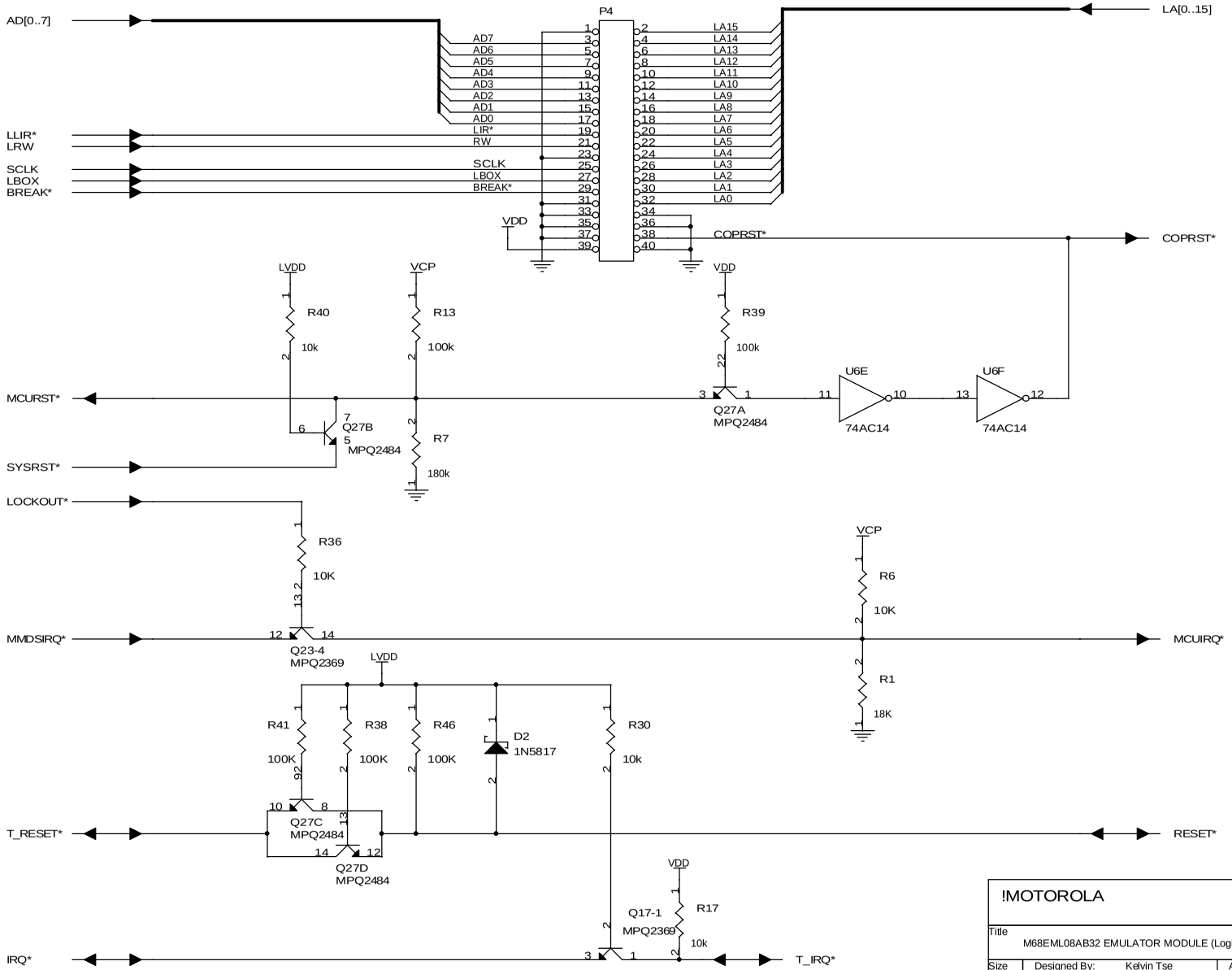
Title: M68EML08AB32 EMULATOR MODULE (CPU port C buffer and OSC)

Size	Designed By:	Approved By:	Rev
B	C.C. Poon	Edward Chui	A

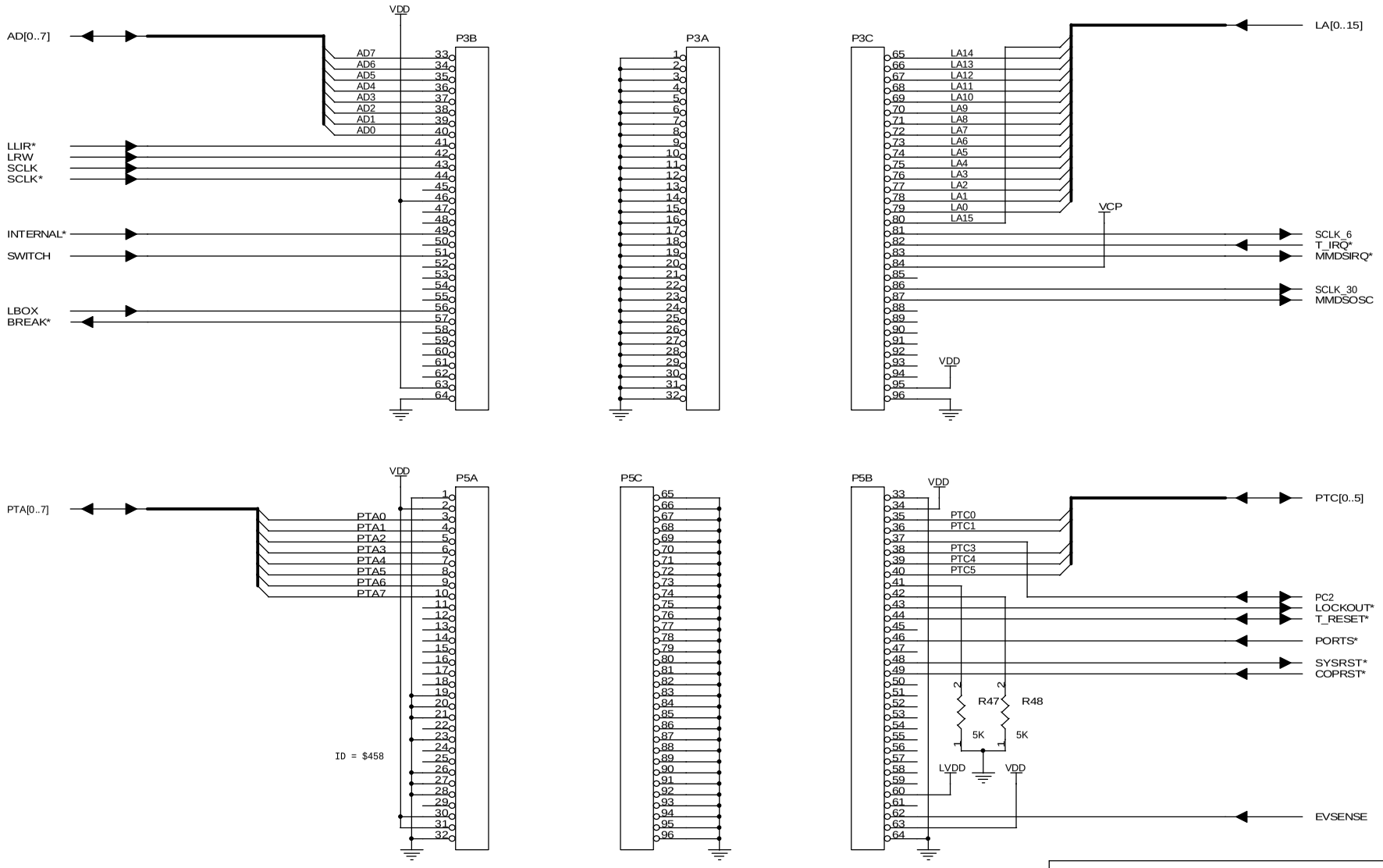
Date: Tuesday, February 22, 2000 Sheet 5 of 13



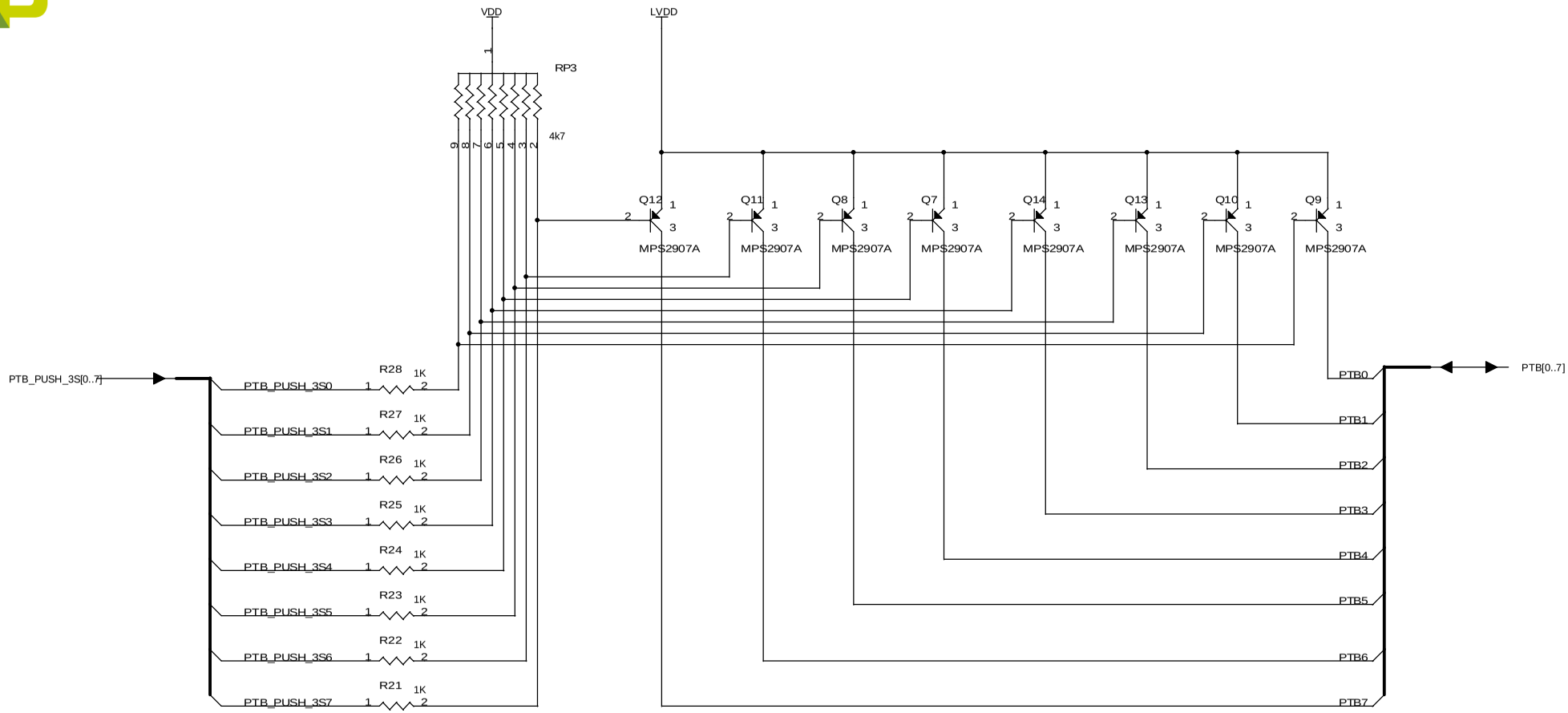
!MOTOROLA				
Title: M68EML08AB32 EMULAOTR MODULE (Keyboard Interrupt)				
Size: B	Designed By: Kelvin Tse		Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000		Sheet 6 of 13		



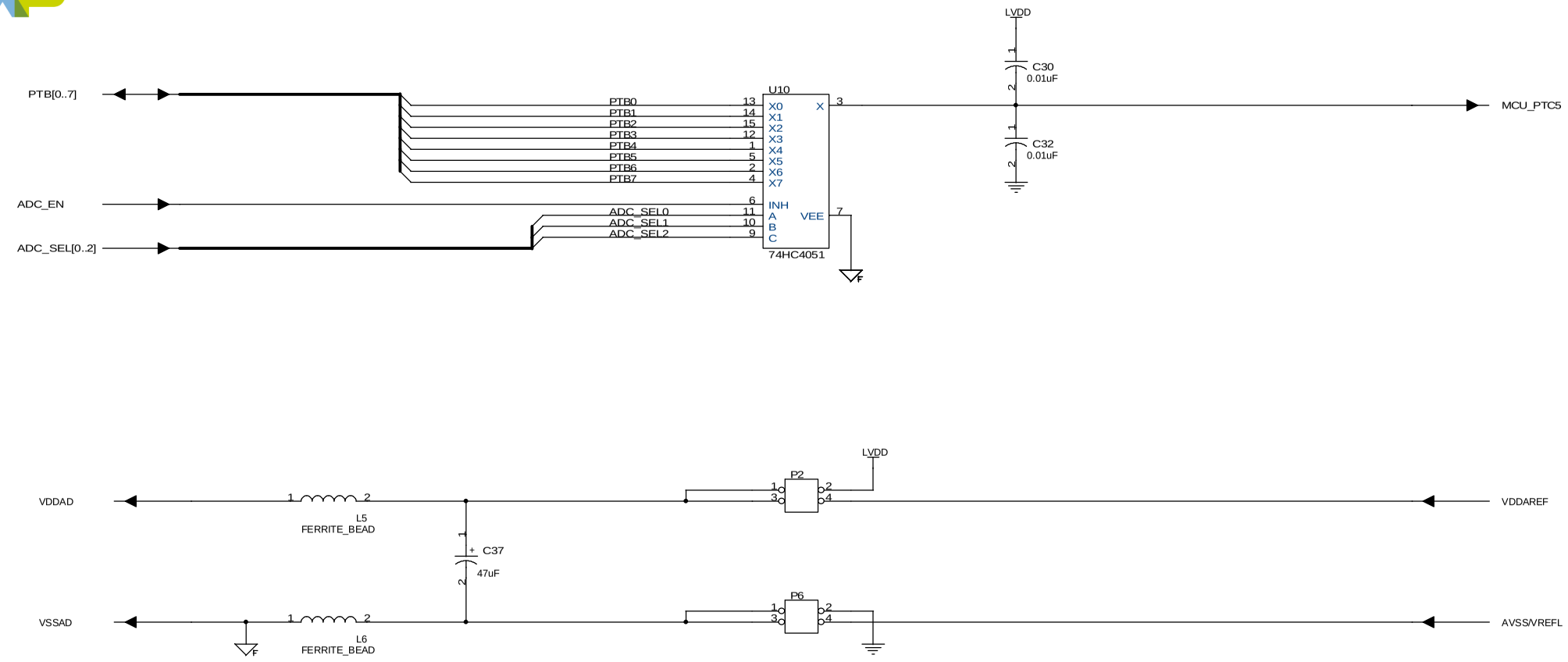
!MOTOROLA			
Title: M68EML08AB32 EMULATOR MODULE (Logic analyzer connector / IRQ / RST)			
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000	Sheet 7 of 13		



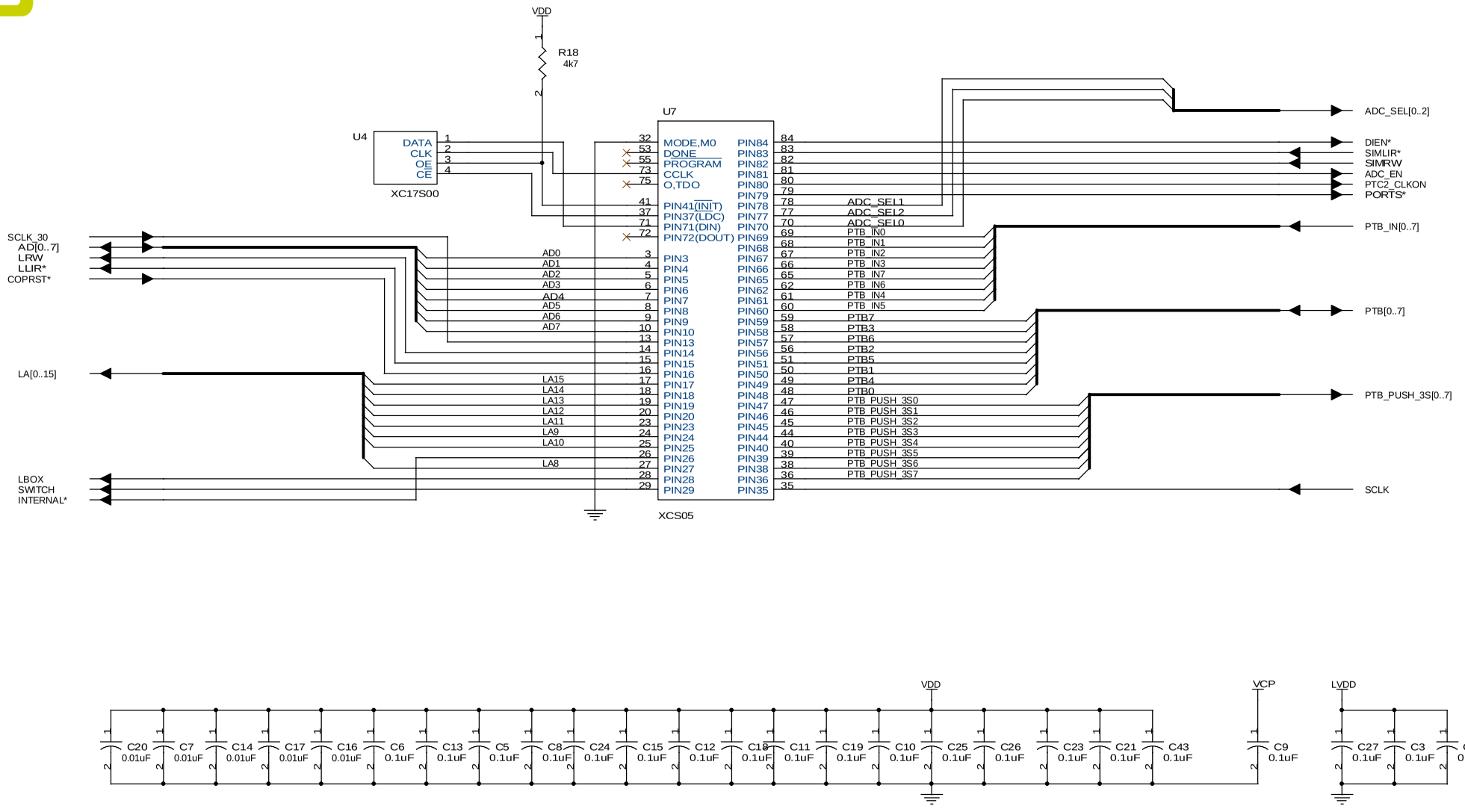
!MOTOROLA			
Title: M68EML08AB32 EMULATOR MODULE (Platform board connectors)			
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000	Sheet 8 of 13		



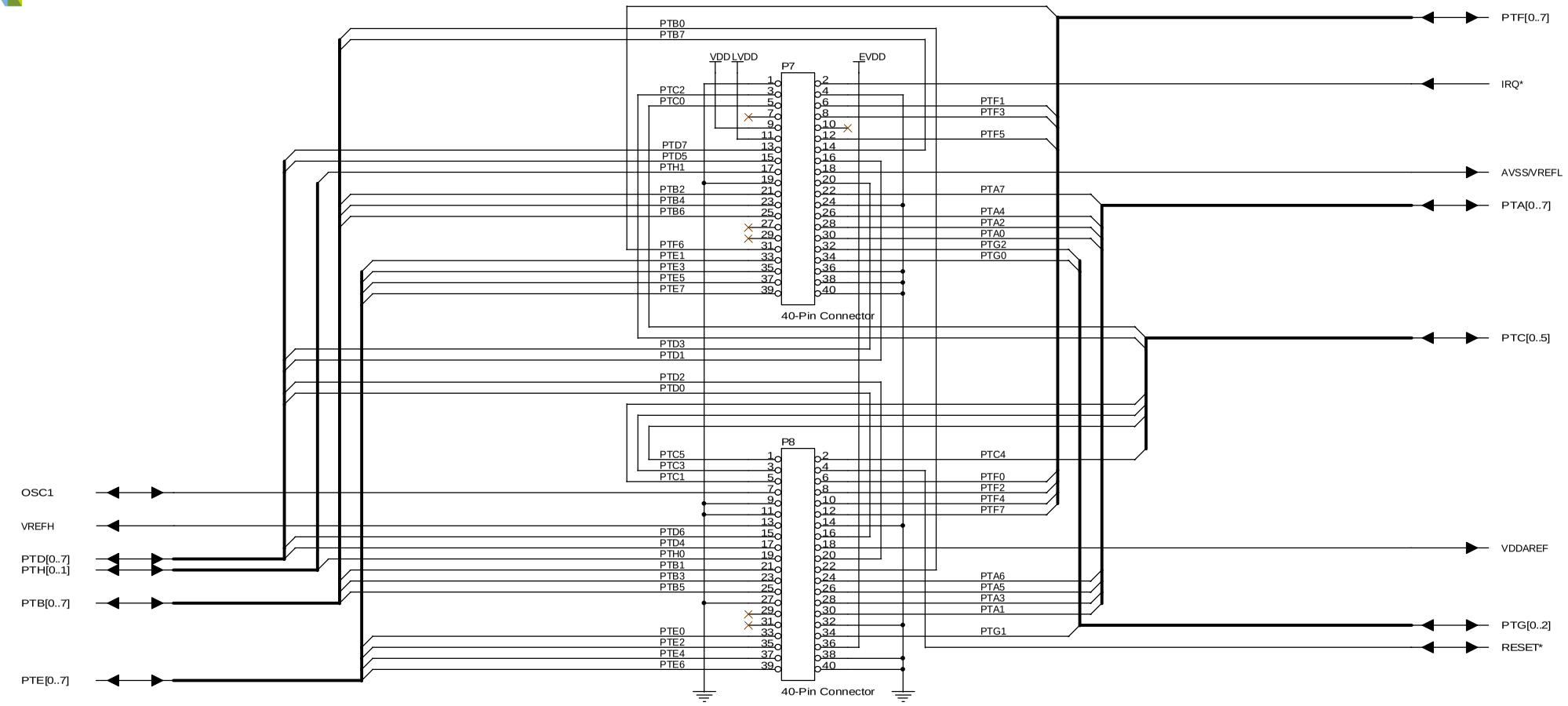
!MOTOROLA			
Title: M68EML08AB32 EMULATOR MODULE (Port B)			
Size: B	Designed By: C.C. Poon	Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000	Sheet 9 of 13		



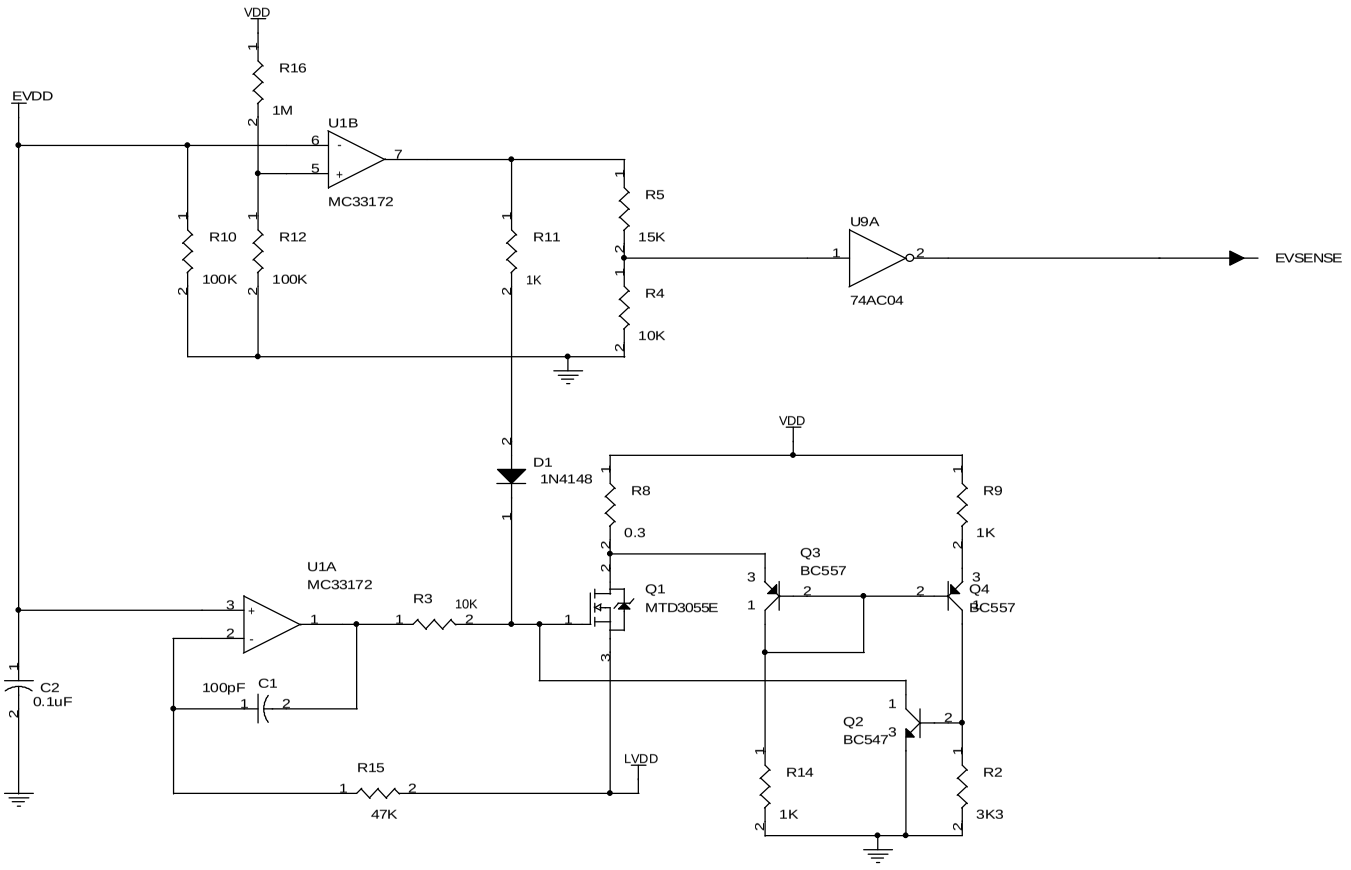
!MOTOROLA			
Title: M68EML08AB32 EMULATOR MODULE (Port B and ADC Input)			
Size: B	Designed By: C.C. Poon	Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000	Sheet 10 of 13		



!MOTOROLA			
Title: M68EML08AB32 EMULATOR MODULE (Programmable Logic module)			
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: A
Date: Tuesday, February 22, 2000	Sheet 11 of 13		



!MOTOROLA			
Title: M68EML08AB32 EMULATOR MODULE (Target head connector)			
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000	Sheet 12 of 13		



!MOTOROLA				
Title: M68EML08AB32 EMULATOR MODULE (Voltage regulator)				
Size: B	Designed By: Kelvin Tse		Approved By: Edward Chui	Rev: A
Date: Monday, February 21, 2000		Sheet 13 of 13		

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