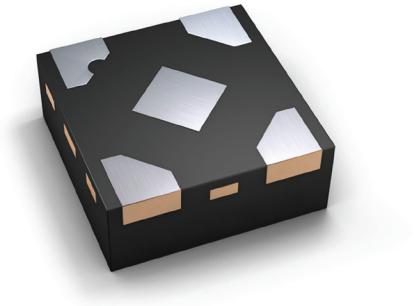
NXP's innovative GX packages: Saving space, reducing cost

Discrete logic is certainly not new, and NXP recognizes its enduring importance for today's applications. That's why we continue to innovate.

With the wide availability of affordable microcontrollers, FPGAs, and ASICs, modern systems no longer need discrete logic as the foundation for a device's digital functionality. At the same time, however, industry trends are imposing constraints that make discrete logic an increasingly valuable design tool. Engineers are confronting the demands for quick time to market with lower cost, that are highly portable—or even wearable—devices with long battery life. When facing challenges such as these, designers need something that discrete logic provides: flexibility.

If requirements change and the preferred microcontroller no longer has enough I/O pins, discrete logic is a simple approach to I/O expansion. If existing ASICs cannot communicate properly because of incompatible timing, clock-edge specifications or different voltage levels, a discrete logic device can usually provide a quick and inexpensive solution. Discrete buffers provide higher current for driving LEDs and improved signal integrity for serial communication over long cables or in noisy environments, translators/level shifters provide the interface between systems or sub-systems with different operating voltages.

These are a few examples of the many ways in which discrete logic offers today's engineers a variety of straightforward, inexpensive solutions that brings flexibility to the development process and the final product. However, in these situations, packaging characteristics are an especially important factor in a designer's ability to address his design/interface issues. Once the electrical problem has been solved, the designer is faced with finding a practical solution, one that can be incorporated into the existing PCB board layout and not put an undue manufacturing/assembly burden on the production operation. Thus, the selection of the package that incorporates the logic solution is very important—one that uses the least amount of PCB real estate while at the same time is easy to use in the assembly process.



The GX package

NXP is committed to innovation in the field of discrete logic. We are the industry leaders in improving all aspects of logic-device packaging and performance. As part of this effort, we first introduced the 5-pin GX package in 2012.

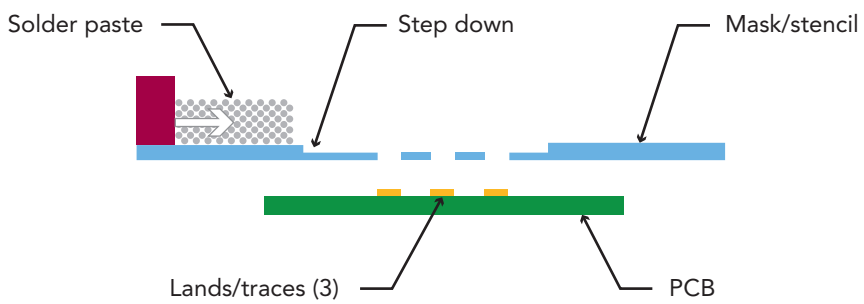
This package is certainly compact at 0.8 mm × 0.8 mm, with a height of only 0.35 mm. But the most important feature is the novel placement of the contacts — by utilizing the space at the corners of the package and including a terminal in the center of the part, NXP developed a package that provides an extremely small form factor while maintaining a pitch greater than 0.4 mm.

To understand the full significance of this innovative design, we need to consider some details related to PCB assembly procedures.

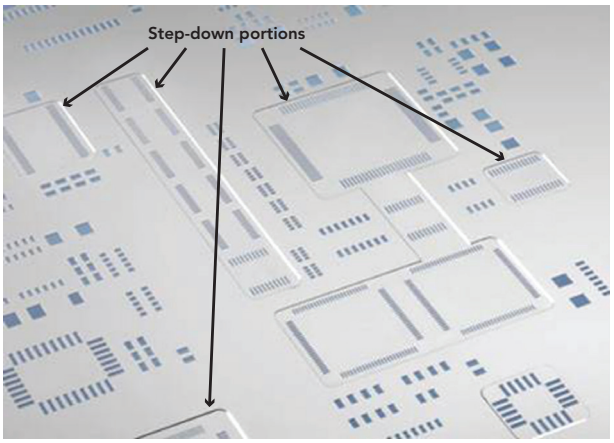
The trade-off: lead pitch vs. DFM

Design for manufacturability (DFM) is a critical factor in the success of high-volume products. At the same time, consumers expect ongoing miniaturization, especially with portable and wearable devices such as mobile phones, smart tablets, and biometric sensors. A conflict arises when package miniaturization requires a pin or land pitch that is smaller than 0.4 mm, because this is the approximate threshold at which standard manufacturing practices can become expensive and unreliable.

When a component's pitch is less than 0.4 mm, the board-assembly process may need to be modified to ensure that reflow soldering does not result in shorts between pins. First, fine-pitch components are more likely to require costly Type 4 solder paste, rather than the standard Type 3. Type 4 paste, which has higher viscosity and smaller particle size, is more effective with small stencil apertures.



Second, the thickness of the solder stencil must be reduced. Reducing the stencil thickness leads to a corresponding reduction in the amount of solder deposited on the pad, and this smaller quantity of solder is less likely to form a bridge between adjacent pads. In order to ensure adequate mechanical strength and accommodate smaller or tighter pitch components, the assembly process for these components with very-fine-pitch will employ a so-called "step-down" stencil.



Step-down stencil

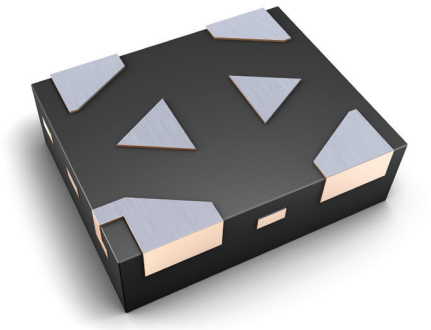
Such stencils are, of course, more complex to manufacture and therefore more expensive; they are also more fragile and may need to be replaced more frequently. In addition to the increased cost, the need for a step-down stencil imposes irksome restrictions on component placement—the smaller-pitch components must be located in PCB areas that correspond to the thinner sections of the stencil.

Saving space, reducing cost

We can see from the previous discussion that GX devices represent a milestone in IC packaging technology: same functionality, less board space, improved manufacturability. Let's consider some numbers. The 6-pin SOT891 package is 1 mm × 1 mm, with a pitch of 0.35 mm. So we have a component area of 1 mm^2, and with a pitch of 0.35 mm we will surely need to confront the manufacturing difficulties discussed above. The GX package, at 0.8 mm × 0.8 mm, offers a component area of 0.64 mm^2—a 36% reduction compared to the SOT891. And despite this significantly smaller footprint, the pitch has increased to > 0.4 mm, enough to eliminate the DFM issues.

It's true that the GX package has only five pins whereas the SOT891 has six, but the sixth pin is unnecessary for many components. Numerous logic devices—including single-channel buffers and inverters, two-input Boolean gates—can be implemented with only three pins in addition to power and ground.

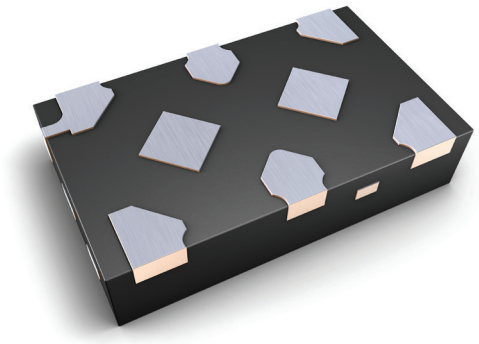
Furthermore, NXP recently introduced a 6-pin version of the GX package.



The 6-pin GX offers the same DFM advantages as the 5-pin version while greatly increasing the number of logic devices that can benefit from this innovative package design. With four pins in addition to power and ground, the list expands to include, for example, dual buffers and inverters, three-input Boolean gates, three-input configurable gates, and two-input multiplexers. And with dimensions of 0.8 mm × 1 mm, the 6-pin GX still offers reduced component area compared to the SOT891.

More pins, more functionality, more benefits

NXP is pleased to introduce our latest packaging innovation: the 8-pin GX.



The GX-8 represents NXP's determination to offer compact, cost-effective packages that respond to the market's increasing demand for single- and dual-gate logic devices. The GX-8 has a pitch greater than 0.4 mm and thus maintains the DFM benefits associated with the 5- and 6-pin GX. But the additional pins offered by the GX-8 open up new opportunities for the inclusion of additional, more complex functions while saving board space and reducing assembly costs.

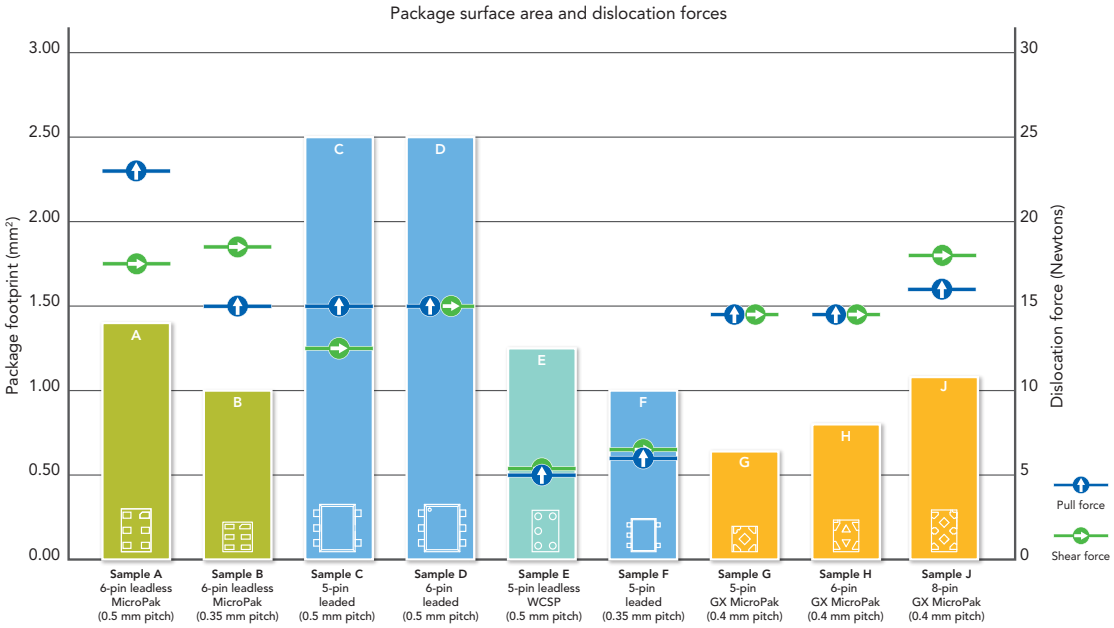
With six pins in addition to power and ground, GX-8 devices can have four inputs and two outputs—enough for two separate Boolean gates. And with capacity for two gates, the 8-pin GX can support combination logic, i.e., devices that integrate different logic functions (such as one NAND gate and one NOR gate) into a single package. Combination logic is a valuable tool for the PCB designer:

- The cost of one dual-gate package is lower than the cost of two single-gate packages.
- Combining two logic functions into one device saves space by reducing pin count: two separate gates would require two 5-pin devices and thus 10 pins total, whereas two gates in a combination-logic device can be implemented with only 8 pins. The fundamental benefit here is the ability to use the same power and ground connections for two different gates and combining them into one package that is much smaller than the sum of two individual packages and the spacing between them.
- Standard design practice calls for at least one power-supply decoupling capacitor for every integrated circuit. Combination logic eliminates not only the second package but also the second decoupling capacitor.
- Combination logic can enhance manufacturing efficiency. Pick-and-place machines have limited capacity with respect to how many different parts can be placed by one machine. Combination logic reduces the number of items in the BOM and thus helps to avoid additional pick-and-place operations.

Leads or no leads?

The GX, like various other NXP logic packages, is leadless—that is, it connects to the PCB through metal pads or "lands" instead of protruding leads. There are a number of benefits associated with leadless packages. These are not specific to GX devices, but it's important to recognize that the GX package offers not only the DFM improvements discussed already but also the following advantages over leaded devices:

- Leadless packages are actually more mechanically robust than comparable leaded packages; the pads present a larger contact area and thus allow for a stronger bond. NXP has abundant empirical data that confirms the reliability of leadless packages such as the GX.



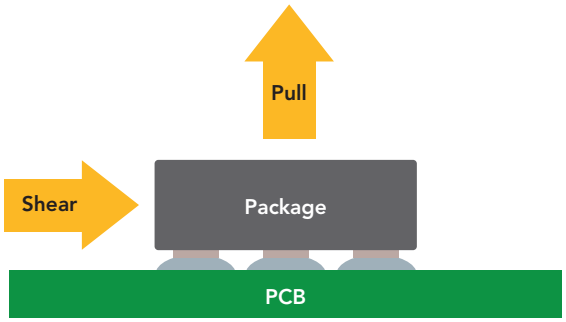
- The connection pads for GX and other leadless devices are flat metal surfaces on the bottom of the package; this eliminates assembly difficulties that can occur when the pins of a leaded package are either bent or do not exhibit sufficient coplanarity.
- Reflow soldering automatically corrects for small errors in component placement or orientation because the surface tension of molten solder naturally favors good alignment between a component and its corresponding PCB pads. However, this effect is more pronounced with leadless packages because they are smaller and lighter than comparable leaded packages.
- Even electrical performance can improve when moving from leaded to leadless devices: leadless packages offer lower parasitic inductance and thus enhanced signal integrity for high-speed applications.

Contact area vs. chip area: the key to mechanical strength

As mentioned in the previous section, leadless packages offer superior durability compared to leaded packages. The primary reason for this is quite simple: solder provides the mechanical connection between a device and the PCB, and packages that have a higher ratio of contact area to package area will have more solder relative to the size of the package/IC.

As shown in the below "surface area vs. contact area" table, samples A and B (both leadless) have far higher contact-area-to-chip-area ratio than the leaded parts. Furthermore, testing conducted by NXP has

confirmed that leadless components can surpass leaded components in their ability to withstand both pull force and shear force.



GX devices are leadless and thus share in this enhanced durability. However, the unique geometry of the 5-pin GX package creates an even higher contact-area-to-package-area ratio. This means that the GX family of packages may be not only the world's smallest but also the world's strongest logic package.

Surface area vs. contact area

Package	Sample	Package area (mm^2)	Contact area (mm^2)	Ratio
SOT886	A	1.45	0.39	27%
SOT891	B	1.00	0.30	30%
5-pin leaded (0.5 mm pitch)	C	2.50	0.21	16%
6-pin leaded (0.5 mm pitch)	D	2.50	0.25	10%
5-ball WCSP (0.5 mm pitch)	E	1.35	0.20	15%
5-pin leaded (0.35 mm pitch)	F	1.0	0.06	6%
5-pin GX (SOT1226)	G	0.64	0.21	34%
6-pin GX (SOT1255)	H	0.8	0.19	24%
8-pin GX (SOT1233)	J	1.08	0.29	26%

Conclusion

Space-constrained applications have benefited immensely from the high levels of integration offered by microcontrollers, FPGAs, and sophisticated ASICs. Nonetheless, discrete logic is and will continue to be an important factor in enabling designers to produce low-cost, high-performance devices that satisfy the market's expectations for increasing portability and continuous innovation.

NXP is committed to supplying the logic devices that engineers need, and the GX package—truly a breakthrough in IC packaging technology—is a prime manifestation of this commitment. For more information, including a list of devices available in the 5-pin, 6-pin, and 8-pin GX packages, please visit our website: www.nxp.com/logic.

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