NXP Semiconductors Application Note

i.MX7 SABRE SD Board—Running the Core at 1.2 GHz

1. Introduction

NXP introduced a new part to the i.MX7 D lineup of MPUs. These new MPUs (MCIMX7D2DVK12SC and MCIMX7D2DVM12SC) can run their cores up to a maximum of 1.2 GHz. This application note shows you how to run the current SABRE SD board at this higher frequency.

Note that the components on the SABRE board are specified to a maximum core frequency of 1.0 GHz. Running at this higher frequency is not guaranteed to function and reduces the lifetime of the part. See *i.MX7 Dual/Solo Product Lifetime Usage* (document AN5334) for details.

Although the i.MX7 that is delivered on this board is not specified to run at this higher frequency, most parts tolerate this frequency at a room temperature for evaluation purposes.

The two new MPUs added to the i.MX 7D family (MCIMX7D2DVK12SC and MCIMX7D2DVM12SC) are the only parts guaranteed to operate at 1.2 GHz. They have no reduction of operating lifetime at this CPU frequency.

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2. Required operational changes

For the core to operate at this higher frequency, the Vdd_ARM voltage must be increased to 1.22 V from 1.1 V (1 GHz). Also, the clock driving the ARM[®] Cortex[®]-A7 cores must be increased to 1.2 GHz. These parameters are software-controlled on the SABRE board. It means that the higher speed evaluation is only available while running Linux with a modified DTB file.

2.1. BSP changes

The changes to the BSP are very simple and limited to one file. A new DTB file is required to enable Linux to change the frequency and the Vdd_ARM voltage. The source file *imx7d.dtsi* must be modified and then recompiled.

An additional line must be inserted into the "operating-points" section (highlighted in yellow). The diff file output is as follows:

The added line adds 1200000 KHz and 1200000 μ V, which indicates a new operational point of 1.2 GHz at 1.2 V. The higher voltage enables the chip to operate at this higher frequency. Note that this higher voltage reduces the operating life of the chip, so run at this frequency/voltage combination only when needed. Linux changes the operating frequency up and down as it determines the need for additional performance.

When this change is made to the DTSI file and the file is recompiled, it generates the proper DTB file that must be included in the u-boot environment, and this information is passed to the Linux kernel when booting.

3. Required u-boot changes

For Linux to operate at this new speed, add the new file to the bootable partition and make the "fdt_file" parameter point to the new DTB file. To accomplish this, copy the new DTB file to the FAT file system side of the SD card. Change the "fdt_file" parameter to point to the new file, as shown in Figure 1.

In this example, the DTB file is named "imx7d-sdb.1.2ghz.dtb":



Figure 1. DTB file naming

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This is confirmed as follows:

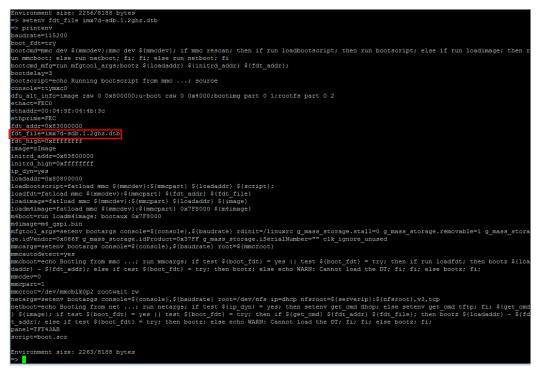


Figure 2. DTB file naming confirmation

4. Verifying faster speeds

To verify that the new FDT file is used, run the *cpufreq-info* program on the serial console. Here is the output you should see:

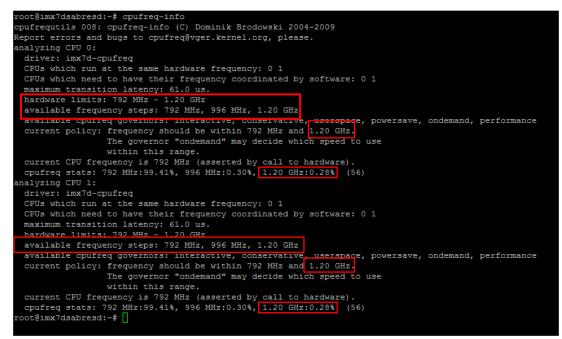


Figure 3. Verifying faster speeds

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Verifying faster speeds

This program reports that the additional frequency of 1.2 GHz is available for the Linux kernel to be selected, based on the CPU load.

Now that it is verified that the new speed is available, run the Dhrystone benchmark to see the difference in speed. The screenshots indicate that there is a performance difference of 20 % (which is expected). Note that the key item here is the difference and not the raw number.

This is the 1 GHz (original) DTB file:

root@imx7dsabresd:~# ./dry2				
Dhrystone Benchmark, Version C, Version 2.2				
Program compiled without 'register' attribute Using times(), HZ=100				
Trying 50000 runs through Dhrystone:				
Measured time too small to obtain meaningfu	ul results			
Trying 500000 runs through Dhrystone:				
Measured time too small to obtain meaningfu	ul results			
Trying 5000000 runs through Dhrystone:				
Measured time too small to obtain meaningfu	il results			
Trying 50000000 runs through Dhrystone:				
Microseconds for one run through Dhrystone:				
Dhrystones per Second:	3770739			
root@imx7dsabresd:~#				

Figure 4. 1 GHz DTB file

This is the 1.2 GHz DTB file:

root@imx7dsabresd:~# ./dry2				
Dhrystone Benchmark, Version C, Version 2.2				
Program compiled without 'register' attribute Using times(), HZ=100				
osing cimes(), no ico				
Trying 50000 runs through Dhrystone:				
Measured time too small to obtain meaningful	results			
Trying 500000 runs through Dhrystone:				
Measured time too small to obtain meaningful	results			
Trying 5000000 runs through Dhrystone:				
Measured time too small to obtain meaningful results				
Trying 50000000 runs through Dhrystone:				
Microseconds for one run through Dhrystone:	0.2			
Dhrystones per Second:	4541326			
root@imx7dsabresd:~#				

Figure 5. 1.2 GHz DTB file

When running the Dhrystone benchmark, run *cpufreq-info*. Figure 6 shows that the core is running at 1.2 GHz:

```
oot@imx7dsabresd:~# ./dry2 &
1] 888
Dhrystone Benchmark, Version C, Version 2.2
rogram compiled without 'register' attribute
sing times(), HZ=100
Trying 50000 runs through Dhrystone:
coot@imx7dsabresd:~# Measured time too small to obtain meaningful results
Trying 500000 runs through Dhrystone:
leasured time too small to obtain meaningful results
Trying 5000000 runs through Dhrystone:
feasured time too small to obtain meaningful results
Trying 50000000 runs through Dhrystone:
pufreg-info
pufrequtils 008: cpufreq-info (C) Dominik Brodowski 2004-2009
eport errors and bugs to cpufreq@vger.kernel.org, please.
analyzing CPU 0:
 driver: imx7d-cpufreq
 CPUs which run at the same hardware frequency: 0 1
 CPUs which need to have their frequency coordinated by software: 0 1
 maximum transition latency: 61.0 us.
 hardware limits: 792 MHz - 1.20 GHz
 available frequency steps: 792 MHz, 996 MHz, 1.20 GHz
 available cpufreq governors: interactive, conservative, userspace, powersave, ondemand, performance
 current policy: frequency should be within 792 MHz and 1.20 GHz.
                 The governor "ondemand" may decide which speed to use
                 within this range.
 current CPU frequency is 1.20 GHz (asserted by call to hardware).
 cpufreq stats: 792 MHz:99.44%, 996 MHz:0.06%, 1.20 GHz:0.50% (92)
nalyzing CPU 1:
 driver: imx7d-cpufreq
 CPUs which run at the same hardware frequency: 0 1
 CPUs which need to have their frequency coordinated by software: 0 1
 maximum transition latency: 61.0 us.
 hardware limits: 792 MHz - 1.20 GHz
 available frequency steps: 792 MHz, 996 MHz, 1.20 GHz
 available cpufreq governors: interactive, conservative, userspace, powersave, ondemand, performance
 current policy: frequency should be within 792 MHz and 1.20 GHz.
                 The governor "ondemand" may decide which speed to use
                 within this range.
 current CPU frequency is 1.20 GHz (asserted by call to hardware).
 cpufreq stats: 792 MHz:99.44%, 996 MHz:0.06%, 1.20 GHz:0.50% (92)
 oot@imx7dsabresd:~# Microseconds for one run through Dhrystone:
                                                                        0.2
                                               4545454
hrystones per Second:
```

Figure 6. cpufreq-info

5. Getting the patch

The patch is attached to this application note.

NOTE

This DTB file works with the NXP Linux release version 4.1.15_1.2.0.

6. Revision History

Table 1 summarizes the changes done to this document since the initial release.

Table 1. Revision history

Revision number	Date	Substantive changes
0	04/2017	Initial release

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