AN12409 i.MX 6/7/8 series USB Certification Guide Rev. 4 – 8 June 2023

Application note

Document Information

Information	Content
Keywords	i.MX 6/7/8, USB Certification Test, USB Compliance Test
Abstract	The purpose of this document is to describe how to perform USB Certification Test on the i.MX 6/7/8 series family of applications processor. This document constitutes the description of procedures, tools, and criteria for USB Compliance Test.



1 Introduction

The purpose of this document is to describe how to perform USB Certification Test on the i.MX 6/7/8 series family of applications processor. This document constitutes the description of procedures, tools, and criteria for USB Compliance Test.

2 Test preparing

This chapter lists all required materials for running the compliance test, including equipment, documents, software and so on.

2.1 Test board

Tests were performed on the following boards:

- MCIMX8 Series (Example)
- MCIMX7 Series
- MCIMX6 Series

2.2 Test environment

- DUT OS: Linux version 4.9.51 (Example)
- Test Bed Computer OS: WIN 10 and WIN 7

2.3 Test equipment

The following tables list the test equipment and the tests for which they are required. We used Keysight(Agilent) equipment for USB Electrical Test, but customer may use equipment from other vendors instead, such as Tektronix, Lecroy.

Table 1.	Digital	Oscilloscope,	Software,	and	Accessories
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Test Equipment			Tests					
Part Number	Description	Manufacturer	Embedded Host Super-Speed transmitter	Device Super-Speed transmitter	Embedded Host Hi-Speed	Device Hi- Speed	Low/Full Speed	
U7243B	USB 3.0 5 Gbps and 10 Gbps Transmitter Compliance Software	Keysight(Agilent)	1	1	N/A	N/A	N/A	
N5416A	USB 2.0 Automated Software	Keysight(Agilent)	N/A	N/A	1	1	1	
DSAV204A	Infiniium V-Series Oscilloscopes	Keysight(Agilent)	1	1	N/A	N/A	N/A	
DSO9254A	Digital real-time Oscilloscope	Keysight(Agilent)	N/A	N/A	1	1	1	
1169A	Differential Probe Amplifier	Keysight(Agilent)	N/A	N/A	1	1	N/A	
N5381A	Differential solder in Probe head	Keysight(Agilent)	N/A	N/A	1	1	N/A	
E2697A	Single-ended Probe	Keysight(Agilent)	N/A	N/A	N/A	N/A	3	
N2774A	Current probe	Keysight(Agilent)	N/A	N/A	N/A	N/A	1	
54855-67604	Precision BNC male to SMA 3.5 Female Adapter	Agilent	2	2	N/A	N/A	N/A	

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Table 1. Digital Oscilloscope, Software, and Accessories...continued

Test Equipment			Tests				
Part Number	Description	Manufacturer	Embedded Host Super-Speed transmitter	Device Super-Speed transmitter	Embedded Host Hi-Speed	Device Hi- Speed	Low/Full Speed
15443A	cable pair consists of two cables SMA (m) to SMA (m)	Keysight(Agilent)	2	2	N/A	N/A	N/A
HSEHET Board	High-Speed Embedded Host Electrical Test Board	Allion	N/A	N/A	1	N/A	N/A
Packet-Master USB-PET	USB Protocol and Electrical Tester	MQP	N/A	N/A	1	N/A	N/A
33401A	Digital Multimeter equivalent.	Keysight(Agilent)	N/A	N/A	1	1	1
P40A-1P2J	DC5V Power Supply	SunPower	N/A	N/A	1	1	1

Table 2. Test Fixtures for USB Electrical Test

Test Fixture			Tests					
Part Number	Description	Manufacturer	Embedded Host Super-Speed transmitter	Device Super-Speed transmitter	Embedded Host Hi-Speed	Device Hi- Speed	Low/Full Speed	
5M 94V-0 3913-01	USB 3.0 Device Test Fixture-1	Intel	N/A	1	N/A	N/A	N/A	
5M 94V-0 3913-01	USB 3.0 Host Test Fixture-1	Intel	1	N/A	N/A	N/A	N/A	
5M 94V-0 3913-01	USB 3.0 Device Test Fixture-2	Intel	N/A	1	N/A	N/A	N/A	
5M 94V-0 3913-01	USB 3.0 Host Test Fixture-2	Intel	1	N/A	N/A	N/A	N/A	
5M 94V-0 4316 16-15	USB 3.0 Device Test Fixture-1C	Intel	N/A	1	N/A	N/A	N/A	
5M 94V-0 4316 16-16	USB 3.0 Host Test Fixture-1C	Intel	1	N/A	N/A	N/A		
E2649-66401	Device High-Speed Signal Quality Test Fixture	Keysight(Agilent)	N/A	N/A	N/A	1	N/A	
E2649-66402	Host High-Speed Signal Quality Test Fixture	Keysight(Agilent)	N/A	N/A	1	N/A	N/A	
E2649-66405	USB 2.0/3.0 Droop/Drop TestFixture	Keysight(Agilent)	N/A	N/A	N/A	N/A	1	
E2646A/B	USB Inrush (SQiDD) Test Fixture	Keysight(Agilent)	N/A	N/A	N/A	N/A	1	
E2649-66403	Receiver Sensitivity Test Fixture	Keysight(Agilent)	N/A	N/A	1	N/A	N/A	

Table 3. Digital Signal Generator for Receive Sensitivity Test

Required Equipment			Tests				
Part Number	Description	Manufacturer	Embedded Host Super-Speed transmitter	Device Super-Speed transmitter	Embedded Host Hi-Speed	Device Hi- Speed	Low/Full Speed
82357A	USB/GPIB interface	Keysight(Agilent)	N/A	N/A	N/A	1	N/A
81130A	Pulse/Pattern generator	Keysight(Agilent)	N/A	N/A	N/A	N/A	N/A
8493C	6 dB attenuators	Keysight(Agilent)	N/A	N/A	N/A	1	N/A
8120-4948 or equivalent	50 ohm coaxial cable with male SMA connectors at both ends	Keysight(Agilent)	N/A	N/A	N/A	2	N/A

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Required Equipment	Tests				
Description	Embedded Host Super-Speed transmitter	Device Super-Speed transmitter	Embedded Host Hi-Speed	Device Hi- Speed	Low/Full Speed
5 m USB cable (any listed on USB-IF website)	N/A	N/A	1	1	6
1.5 m USB cable (any listed on USB-IF website)	N/A	N/A	1	N/A	N/A
1 m USB cable (any listed on USB-IF website)	N/A	N/A	N/A	N/A	1
4" USB cable(any listed on USB-IF website)	N/A	N/A	1	1	1
Hi-Speed USB Hub (any listed on USB-IF website)	N/A	N/A	4	N/A	4
Full-Speed USB Hub (any listed on USB-IF website)	N/A	N/A	1	N/A	1
Super-Speed USB Hub (any listed on USB-IF website)	1	1	N/A	N/A	N/A
High-Speed USB Device (any listed on USB-IF website)	N/A	N/A	1	1	N/A
Full-Speed USB Device (any listed on USB-IF website)	N/A	N/A	N/A	N/A	1
Low-Speed USB Device (any listed on USB-IF website)	N/A	N/A	N/A	N/A	1

Table 4. Miscellaneous cables and devices



Figure 1. E2649 High-Speed Test Fixture Set

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Figure 3. 5M 94V-0 Super Speed Test Fixture Set

2.4 Test software

Table 5. Test software used for USB Certification Test

Name	Version	Description
USBET20	1.20	USB Electrical Analysis Tool

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Name	Version	Description
USBHSET	1.2.2.1	Window-based utility Tool used to initiate test modes
USB20CV	1.4.11.0	USB 2.0 Command Verifier for USB 2.0 Device Framework testing
USB30CV	1.1.2.0	USB 3.0 Command Verifier for USB 3.0 Device Framework testing
GraphicUSB	4.47	Test software for PET Test

Table 5. Test software used for USB Certification Test...continued

Note: Download the latest software from the websites of USB-IF and MQP.

2.5 USB-IF required tests

Devices which support features of [USB 3.0] and [USBOTG&EHv2.0] shall undergo additional testing beyond the tests described in this document. This additional testing is a subset of existing tests for USB peripherals and USB host controllers.

<u>Table 6</u> describes which tests are required for full USB-IF certification by an EH with a Standard-A, Type C, or Micro-AB connector.

<u>Table 7</u> describes which tests are required for full USB-IF certification by a Device with a Micro-AB, Micro-B connector, or Type C.

Table 6. Embedded Host test requirements

USB-IF test ► USB speed ▼	Enhanced SS Electrical	Automated Test Ch6	Manual Test Ch7	Drop/Droop	DS LS SQT	DS FS SQT	DSHS Electrical
Super-Speed Host	/*						
High-Speed Host		✓	✓	✓ / **	*	*	✓
Full-SpeedHost		√	√	✓ / **	*	*	
Low-Speed Host		1	√	✓ / **	1		

Table 7. Device test requirements

USB-IFtest ► USB speed ▼	Enhanced SS Electrical	IOP Goldtree	Avg Current	Automated Test Ch6	Manual Test Ch7	USBCV	Back- Voltage	Inrush Current	US LS SQT	US FS SQT	USHS Electrical
SS Device	✓ / *										
FS Device		1	1	*	1	1	1	1	*	*	
HS Device		√	1	*	1	√	1	1	*	*	1

Note:

- USB-IF allows Embedded Host to use the Micro-AB receptacle in 2012.
- For peripheral, if the silicon is only compliant with the general USB 2.0 spec, it is recognized as standard USB2.0 peripheral, Automated Test Ch6 must not be launched. If the silicon is compliant to the supplement of OTG and EH Rev. 2.0 (with OTG descriptor in the declaration), the device is recognized as B-device, so Automated Test Ch6 must be launched.

The following symbols are used in these tables: ✓ Always required * Required if feature is supported ** Required if there are multiple downstream ports.

2.6 Five avenues to certify

There are five avenues for certifying a product with the USB-IF.

- 1. Participate in a USB-IF Sponsored Compliance workshop (USB-IF Member Company Benefit Only)
- 2. Attend an Authorized Independent Test Lab

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- 3. Participate in the USB-IF Qualification by Similarity program
- 4. Attend the USB-IF Platform Interoperability Lab (USB-IF Member Company Benefit Only)

OEM Arrangements

Note: All companies seeking to use the USB-IF logos on their product must have a valid USB-IF Trademark License Agreement on file with the USB-IF and the product must be certified.

2.7 Register the product in USB-IF

To attend a test lab, a vendor must first Register their product with the USB-IF. The USB-IF collects a variety of registration data to categorize the product and ensure that the appropriate testing is performed. Once all registration questions are answered and appropriate documentation submitted, a vendor is able to select an ITL that is capable of testing the product type categorized by the registration information. An email will be sent to you, the ITL and USB-IF Administration confirming the selection of ITL and registration. Once the Product has been accepted for testing by an ITL a Test ID (TID) will be assigned.

- 1. Register and login your account at https://cms.usb.org/register-product, before that make sure your company is a member of USB-IF;
- Click My Account and then click Add a Product to enter the Product Register page, select a product type for your product, as shown in <u>Figure 4</u>. If you do not know what kind of Product Type you should choose, consult your Test Lab;



- 3. Fill in the detailed information of your product, including Marketing Name, Revision, Product Category, contact window and so on.
- 4. Wait for USB-IF to approve it.

Note: Make sure that the Marketing Name is the same as the product name in checklists. Use the VID of your company registered on USB-IF and not the one of your USB silicon providers. **The VID of NXP product on USB-IF is 1fc9 in hex or 8137 in decimal.** The current membership list will be available here soon. You can download the whole <u>Company List</u> using the following link: <u>https://usb.org/members</u>

2.8 Compliance test reference documents

Get to know the whole environment settings and detailed test steps of USB Compliance Test, study the following documents:

Universal Serial Bus 3.0 Specification, revision 1.0(USB-IF, 2008)

- Universal Serial Bus 3.1 Specification, revision 1.0(USB-IF, 2013)
- Universal Serial Bus Implementers Forum Full and Low Speed Electrical and Interoperability Compliance Test Procedure Version 1.3 (USB-IF, 2004)
- USB On-The-Go and Embedded Host Automated Compliance Plan for the On-The-Goand Embedded Host Supplement Revision 2.0 Version 1.2 (USB-IF, 2012)
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification Revision 2.0 Version 1.1A (USB-IF, 2012)
- USB-IF USB 2.0 Certification Mandatory Test Matrix (USB-IF, 2019)
- Universal Serial Bus Specification Revision 2.0 (USB-IF, 2000)
- USB 2.0 Electrical Compliance Test Specification Version 1.07(USB-IF, 2019)
- Embedded High-speed Host Electrical Test Procedure Revision 1.01 (USB-IF, 2006)
- Universal Serial Bus Implementers Forum Device Hi-Speed Electrical Test Procedure For Agilent Infiniium Revision1.2 (USB-IF, 2003)
- Universal Serial Bus Implementers Forum Host Hi-Speed Electrical Test Procedure For Agilent Infiniium Revision1.3 (USB-IF, 2004)
- Agilent N5416A USB 2.0 Compliance Test Option (Agilent, 2013)
- Gold Suite Summary Test Procedure V1.35 Draft (USB-IF)
- Allion HSEHET User Manual (Allion, 2012)
- Universal Serial Bus Revision 2.0 USB Command Verifier Compliance Test Specification Revision 1.2 (USB-IF, 2003)
- Universal Serial Bus Revision 3.1 USB Command Verifier Compliance Test Specification Revision 0.7 (USB-IF, 2015)
- Universal Serial Bus Mass Storage Class Compliance Test Specification Revision 1.1 (USB-IF, 2014)
- i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Industrial Products REV 0 (NXP, 2018)
- i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Consumer Products REV 0 (NXP, 2018)
- i.MX 8M Dual / 8M QuadLite / 8M Quad Product Lifetime Usage REV 0 (NXP, 2018)
- Quick Start Guide i.MX 8M Quad Evaluation Kit REV 0 (NXP, 2018)
- i.MX 8X Family of Applications Processors REV 0 (NXP, 2018)
- i.MX 7ULP Applications Processors REV 0 (NXP, 2018)
- i.MX 8M Mini Family of Applications Processors REV 0 (NXP, 2018)

3 Electrical test procedure

3.1 Legacy USB compliance tests

- Upstream Full Speed Signal Quality Test
- Back-Voltage Test
- Device Inrush Current Test
- Downstream Full Speed Signal Quality Test
- Downstream Low Speed Signal Quality Test
- Host Drop Test

3.1.1 Upstream full speed signal quality test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 5</u>, and make sure you set the Test Type configuration option to "Full-Speed Far End" before running the test. Connect the equipment and test fixture as shown in <u>Figure 6</u> below.
- 2. Invoke the HS Electrical Test Tool software on the Computer, select **Device**, and click the **TEST** button to enter the Device Test menu, see Figure 7.
- 3. On the Device Test Menu of the HS Electrical Test Tool software, click **Enumerate Bus** once. All devices attached to the host controller should appear in the device enumeration list.
- 4. Highlight the device under test and select **LOOP DEVICE DESCRIPTOR** from the Device Command drop down menu. Click **[EXECUTE]** once.
- 5. Click **Run Tests** in the USB Automated Test Software on Oscilloscope. After the test is finished, you can view the report in **HTML Report** page.



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	JSB-IF HS Electrical Test Tool		
	Select Type Of Test	Select Host Controller For Use In Testing	
	Device	PCI bus 5, device 0, function 2 2 Ports	
	C Hub		
	C Host Controller/System		
	()	Exit	
Figure 7. Electrical Test	t Tool Main Menu		

HS Electrical Test Tool - Device Test	
Select Device NONE VID 0x4b4, PID 0x6560, Address 1, Port 5 VID 0x58f, PID 0x9254, Address 2, Port 5 VID 0x4b4, PID 0x6560, Address 3, Port 5 VID 0x4b4, PID 0x6560, Address 4, Port 5 VID 0x4b4, PID 0x6560, Address 5, Port 5 VID 0x46d, PID 0xc016, Address 6, Port 5	Device Control Device Command Device Address NONE TEST_J TEST_K TEST_SE0_NAK TEST_PACKET SUSPEND
Enumerate Bus	RESUME RESET DEVICE DESCRIPTOR LOOP DEVICE DESCRIPTOR SET ADDRESS ENABLE WAKEUP DISABLE WAKEUP
igure 8. Device Control Command	SINGLE STEP SET FEATURE SINGLE STEP GET DEV DESC

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Note:

- 1. *i.MX* is enumerated as an MSC device, Low Speed upstream is not supported. And it is ok to measure the upstream full speed EYE without the 5 tiers of hubs since it has no effect on the signal integrity itself.
- 2. High-speed electrical tests are performed either near-end or far-end depending on the configuration of the product. The terms "near-end" and "far-end" are based on which end of the cable the test fixture is attached in relation to the device being tested.

All HS peripherals with a B-receptacle are tested near-end (at the peripheral's receptacle). HS devices that have a captive cable are tested far-end (at the end of the captive cable). Unlike full-speed electrical tests, which are always performed far-end, the length of the cable used in HS electrical tests is not important. High-speed electrical tests of downstream ports on hosts and hubs are always performed near-end.

- See the detailed explanation of Far End and Near End in USB-IF Compliance Updates, <u>http://compliance.usb.org/index.asp?UpdateFile=Electrical&Format=Standard#8</u>
- 3. The VID of NXP product in USB-IF is 1fc9 in hex or 8137 in decimal.
- 4. A Full-Speed Hub here can force the downstream devices operating in Full-Speed Mode.

3.1.2 Back-voltage test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 11.
- Connect power supply to DUT and connect the device upstream port to the back-voltage test fixture using a known good USB cable as shown in <u>Figure 12</u>. Measure and record DC voltages on **VBUS**, **D+** and **D-**. Voltages should all be less than or equal to 400 mV. Any voltages greater than 400 mV will be recorded as a failure.

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- Plug DUT into a known good host, and verify proper enumeration. Unplug USB cable from the host and reconnect the USB cable to the back-voltage test fixture. Measure and record the DC voltages of VBUS,D + and D-. All voltages must be less than or equal to 400 mV. Any voltages greater than 400 mV will be recorded as a failure.
- 4. After the test is finished, you can view the report in **HTML Report** page.

) 🖼 🖬 🗠		
Task Flow _	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report	
Set Up	Device Suspend/Resume/Reset Timing Device Test J/K, SE0_NAK Device Receiver Sensitivity Device Receiver Sensitivity	^
Select Tests	Inrush Current Test O Upstream Full Speed Signal Quality and Transition Time Test O Upstream Low Speed Signal Quality and Transition Time Test O Rack-voltage Test Before Enumerate	
Configure	 ✓ ○ VBUS Before Enumerate ✓ ○ D + Before Enumerate ✓ ○ D - Before Enumerate 	Щ
Connect		
	✓ O D+After Enumerate	~
\mathbf{V}	Test Group: Back-voltage Test Before Enumerate	
Run Tests	Description: Measures the voltages of VBUS, D+ and D- at upstream port of device to test that device does not supply VBUS at its upstream port or provide power to D+/D	^

Figure 11. Automated Test Software setting for Back-Voltage Test

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Table 8. Back-Voltage Test Record

Test Point	DC Voltage Before enumeration(mV)	DC Voltage after enumeration and removal(mV)	Expected Value (VDC)
VBUS	72	72	≤ 400 mV
D+	0	0	≤ 400 mV
D-	0	0	≤ 400 mV

3.1.3 Device inrush current test

The USB 2.0 Spec allows a maximum capacity of 10uF and therefore a maximum Inrush of 50uC. It is required to have at least a 1uF of capacity in order to make ADP detection possible. The DUT cannot consume more that 100 mA during this 100 ms of the starting up. Inrush current should be measured for a minimum of 100 milliseconds after attach.

Test Instructions:

- 1. Connect the equipment and test fixture as shown in <u>Figure 13</u>, use the current probe to capture the **VBUS** current waveform, make sure that the probe direction is the same.
- 2. Attach the DUT to SQiDD board, then place the switch on SQiDD board to the discharge position (opposite the ON position).
- 3. Disconnect the DUT from SQiDD board, then place the switch on SQiDD board to the ON position.
- 4. Adjust the oscilloscope settings to match the current test requirement: time base 50 ms/div, Vertical resolution 500 mA/div, sample rate >1MS/s.
- 5. Reconnect the DUT to SQiDD board in order to capture the inrush current waveform, then save the waveform as a *.wfm or *.csv.
- Use the analysis software "USBET20" on Computer to analyze the waveform file, then a page shows the test result as shown in <u>Figure 15</u> below. The failures for Inrush mostly occur due to a too large capacity between VBUS and GND.

Note:

Note: When doing the measurement make sure that you calibrate the current probe to 0 mA before doing the measurement since a current probe will get quickly a DC offset that will result in a wrong measurement.

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THE LISPETTO LISP 2.0 Electrical Test Tool 1.20.00	
USBET20 - USB 2.0 Electrical rest TOOL 2.20.00	
Device/Host SQ Hub DS SQ Inrush Current	
Inrush Current Data	
C:\Work\IMX6\Documents\Compliance Test report\USB	
	Test
Inrush Current Data	
tek0001CH_4_2.csv	Browse
Supply Voltage	
5	
Figure 14. USBET20 operation interface	

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3.1.4 Downstream full speed signal quality test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 16</u>, and make sure you set the Test Type configuration option to "Full-Speed Far End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 17.
- 3. Click **Run Tests**, after the test is finished, you can view the report in **HTML Report** page.

Set Up Select Tests Configure Connect	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report Image: Configure O USB Tests Image: Configure O Hi-Speed Image: Configure O Hi-Speed Image: Configure O Hi-Speed Image: Configure O Host Full Speed Signal Quality and Transition Time Test Image: Configure Image: Configure Image: Configure O Host Full Speed Signal Quality and Transition Time Test Image: Configure Image: Configure Image: Configure O Host Full Speed Signal Quality and Transition only) Image: Configure Image: Configure Image: Configure Image: Configure O Host Low Speed Signal Quality and Transition Time Test Image: Configure Image:





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3.1.5 Downstream low-speed signal quality test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 20, and make sure you set the Test Type configuration option to "Low-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 21.
- 3. Click **Run Tests**, after the test is finished, you can view the report in **HTML Report** page.







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3.1.6 Host drop test

The Drop test is a measure of a Host/Hub's ability to host full load current while keeping the output voltage above spec. To perform this test, **VBUS** is measured with all downstream ports loaded with 500 mA loads (for host and self-powered hubs). The lowest value measured across all ports must be between 4.75 V and 5.5 V for host and self-powered hubs.

The Droop test is a transient test on adjacent ports. When a device is hot plugged into another port, the droop in VBUS supplied to a port must be less than or equal to 330 mV for host, self-powered, and bus powered hubs. If there is only one Host Port on board, this test is not needed.

Test Instructions:

- 1. First, power the test fixture from your Computer or a USB charger. The DS1 LED should illuminate (green LED).
- 2. There are several switches/buttons used for general control of the test fixture. They include:
 - Switch S5 allows you to select either the Droop or Drop test.
 - Switch S4 allows you to select either the 100 mA or 500 mA load.
 - Press and hold S1 for at least 3 seconds to turn on the test fixture.
 - While pressing and holding S2, press S1 to turn off the test fixture .
 - When the fixture is on, press S2 enables the left port.
 - When the fixture is on, press S1 enables the right port.

- 3. Measure VBUS at downstream USB connector with no cable or device inserted (no load), then record it as $V_{\text{NL}}.$
- 4. Measure VBUS at downstream USB connector with 500 mA load, then record it as V_{LOAD} .

Table 5. Host blop fest Recold			
Item	Port01_Voltage	Expected Value (VDC)	
V _{non-load}	5.19 V	4.75 V <= VBUS <= 5.5 V	
V _{Load}	5.083 V	4.75 V <= VBUS<= 5.5 V	
V _{drop}	107 mV	≤ 750 mV	
V _{droop}	NA	≤ 330 mV	

Table 9. Host Drop Test Record

Note: USB-IF has published an ECN to increase the maximum voltage on VBUS from 5.25 V to 5.5 V in August 2014. So the maximum voltage is 5.5 V now.

Keep the following items in mind for drop test:

a) When doing the measurement take the cable resistance/voltage drop into account what can be significant with high currents. For example, if you have 0.25 Ohm resistance for cable and connectors and a current of 500 mA you will have a voltage drop of 0.125 V. Therefore the measurement should be done as near to the A-Receptacle as possible and if accessible you can measure at the A-receptacle **VBUS/GND** soldering pad. Measuring at the A-receptacle is the location that the USB specifications define to measure but since it is often too difficult to access you probably use a fixture and maybe also a cable in between, be aware that these will give some additional voltage drop.

b) During testing use the power supply that is used in the market and when changing the power supply re-test **VBUS** drop.



3.2 Device high-speed signal test

- Device High-Speed Signal Quality Test
 - EL_2: Data Rate Test
 - EL_4, EL_5: Eye Pattern Test

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- EL_6: Rise and Fall Time Test
- EL_7: Non-Monotonic Edge Test
- Device Packet Parameters Test
 - EL_21: Sync Field Length Test
 - EL_25: EOP Length Test
 - EL_22: Measure Inter-packet Gap Between First and Second Packets
 - EL_22: Measure Inter-packet Gap Between Second and Third Packets
- Device CHIRP Timing Test
 - EL_28: Measure Device CHIRP-K Latency
 - EL_29: Measure Device CHIRP-K Duration
 - EL_31: Device Hi-Speed Terminations Enable and D+ Disconnect Time
- Device Suspend/Reset/Resume Timing Test
 - EL_38, EL_39: Device Suspend Timing Response
 - EL_40: Device Resume Timing Response
 - EL_27: Device CHIRP Response to Reset from Hi-Speed Operation
 - EL_28: Device CHIRP Response to Reset from Suspend
- Device Test J/K, SE0_NAK Test
 - EL_8: Device J Test
 - EL_8: Device K Test
 - EL_9: Device SE0_NAK Test
- Device Receiver Sensitivity Test 14
 - EL_18: Minimum SYNC Field
 - EL_17: Receiver Sensitivity Test
 - EL_16: Squelch

Note:

- For High-Speed Device Test, install HS Electrical Test Tool software on Computer, which can set DUT into specific test pattern.
- To study the detailed description of the test items, you can read this document "USB 2.0 Electrical Test Specification" on <u>https://usb.org/document-library/usb-20-electrical-test-specification</u>.
- Device Receiver Sensitivity Test need additional equipment: Digital signal generator (for example Agilent 81130A) and related accessories.

3.2.1 HS device electrical test limits

Table 10. HS device electrical test limits

Test Name	Pass Limits
EL_2 Data Rate	Within 480 Mb/s +/-0.05%
EL_4 Eye Pattern(Without captive cable)	Must meet Template 1 transform waveform requirements at TP3
EL_5 Eye Pattern15 (With captive cable)	Must meet Template 2 transform waveform requirements at TP2
EL_6 Device Rise/Fall Time	>500 ps
EL_7 Device Non-Monotonic Edge Test	Must have monotonic data transitions over the vertical openings
EL_21 Device Sync Field Length Test	32 bits, 65.62 ns <= VALUE <= 67.700 ns
EL_25 Device EOP Length Test	8 bits, 15.600 ns <= VALUE <= 17.700 ns
EL_22 Measure Interpacket Gap Between Second and Third Packets	16.640 ns <= VALUE <= 399.400 ns
EL_22 Measure Interpacket Gap Between First and Second Packets	16.640 ns <= VALUE <= 399.400 ns
EL_28 Measure Device CHIRP-K Latency	2.500 µs <= VALUE <= 6.000000 ms
EL_29 Measure Device CHIRP-K Duration	1.000 ms <= VALUE <= 7.000 ms

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Table 10. It's device electrical test limitscontinued				
Test Name	Pass Limits			
EL_31 Device Hi-Speed Terminations Enable and D+ Disconnect Time	1 ns <= VALUE <= 500.000 μs			
EL_40 Device Resume Timing Response	Must transition back to high-speed operation within two-bit times from the end of resume time signaling			
EL_27 Device CHIRP Response to Reset from Hi-Speed Operation	3.100 ms <= VALUE <= 6.000 ms			
EL_28 Device CHIRP Response to Reset from Suspend	2.500 μs <= VALUE <= 6.000000 ms			
EL_38 EL_39 Device Suspend Timing Response	3.000 ms <= VALUE <= 3.125 ms			
EL_8 Device J Test	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV			
EL_8 Device K Test	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV			
EL_9 Device SE0_NAK Test	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV			
EL_18 Minimum SYNC Field	Detect the end of the SYNC field within 12-bit times			
EL_17 Receiver sensitivity	VALUE <= +/- 200 mV			
EL_16 Squelch	VALUE >= +/- 100 mV			

Table 10. HS device electrical test limits ... continued







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Figure 26. Template 1 for Device without a captive cable

3.2.2 Device high-speed signal quality test

These tests measure the ability of transmitters to do valid high-speed signaling. High-speed signal quality is measured on upstream ports. A high-speed scope with differential probes is used. Signaling data is captured with the scope and then translated to an eye pattern. The signal quality eye patterns obtained from the measurements must agree with the transmit eye patterns in the USB 2.0 Specification.

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 27, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 28.
 - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the Device Hi-speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
 - Connect the [INIT PORT] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
 - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
- 3. Invoke the HS Electrical Test Tool software on the Hi-Speed Electrical Test Bed Computer. Select Device and click the **TEST** button to enter the Device Test menu. The DUT should be enumerated with the device's VID shown together with the root port in which it is connected.

- 4. Select TEST_PACKET from the Device Command drop down menu and click EXECUTE. It forces the DUT to transmit test packets continuously.
- 5. Click **Run Tests** button of Automated Test Software on Oscilloscope.
- 6. Place the Test Switch (S1) in the **TEST** position according to the requirement of Automated Test Software. Verify that the yellow TEST LED is lit. You should see the transmitted test packet on the oscilloscope as Figure 31.
- 7. When the Testing Complete dialog appears, click OK. The Results tab shows the test results, and the HTML Report shows the whole report.



Figure 27. Device HS Signal Quality Test



HS Electrical Test Tool - Device Test Select Device NONE VID 0v4b4, PID 0v5820, Address 1, Part 5	Device Control Device Command Device Address
	TEST_PACKET Status Window
Enumerate Bus	EXECUTE Return To Main

н	5 Electrical Test Tool - Device Test			
	Select Device NONE VID 0x4b4, PID 0x6830, Address 1, Port 5	Device Control Device Command TEST_PACKET Status Window	Device Address	
	Enumerate Bus	EXECUTE	Return To Main	
Figure 30. Test_Packet F	or Eye Diagram Test			-



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3.2.3 Device packet parameters test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 33</u>, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 28.
 - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the Device Hi-speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
 - Connect the [INIT PORT] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
 - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
- 3. Reboot the device to restore the USB device to normal operation.
- Click Enumerate Bus on the menu of the HS Electrical Test Tool. Using the oscilloscope, verify the SOF (Start of Frame) packets are being transmitted on the port under test. You may need to lower the trigger level to somewhat below 400 mV.

- 5. Select Single Step Set Feature from the Device Command window. Click EXECUTE once. Oscilloscope will measure the sync field length (number of bits) of the third (from device) packet (EL_21), EOP (End of Packet) width (number of bits) of the third packet (EL_25), inter-packet gap between the second (from host) and the third (from device in respond to the host's) packets (EL_22), as shown in Figure 35 to Figure 37.
- In the Device Test menu of the HS Electrical Test Tool, click STEP once again. This is the second step of the two-step Single Step Set Feature command. Oscilloscope will measure the inter-packet gap between the first (from host) and the second (from device in respond to the host's) packets (EL_22), as shown in Figure 38.
- 7. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

USB Test	t USB Device *	
File View	Tools Help	
🗅 🚅 🖬 🔤		
Task Flow	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report	
Set Up Select Tests Configure	USB Tests Hi-Speed Device Hi-Speed Device Hi-Speed Signal Quality Test Device Packet Parameters O EL_21 Device Sync Field Length Test O EL_25 Device EOP Length Test O EL_22 Measure Interpacket Gap Between Second and Third Packets O EL_22 Measure Interpacket Gap Between First and Second Packets Device CHIRP Timing Device Suspend/Resume/Reset Timing Device Test J/K, SE0_NAK Device Receiver Sensitivity	THE STREET
Connect	E O Low and Full Speed	~
$ \Psi $	Test Group: Device Packet Parameters	
Run Tests	Description: Measures sync field length, end of packet (EOP) width, and interpacket gap of transmitted packets.	^
		~
Figure 33. Device	HS Packet Parameters Test	



HS Electrical Test Tool - Device Test		
Select Device	Device Control	
NONE	Device Command	Device Address
VID 0x4b4, PID 0x6560, Address 1, Port 5	NONE NONE TEST_J TEST_K TEST_SE0_NAK TEST_PACKET SUSPEND	
Enumerate Bus	RESUME RESET DEVICE DESCRIPTOR LOOP DEVICE DESCRIPTOR SET ADDRESS ENABLE WAKEUP	eturn To Main
igure 35. Single Step Set Feature for Packet Paran	DISABLE WAKEUP SINGLE STEP SET FEATURE SINGLE STEP GET DEV DESC neters Test	


Figure 36. EL_21 Device Sync Field Length Waveform



Figure 37. EL_25 Device EOP Length Waveform

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Figure 38. EL_22 Device Inter-packet Gap (Between Second and Third Packets) Waveform

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HS Electrical Test Tool - Device Test Select Device NONE VID 0x4b4, PID 0x6560, Address 1, Port 5	Device Control Device Command SINGLE STEP SET FEATU Status Window Operation Successful	Device Address
Enumerate Bus	Step Re	eturn To Main
Figure 39. Single Step Set Feature - Second Step		

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3.2.4 Device CHIRP timing test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 41 below, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 42 below.
 - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
 - Connect the [INIT PORT] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
 - Attach the single end probes on Channel 2 to D- of TP2, Channel 3 to D+ of TP2.
- 3. Reboot the device to restore the USB device to normal operation.
- 4. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Oscilloscope will capture and measure the Chirp handshake as shown in Figure 43 below.

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5. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

🛎 USB Test	USB Device *	×
File View T	ools Help	
🗅 🚅 🖬 🔤	¤⊼ r @ @ <mark>0</mark>	
Task Flow _	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report	
Set Up		^
Select Tests	O Device Hi-Speed Signal Quality Test O Device Packet Parameters O Device CHIRP Timing	
	 EL_28 Measure Device CHIRP-K Latency EL_29 Measure Device CHIRP-K Duration EL_31 Device Hi-Speed Terminations Enable and D+Disconnect Time 	III
	Device Suspend/Resume/Reset Timing O Device Test J/K, SE0_NAK O Device Receiver Sensitivity	
Connect	C Low and Full Speed O Inrush Current Test O Inrush Current Test	
\vee	Test Group: Device CHIRP Timing	
Run Tests	Description: Tests device CHIRP K and CHIRP J timing response.	^
		*
Figure 41. Device C	hirp J/K Test	



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Figure 43. Device CHIRP J/K Waveform

3.2.5 Device Suspend/Reset/Resume timing test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 44 below, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Fig3-38 above.
 - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
 - Connect the [INIT PORT] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
 - Attach the single end probes on Channel 2 to D- of TP2, Channel 3 to D+ of TP2.
- 3. Reboot the device to restore the USB device to normal operation.
- 4. Click Enumerate Bus on the menu of the HS Electrical Test Tool. Choose the right device, Select SUSPEND from the Device Command drop down menu, then click EXECUTE once to place the device into suspend. The captured suspend transition should appear as in <u>Figure 45</u> below.
- 5. Select **RESUME**, then click **EXECUTE** once to resume the device from suspend. The captured resume transition should appear as in Figure 47 below.

- 6. Select **RESET**, then click **EXECUTE** once to reset the device operating in high speed. The captured transition should appear as Figure 49 below.
- Select SUSPEND, and click EXECUTE to place the device into suspend once again. Then select RESET
 and click EXECUTE once to reset the device from suspend. The captured transition should appear as
 Figure 51 below.
- 8. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

USB Test	t USB Device *	
File View	Tools Help	
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Task Flow _	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report	
Set Up Select Tests Configure	 USB Tests Hi-Speed Device Hi-Speed Device Hi-Speed Signal Quality Test Device Packet Parameters Device CHIRP Timing Device Suspend/Resume/Reset Timing EL_38 EL_39 Device Suspend Timing Response EL_40 Device Resume Timing Response EL_27 Device CHIRP Response to Reset from Hi-Speed Operation EL_28 Device CHIRP Response to Reset from Suspend Device Test J/K, SE0_NAK Device Receiver Sensitivity 	
Connect	⊡□ O Low and Full Speed	~
V	Test Group: Device Suspend/Resume/Reset Timing	
Run Tests	Description: Tests device suspend, resume and reset timing response.	^
		V

HS Electrical Test Tool - Device Test		
Select Device NONE VID 0x4b4, PID 0x6830, Address 1, Port 5 Enumerate Bus	Device Control Device Command SUSPEND NONE TEST_J TEST_K TEST_SE0_NAK TEST_PACKET SUSPEND RESUME RESET DEVICE DESCRIPTOR LOOP DEVICE DESCRIPTOR SET ADDRESS ENABLE WAKEUP DISABLE WAKEUP	Device Address
Figure 45. Device Suspend Command	SINGLE STEP SET FEATURE SINGLE STEP GET DEV DESC	

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File	Control	Setup	Measure	Analyze	Utilities	Help		7:54	1 AM
	50.0 MSa/	s 262 k	:pts	~	~~~~	<u></u> _	2	1 0	
	0 ⁰		2	On 500 mV/	\approx) On 500 mV/	1 <u>2</u> 0 P	n	
1	USB S	uspend	Fiming Test						
	Instruct	ions: SU cation: -3	SPEND DUT ImS to 3 125	F, measure f mS_Becor	irom END o d Results	of last SOF to r	ising edge of l	=S J	
	Load N	lext Step	Setup: RES	UM2&3.set	41 (Courto.				←T
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1				400		590000000 ma		2 COD V	Ť
More (1 of 2)	Markers			400 Дз/	<u> </u>	.3300000000 ms		2.000 V	
Delete	mancers	Codico		A(2) =	X -3.10273129	Ү 5 ms – 4 r	٩V		13
All				B(3) = A =	2.72344 µ 3.1054546	s 2.9 9 ms 2.9	951 V 954 V		
Figuro	46 Dovice	Success	Moveform						_

Figure 46. Device Suspend Waveform

HS Electrical Test Tool - Device Test		
Select Device	Device Control	
NONE	Device Command	Device Address
VID 0x404, PID 0x6830, Address T, Port 5	RESUME NONE TEST_J TEST_K TEST_SE0_NAK TEST_PACKET	0
Enumerate Bus	SUSPEND RESUME DEVICE DESCRIPTOR LOOP DEVICE DESCRIPTOR SET ADDRESS	eturn To Main
	ENABLE WAKEUP DISABLE WAKEUP SINGLE STEP SET FEATURE SINGLE STEP GET DEV DESC	
Figure 47. Device Resume Command		

2.00 GSa/s 262 kpts · · · · · · · · · · · · · · · · · · ·	
이 만 <u>이 만 500 mV/ 적</u> 이 만 500 mV/ 적 이 만	
	L
USB Resume Timing Test	
Instructions: RESUME DUT; Verify SOF occurs after leaving K state; Record results.	
Load Next Step Setup: RSTFHS2&3.set	
	I
(1of 2)	
Delete All	

HS Electrical Test Tool - Device Test		
Select Device NONE VID 0x4b4, PID 0x6830, Address 1, Port 5 Enumerate Bus	Device Control Device Command	Device Address
rigure 43. Device Reset Command		

File	Control	Setup	Measure	Analyze	Utilities	Help	7:57 AM
	25.0 MSa/	's 262 k	ots 📕		~~~~		1 🖲 🗕
	0 ⁰		0	On 500 m V/	~ (3) 📴 500 mV/ 😤	0n
1	USB R	eset Fror	n Hi-Speed	Timing Test	t A× ≟		
	Instruct	ions: RE cation: 3	SET DUT; n .1 mS to 6 m	neasure fror S: Record th	n beginnin 1e result.	g of last SOF to Chir	р-К.
	Load N	lext Step	Setup: RST	RSUS2&3.9	set	Device	
ŢŢ					+	CHIRP-K	
+]+ ₁∕↔					··••··		
1 n							
• • ^					+		
±-┐ └			1111111111				← I
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<u>+</u>							
More	T [5 E	1.00 ms/	∿ ∿ <mark>↑</mark> 🛃	3.000000000 ms ┥ 0	▶ 1 670 mV 🔶 ↑
(1 of 2)	Markers	Scales			V	v	2
Delete All				$A \longrightarrow (2) = B \longrightarrow (2) =$	-3.2909192 -10.18 ns	'0 ms −4 mV −12 mV	
				Δ =	3.2909090	12 ms −8 mV	

Figure 50. Device Reset from Hi-Speed Waveform

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File	Control	Setup	Measure	Analyze	Utilities	Help			7:587	AM
	10.0 MSa/	s 262 k	pts	~	~~~~	<u>~~~</u> ~			1 0	_
	0 On		2	On ▼ 500 mV/	2) On 500 mV/	2	1 On		
4	USB R	eset from	n Suspend T	iming Test	÷					
\mathbf{N}	Instruct	ions: SU cation: 2	SPEND DU 5 uS to 3 m8	T; RESET L S; Record th)UT; meası e results.	ure falling D+ t	o chirp-K			
T TT										
										
Ţ _ĵ1										
_∫1										
1 în	Av									
			and the second se	والمرابع المرابع المرابع المرابع	da la de la de la de la de El El		ويتم والمرام المرام المرام الم	a adarbahat atar atar	adebulu D+ •	18
[-] L	Ť [s n	2.00 ms/	م ارم <mark>1</mark> 8.2	2200000000 ms		T 1.800 V		
More (1 of 2)	Measure	ments M	arkers Scales	5	Measu	rement				
Delete All	📫 curi	AT rent 1. Mean 1.	ime(3-2) 2375000 ms 2375000 ms							HEA.
		min 1.	2375000 ms							

Figure 51. Device Reset from Suspend waveform

3.2.6 Device Test J/K, SE0_NAK test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 52 below.
- 2. Connect the equipment and test fixture as shown in Figure 53.
 - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
 - Connect the [INIT PORT] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
 - Attach the single end probes on Channel 2 to D- of TP2, Channel 3 to D+ of TP2.
- 3. Reboot the device to restore the USB device to normal operation.
- 4. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Choose the right device, Select **TEST_J** from the Device Command drop down menu, then click **EXECUTE** once to place the device into TEST_J test mode.
- Switch the test fixture into the TEST position. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.

- 6. Reboot the device to restore the USB device to normal operation.
- Click Enumerate Bus on the menu of the HS Electrical Test Tool. Choose the right device, Select TEST_K from the Device Command drop down menu, then click EXECUTE once to place the device into TEST_K test mode.
- 8. Switch the test fixture into the **TEST** position. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
- 9. Reboot the device to restore the USB device to normal operation.
- Click Enumerate Bus on the menu of the HS Electrical Test Tool. Choose the right device, Select TEST_SE0_NAK from the Device Command drop down menu, then click EXECUTE once to place the device into TEST_SE0_NAK test mode.
- 11. Switch the test fixture into the **TEST** position. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
- 12. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.



Figure 52. Device Test_J/K, SE0_NAK Test

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HS Electrical Test Tool - Device Test		
Select Device	Device Control	
NONE	Device Command	Device Address
VID 0x4b4, PID 0x6830, Address T, Port 5	TEST_J 👻	0
	NONE	
	TEST_K	
	TEST_SE0_NAK TEST_PACKET	
	SUSPEND	
Enumerate Bus	RESET	eturn To Main
	LOOP DEVICE DESCRIPTOR	
	ENABLE WAKEUP	
	DISABLE WAKEUP SINGLE STEP SET FEATURE	
	SINGLE STEP GET DEV DESC	
Figure 54. Device Test J Command		

Table 11. Host Drop Test Record

Test Mode	D+ Voltage(mV)	D- Voltage(mV)	Expected Value			
J	415	4	360 mV <= D+ <= 440 mV			
			-10 mV <= D- <= 10 mV			
К	4	417	360 mV <= D- <= 440 mV			
			-10 mV <= D+ <= 10 mV			
SE0_NAK	1	1	-10 mV <= D+ <= 10 mV			
			-10 mV <= D- <= 10 mV			

3.2.7 Device receiver sensitivity test

Receiver Sensitivity and Squelch measurements are supposed to be made at the upstream port pins as defined in the USB 2.0 Specification.

A hi-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12-bit times. When all packets are NAK by the device this test (EL_18) is considered to have passed. In Section 7.1.7.2, it requires squelch (EL_16) to occur below 100 mV magnitude. So no packets must be acknowledged between -100 mV and +100 mV. Full squelch may occur at higher voltages, but it is mandatory between -100 mV and +100 mV.

Receiver sensitivity requires all packets to be reliably received down to 150 mV magnitude. Packets may be received at lower voltages, but it is mandatory at levels above 150 mV magnitude. This measurement is to be made at the upstream pins but the test fixture does not allow this. Therefore, the USB-IF requires packets to be reliably received at levels above 200 mV (50 mV waiver to compensate for the voltage drop) for EL_17. Packets can, but do not need to be, received between -200 mV and +200 mV.

See the detailed explanation of Device Receiver Sensitivity, you can visit follow link: <u>http://compliance.usb.org/index.asp?UpdateFile=Electrical&Format=Standard#3</u>



Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 56</u> below, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 57 below.
 - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
 - Connect the [**INIT PORT**] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
 - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
- 3. Connect the 81130A pulse generator to the oscilloscope using the 82357A USB/GPIB Interface.
 - If you choose to use the Agilent 81130A Pulse/Pattern Generator, connect the 8493C 6 dB attenuators to OUTPUT1 and OUTPUT2 of Agilent 81130A Pulse/Pattern Generator.
- 4. Connect OUTPUT1 to SMA1 (D+) of the E2649- 66403 Device Receiver Sensitivity test fixture using the 8120- 4948 SMA cables.
- 5. Connect OUTPUT2 to SMA2 (D-) of the E2649- 66403 Device Receiver Sensitivity test fixture using the 8120- 4948 SMA cables.
- 6. On the 81130A, select the MEMCARD soft key. If MEMCARD is not in the menu, press the MORE key until MEMCARD is displayed. The content of the memory appears on the screen. Use the cursor and the rotary knob to select the MIN_ADD1.ST0 setup file. Move the cursor to Perform Operation and turn the knob to select Recall]. Then press the ENTER key to load it. It generates IN packets (of compliant amplitude) with a 12-bit SYNC field packet pattern.
- 7. Reboot the device to restore the USB device to normal operation.
- Click Enumerate Bus on the menu of the HS Electrical Test Tool. Choose the right device, Select TEST_SE0_NAK from the Device Command drop down menu, then click EXECUTE once to place the device into TEST_SE0_NAK test mode.
- 9. Place the test fixture Test Switch (S1) into the **TEST** position. It switches the data generator in place of the host controller. The data generator emulates the **IN** packets from the host controller.
- 10. Verify that all packets from the data generator are **NAK** 'd by the port under test as shown in Figure 58 below. Record the Pass/Fail in **EL_18**.
- 11. On the 81130A, use the cursor and the rotary knob to select the IN_ADD1.ST0 setup file. Move the cursor to Perform Operation and turn the knob to select [Recall]. Then press the ENTER key to load it. It generates IN packets (of compliant amplitude) with a 32-bit SYNC field packet pattern.

- 12. Verify that all packets from the data generator are **NAK** 'd by the port under test as shown in Figure 60 below.
- 13. Adjust the output level of each channel as follows:
 - Select the [LEVELS] soft key, then move the cursor to the numeric value for [High] voltage value.
 - Adjust the output level with the rotary knob or using the number keys while monitoring the actual level on the oscilloscope.
 - Use the cursor arrow buttons to select the channel to change.
 - Reduce the amplitude of the data generator packets in 20 mV steps (on the generator before the attenuator) while monitoring the **NAK** response from the device on the oscilloscope. The adjustment should be made to both channels such that OUTPUT1 and OUTPUT2 are matched, as indicated by the data generator readout.
 - Reduce the amplitude until the **NAK** packets begins to become intermittent.
 - Increase the amplitude such that the NAK packet is not intermittent.
 - It is just above the minimum receiver sensitivity levels before squelch.
- 14. Using the oscilloscope markers to measure the packet amplitude. Read out the [Ay] and [By] values and record the measurement in **EL_17**.
- 15. Now further reduce the amplitude of the packet from the data generator in small steps.
 - Maintain the balance between OUTPUT1 and OUTPUT2 until the receiver just ceases to respond with a **NAK.**
 - This is the squelch level of the receiver.
- 16. Measure the packet amplitude. Read out the [Ay] and [By] values and record the measurement in EL_16.
- 17. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

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ilo Viow	Tools Help	
Task Flow _	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report	
Set Up	USB Tests	^
1	O Device Hi-Speed	
¥ .	O Device Hi-Speed Signal Quality Test	
Select Tests	Device Packet Parameters	
		_
51	Device Suspend/Resume/Reset Inning	=
V I		
Configure	O EL 18 Receiver sensitivity Test - Minimum SYNC Field	
_	□ O EL 17 Receiver sensitivity Test	
1/	C EL 16 Receiver sensitivity Test @ Squelch	
*	🗄 🗆 🖸 O Low and Full Speed	
Connect	🖳 🖸 Inrush Current Test	
	🗄 🖳 🖸 Upstream Full Speed Signal Quality and Transition Time Test	V
\mathbf{V}	Test Group: Device Receiver Sensitivity	
Run Tests	Description: Tests the sensitivity of the receivers on the upstream facing port of the device under test.	^
		V



HS Electrical Test Tool - Device Test
HS Electrical Test Tool - Device Test Select Device NONE VID 0x4b4, PID 0x6830, Address 1, Port 5 Enumerate Bus
SET ADDRESS ENABLE WAKEUP DISABLE WAKEUP SINGLE STEP SET FEATURE SINGLE STEP GET DEV DESC
Figure 58. Device Test SE0 NAK Command



Figure 59. Receiver Respond with NAK to IN from Data Generator

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Figure 60. Measuring the Packet Amplitude

3.3 Host high-speed signal test

- Host High-Speed Signal Quality Test
 - EL_2: Data Rate Test
 - EL_3: Eye Pattern and Mask Test
 - EL_6: Rise and Fall Time Test
 - EL_7: Non-Monotonic Edge Test
- Host Packet Parameters Test
 - EL_21: Sync Field Length Test
 - EL_25: EOP Length Test
 - EL_23: Inter-packet Gap Between First 2 Packets Test
 - EL_22: Measure Inter-packet Gap Between Host and Device Packet Test
 - EL_55: SOF EOP Width Test
- Host CHIRP Timing Test
 - EL_33: Measure Host CHIRP response time
 - EL_34: Measure Host CHIRP-J/K duration
- Host Suspend/Resume Timing Test
 - EL_39: Host Suspend Timing Response

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- EL_41: Host Resume Timing Response

- Host Test J/K, SE0_NAK Test
 - EL_8: Host J Test
 - EL_8: Host K Test
 - EL_9: Host SE0_NAK Test

3.3.1 HS host electrical test limits

Table 12. HS Host Electrical Test Limits

Test Name	Pass Limits
EL_2 Data Rate	Within 480 Mb/s +/-0.05%
EL_3 Data Eye and Mask Test	Must meet Template 1 transform waveform requirements at TP2
EL_6 Host Rise/Fall Time	>500 ps
EL_7 Host Non-Monotonic Edge Test	Must have monotonic data transitions over the vertical openings
EL_21 Sync Field Length Test	32 bits, 65.62 ns <= VALUE <= 67.700 ns
EL_25 EOP Length Test	8 bits, 15.620 ns <= VALUE <= 17.700 ns
EL_23 Inter-packet Gap Between First 2 Packets Test	183.000 ns <= VALUE <= 399.400 ns
EL_55 SOF EOP Width Test	40 bits, 81.100 ns <= VALUE <= 83.388 ns
EL_22 Inter-packet Gap Between Host and Device Packet Test	16.640 ns <= VALUE <= 399.90 ns
EL_33 CHIRP Timing Response	1 ns <= VALUE <= 100.000 μs
EL_34 CHIRP J/K Width	40.000 μs <= VALUE <= 60.000 μs
EL_35 SOF Timing Response	100.000 μs <= VALUE <= 500.000 μs
EL_39 Suspend Timing Response	3.000 ms <= VALUE <= 3.125 ms
EL_41 Resume Timing Response	VALUE <= 3.000 ms
EL_8 Host J Test	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV
EL_8 Host K Test	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
EL_9 Host SE0_NAK Test	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV

3.3.2 Test method and tool

In USB Certification, Host means a product base on Windows x86 or x64 systems, which can implement the HS Electrical Test Tool on it to run the Host test, and an Embedded Host means a product base on Linux, Android, or other RTOS. Anyway, USB-IF defines a method about entering the specified test modes via PID/ VID detection. See chapter **6.4.1** of "*On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification*".

Certification Lab usual provides an HSEHET Board for Host or Embedded Host test, which can be set to different PIDs, as shown <u>Figure 61</u> below.

Table 13. Test Modes

PID	Test Mode
0x0101	Test_SE0_NAK
0x0102	Test_J
0x0103	Test_K
0x0104	Test_Packet

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Table 13. Test Modescontinued	
PID	Test Mode
0x0105	Reserved
0x0106	HS_HOST_PORT_SUSPEND_RESUME
0x0107	SINGLE_STEP_GET_DEV_DESC
0x0108	SINGLE_STEP_ GET_DEV_DESC_DATA



Figure 61. HSEHET Board for Host High-Speed Test

3.3.3 Host high-speed signal quality test

Test Instructions:

- Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 62</u> and <u>Figure 63</u> below, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 64 below.
 - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
 - Before connecting the HSEHET Board, put it in the right position by selecting **Test_Packet**. Then connect the board to the [**INIT PORT**] with a 5 m cable.
 - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
- 3. Click Run Tests button of Automated Test Software on Oscilloscope.
- 4. Host enumerates the HSEHET board and responds to send continuously **Test_Packet.** Flip the switch of the test fixture that switches the termination on. Verify that the yellow TEST LED is lit.
- 5. You should see the transmitted test packet on oscilloscope as shown in Figure 65 and Figure 66 below.
- 6. When the Testing Complete dialog appears, click **Ok**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

(BETA VERSION 0.01.5101) USB Test USB Device *
File View Tools Help
Task Flow _ Set Up Select Tests Configure Connect Run Tests Automation Results Html Report
Set Up Device Under Test (DUT) Device Under Test (DUT)
Device Test Point: C Device C Hub C Host C On-The-Go Embedded Host
HS Test Connection: Test Method: User Description: Device Identifier:
Configure Comments:
Droop Drop Ports
Connect
Run Tests HS Signal Quality Fixture Selection © Agilent Fixture O USBIF O Other Debug and Information Only
Automation Using 81130A/81134A or E3631A or 34401A C Yes C No Export Data" to transform test results:
Configure Devices Export Data

Figure 62. Select Embedded Host for HS Electrical Test

File View	
	Tools Help
) 📽 🖬 🔤 🕯	M 1 I I I I I I I I I I I I I I I I I I
Task Flow	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report
Set Up	
	Host Hi-Speed O Host Hi-speed Signal Quality O Host Hi-speed Signal Quality
Select Tests	O EL_5 Data Lye and Mask rest O EL_6 Host Rise Time O EL 6 Host Fall Time
	 EL_7 Host Non-Monotonic Edge Test Host Controller Packet Parameters
Configure	Host CHIRP Timing O Host Suspend/Resume Timing
₩	C EL_39 Suspend Timing Response O EL_41 Resume Timing Response
Connect	Host Test J/K, SEU_NAK D Low and Full Speed
\mathbf{V}	(Click a test's name to see description)
Run Tests	

Figure 63. Host HS Signal Quality Test





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Note: Select Embedded Host for non-Windows products. Click Connection Option button here to select Differential or Single-End probe if you are using the latest software.

3.3.4 Host packet parameters test

Test Instructions:

- Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 67</u> below, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 66 above.
 - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
 - Before connecting the HSEHET Board, put it in the right position by selecting SINGLE_STEP_GET_DEVICE_DESCRIPTOR. Then connect the board to the [INIT PORT] with a 5 m cable.
 - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
- 3. Click **Run Tests** button of Automated Test Software on Oscilloscope.

- 4. Host enumerates the HSEHET board and responds to send **SOF** s for 15 seconds. Click **OK** to close the Test Instruction dialog.
- After 15 seconds of SOF s, the host initiates the setup phase of the GetDescriptor() command. The host sends SETUP and DATA (first and second packet), then Device sends an ACK. You should see the transmitted test packet on the oscilloscope as shown in <u>Figure 71</u> below. Click OK to close the Test Instruction dialog.
- 6. Disconnect the HSEHET Board, put it in the right position by selecting **SINGLE_STEP_GET_DEVICE_ DESCRIPTOR_DATA**, then reconnect it to test fixture.
- Host enumerates the HSEHET board and request GetDescriptor(), then wait for 15 seconds. After that, Host initiates an IN token, Device responds a DATA, then Host send an ACK. You should see the transmitted test packet on the oscilloscope as shown in Figure 70 below.
- 8. When the Testing Complete dialog appears, click **Ok.** The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

USB Tes	t USB Device *	1 🕑
File View	Tools Help	
י 🖬 📽 נ		
Task Flow _	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report	
Set Up Select Tests Configure	 USB Tests Hi-Speed Host Hi-Speed Host Hi-speed Signal Quality Host Controller Packet Parameters O EL_21 Sync Field Length Test O EL_25 EOP Length Test O EL_23 Inter-packet Gap Between First 2 Packets Test O EL_22 Inter-packet Gap Between Host And Device Packet Test O EL_55 SOF EOP Width Test O Host CHIRP Timing Host Suspend/Resume Timing O EL_39 Suspend Timing Response 	
Connect	O EL_41 Resume Timing Response	
	Host Test J/K, SEO_NAK	~
V	(Click a test's name to see description)	
Run Tests		^

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Figure 70. EL_25 Host EOP Length Waveform



Figure 71. EL_23 Host Inter-packet Gap Waveform
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Figure 72. EL_22 Host Inter-packet Gap (Host Response to Device) Waveform

3.3.5 Host CHIRP timing test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 73 below, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 74.
 - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [TEST PORT] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
 - Attach the single-ended probes on channel 2 to D-, channel 3 to D+ of TP2 on the test fixture.
- 3. Click **Run Tests** button of Automated Test Software on Oscilloscope.
- 4. Connect any known good Hi-Speed device to the initialize port. Capture the CHIRP handshake as shown in <u>Figure 75</u> and <u>Figure 76</u>.
- 5. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

USB Tes	t USB Device *
File View	Tools Help
Task Flow	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report
Set Up	□····□ O USB Tests
	Host Hi-Speed Host Hi-speed Signal Quality
Select Tests	Host Controller Packet Parameters
Configure	□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □
\mathbf{V}	C EL_39 Suspend Timing Response C EL_41 Resume Timing Response
Connect	⊡ ··· □ ○ Host Test J/K, SE0_NAK ⊡ ··· □ ○ Low and Full Speed
V .	Test Group: Host CHIRP Timing
Run Tests	Description: Tests downstream port CHIRP K and CHIRP J timing response.





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File	Control	Setup	Measure	Analyze	Utilities	Help			11:17 AM
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	0 ^{On}		2	0n 500 mV/	2	3) On 500 m	₩ 🍣	(1) On	
4	USB La	ast CHIRI	P to SOF Tir	ning Test		f	×		
7	Instruct Measu	ions: Dis re time fr	connect and om end of h	d reconnecte ost J/K to firs	ed device; t SOF; Spe	Clear displ c: 100 uS t	ay; Press R 5 500 uS	un; Enumerat	te;
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]]]	·····						*****		
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∫ ∫1	Anne								BY ← T D+i fga
ſŢ								B	
More (1of 2)	1 Markers	Coles		100 µs/	v ~ 1 -	89.0000000)	18 4 0 >	100 mV	● ↑
Delete All				A(3) = B(3) = ∆ = 1/AX =	X -225.36460 89.951 ns 225.45455 4 4354838	5 дв б дв 9 йн ,	Y 29 mV 301 mV 272 mV		2
Figure	76. Time b	etween S	OF and Last	Chirp-J/K					

3.3.6 Host Suspend/Resume timing test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 77 below, and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture.
 - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
 - Attach the single-ended probes on channel 2 to D-, channel 3 to D+ of TP2 on the test fixture.
 - Before connecting the HSEHET Board, put it in the right position by selecting
 - HS_HOST_PORT_SUSPEND_RESUME. Then connect the board to the [INIT PORT] with a 5 m cable.
- 3. Click Run Tests button of Automated Test Software on Oscilloscope.
- 4. After 15 seconds the host port enters Suspend state, as shown in <u>Figure 78</u> below. Click **OK** to close the Test Instruction dialog.

- 5. After 15 seconds of suspend state the host shall issue a **Resume K** state on the bus, then continue sending SOFs. The captured transition should be as shown in <u>Figure 79</u> below.
- 6. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

USB Tes	t USB Device *
Task Flow _ Set Up Select Tests Configure Configure	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report Image: Image
Run Tests	Test Group: Host Suspend/Resume Timing Description: Tests host suspend and resume timing response.



Figure 78. EL_39 Host Suspend waveform

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Note: Attach the HSEHET board slightly earlier before clocking the **Run Tests** button, in case you capture the Bus Enumeration instead of Suspend transition.

3.3.7 Host test J/K, SE0_NAK test

Test Instructions:

- 1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 80 below and make sure you set the Test Type configuration option to "Hi-Speed Near End" before running the test.
- 2. Connect the equipment and test fixture as shown in Figure 81 below.
 - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
 - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
 - Before connecting the HSEHET Board, put it in the right position by selecting **Test_J**. Then connect the board to the [**INIT PORT**] with a 5 m cable.
 - Attach the single-ended probes on channel 2 to D-, channel 3 to D+ of TP2 on the test fixture.
- 3. Click **Run Tests** button of Automated Test Software on Oscilloscope.

- 4. Host enumerates the HSEHET board and enters a Hi-Speed **J State** (D+ high; D- low). Flip the switch of the test fixture that switches the termination on. Verify that the yellow TEST LED is lit. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
- 5. Flip the switch of the test fixture to OFF mode.
- 6. Press the RESET button on DUT or repower it to reset the system.
- 7. Remove the HSEHET board from [INIT PORT] of the test fixture, and put it in the right position by selecting **Test_K**. Then connect the board to the [INIT PORT] again with a 5 m cable.
- Host enumerates the HSEHET board and enters a Hi-Speed K State (D+ low; D- high). Flip the switch of the test fixture that switches the termination on, verify that the yellow TEST LED is lit. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
- 9. Flip the switch of the test fixture to OFF mode.
- 10. Remove the HSEHET board from [INIT PORT] of the test fixture, and put it in the right position by selecting **Test_SE0_NAK**. Then connect the board to the [INIT PORT] again with a 5 m cable.
- 11. Host enumerates the HSEHET board and enters the **SE0 State** (D+ low; D- low). Flip the switch of the test fixture that switches the termination on, verify that the yellow TEST LED is lit. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
- 12. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

🕷 USB Tes	t USB Device * 🛛 💶 🔀
File View	Tools Help
Task Flow _	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report
Select Tests	 Hospeta Host Hi-Speed Host Hi-speed Signal Quality Host Controller Packet Parameters Host CHIRP Timing Host Suspend/Resume Timing Host Suspend/Resume Timing Host Test J/K, SEO_NAK C EL_8 Host J Test C EL_8 Host K Test C EL_9 Host SEO_NAK Test
	Test Group: Host Test J/K, SE0_NAK
Run Tests	Description: Measures the K and J signal amplitudes.

Figure 80. Host Test_J/K, SE0_NAK Test

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Table 14. Host Drop Test Record

Test Mode	D+ Voltage(m V)	D- Voltage(mV)	Expected Value
J	400	4	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV
К	4	400	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
SE0_NAK	1	1	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV

3.4 USB3.0 super speed transmitter compliance tests

- Host Low Frequency Periodic Signaling TX Tests
- Host Transmitted SSC Tests
- Host Transmitter Eye Short Channel Tests
- Host Transmitter Eye Far End(TP1) Tests
- Device Low Frequency Periodic Signaling TX Tests
- Device Transmitted SSC Tests
- Device Transmitter Eye Short Channel Tests
- Device Transmitter Eye Far End(TP1) Tests

3.4.1 USB 3.0 super speed transmitted electrical test limits

Table 15. Super Speed Electrical Test Limits

Test Name	Pass Limits
5G LFPS Peak-Peak Differential Output Voltage	800.0 mV <= VALUE <= 1.2000 V
5G LFPS Period (tPeriod)	20.0000 ns <= VALUE <= 100.0000 ns
5G LFPS Burst Width (tBurst)	600.0 ns <= VALUE <= 1.4000 μs

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Test Name	Pass Limits
5G LFPS Repeat Time Interval (tRepeat)	6.0000 μ s <= VALUE <= 14.0000 μs
5G LFPS Rise Time	VALUE <= 4.0000 ns
5G LFPS Fall Time	VALUE <= 4.0000 ns
5G LFPS Duty cycle	40.0000 % <= VALUE <= 60.0000 %
5G LFPS AC Common Mode Voltage	VALUE <= 100.0 mV
5G TSSC-Freq-Dev-Min	-5.300000 kppm <= VALUE <= -3.700000 kppm
5G TSSC-Freq-Dev-Max	TSSCMin ppm <= VALUE <= TSSCMax ppm
5G SSC Modulation Rate	30.000000 kHz <= VALUE <= 33.000000 kHz
5G SSC Slew Rate	VALUE <= 10.000 ms
5G Short Channel Random Jitter	Information Only
5G Short Channel Maximum Deterministic Jitter	VALUE <= 86.000 ps
5G Short Channel Total Jitter at BER-12	VALUE <= 132.000 ps
5G Short Channel Template Test	VALUE = 0.000
5G Short Channel Differential Output Voltage	100.0 mV <= VALUE <= 1.2000 V
5G Random Jitter (CTLE ON)	Information Only
5G Far End Maximum Deterministic Jitter (CTLE ON)	VALUE <= 86.000 ps
5G Far End Total Jitter at BER-12 (CTLE ON)	VALUE <= 132.000 ps
5G Far End Template Test (CTLE ON)	VALUE = 0.000
5G Far End Differential Output Voltage (CTLE ON)	100.0 mV <= VALUE <= 1.2000 V

 Table 15. Super Speed Electrical Test Limits...continued

3.4.2 Host low frequency periodic signaling TX test

This test verifies that the low frequency periodic signal transmitter meets the timing requirements when measured at the compliance test port.

Test Instructions:

- Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 82</u>, and make sure you set the Test Type configuration option in <u>Figure 83</u>. If the DUT is a Standard A port, "Configure Transfer Function" should be "**Std A to Std B**". If the DUT is a Type-C port, "Configure Transfer Function" should be "**C to C**".
- 2. Select the test items in the USB Automated Test Software in Figure 84
- 3. Set the test configures default in Figure 85.
- 4. Connect your Device Under Test to the Host Test Fixture 1. VBUS is not required. If the DUT is a Standard A port, we choose Test Topology of Standard-A Port in <u>Figure 86</u>. If the DUT is a Type-C port, we choose Test Topology of Type-C Port in <u>Figure 87</u>. And you need **a Jumper** to cover the CC pin to GND on which path you choose.
- 5. Connect 5 Inch Host Test Fixture 2 to Host Test Fixture 1 using Type A to Type B cable. When Type-C port is tested, a hub from Type A to Type C is needed in Figure 90.
- 6. Connect **RX+** of the Test Fixture 2 to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes.
- Connect TX+ and TX- of the Test Fixture 1 to Oscilloscope Channel 1 and Channel 3 using SMA cables. The full connection diagram is show in <u>Figure 89</u> and <u>Figure 90</u>
- 8. Click **Run Tests** in the USB Automated Test Software on Oscilloscope. After the test is finished, you can view the report in HTML Report page.

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sure/Mark Math	Analyze Utilities Demos Help	
ots	Gallery Quick Jitter Diagrams D	
	Histogram Mask Test	4.00
	Automated Test Apps	U7233A/U7233B DDR1 Test App
	Analysis Diagram Measurement Analysis (EZJIT) Jitter/Noise (EZJIT Complete) Real-Time Eye Launch VSA Unlicensed Apps	07231B/07231C DDR3 Test App0N6462A/N6462B DDR4 Test AppN6469A eDP Test AppN5392B/N5392C Ethernet Test App00N5399C/N5399D HDMI Test App00N5413B/N5413C DDR2(+LP) Test App00U7238E MIPI D-PHY Test App00N5393F/N5393G PCIExpress Test App00
		N5411B SATA6G Test App U7243B USB3 Test App

Figure 82. Automated Test Software for USB 3.0



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Figure 89. Full Connection Diagram of Host TX Test Topology with Standard-A Port



Figure 90. Full Connection Diagram of Host TX Test Topology with Type-C Port

9. In test execution, the test software pops up the right image in <u>Figure 91</u>. Disconnect the DUT and USB test fixture, then **restart DUT**, and click OK.

When the dialog information appears again, power on DUT normally, then connect DUT to USB test fixture, and make sure that the LFPS signal is captured at the same time. If the captured waveform is the same with the reference, click **OK** in Figure 92.

, File Control Setup Display Trigge	er Measure Math	Analyze Utilities Demos Help	2:41 PM Jul 29, 2016		.][
Run Stop Single 💽 80.0 GSa/s	80.0 kpts	~~~~~~	12.0 GHz	T 0.0 V	
Ţ <u>1.00 V/ 0.0 V</u> + ₽	.)				
e Meas					
Pertic Running T	est 1 of 22		X]	
	Current T	Test: 5G LFPS Peak-Peak Differential Output Voltage			
Completed	Status: Performent M	3.1 Information Please disconnect the USB 3.0 test fixture for Please exit/ close the HSETT tool Ol	rom the DUT and reset or po	ower cycle the DUT.	
Stop	Progress:				
Figure 91. Prompt Box in Tes	st				

10. The software automatically completes the test in Figure 93 and Figure 94.





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3.4.3 Host transmitted SSC/ Eye short / Eye far end tests

Transmitted SSC test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with spec required TX equalization. To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Transmitted Eye Test at 5 GT/s verifies that the transmitter meets the eye width, deterministic jitter, and random jitter requirements when measured at the compliance test port with nominal transmitter equalization and after processing with the appropriate channels and post-processing as shown in Table 16.

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

	<u> </u>	
Connector Type	Channel	Reference Equalizer
Std-A	3 m Cable + 5" PCB	Long Channel
Std-B	3 m Cable + 11" PCB	Long Channel
Type-C(Host)	Device Under Test >> USB 3.1 Host Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB) SSGen1 TxComp12p7dB Embedding.s4p	Long Channel

Table 16. Channels and Reference Equalizer for Testing Device Types

Connector Type	Channel	Reference Equalizer
Type-C(Device)	Device Under Test >> USB 3.1 Device Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB) SSGen1_TxComp12p7dB_Embedding.s4p	Long Channel
Micro-B	1 m Cable + 11" PCB	Long Channel
Micro-AB (Host only)	1 m Cable + 5" PCB + Micro-A to Std-A Receptacle adapter	Long Channel
Micro-AB(DRD)	1 m Cable + 11" PCB (device mode) 1 m Cable + 5" PCB + Micro-A to Std-A Receptacle adapter (host mode) Both tests are required	Long Channel
Tethered (Standard A Plug)	11" PCB	Long Channel
All Types	No Channel (break-out fixture only)	Short Channel

Table 16. Channels and Reference Equalizer for Testing Device Types ... continued

Note:

Note: Refer to <u>https://usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf</u> for embedding the long channels when using breakout fixtures.

Test Instructions:

- The connection will remain unchanged in <u>Figure 95</u>, and the "I have completed these instructions" will be directly checked, and then click Next. After LFPS TX test is over, then continue to start SSC Test automatically.
- 2. In the stage of automatic test, if below dialog in <u>Figure 96</u> appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP1 test pattern** manually.

Make sure that the Cal output channel is connected to the SSRX port of fixture, then click **"Toggle"** button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click **OK** and continue to do next test.

- 3. If below dialog in <u>Figure 97</u> appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP0 test pattern**. Make sure that the Cal output channel is connected to the SSRX port of fixture, then click toggle button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click **OK** and continue to do next test.
- 4. After SSC test is over, then continue to start **"Transmitter Eye Short Channel Test"** automatically in Figure 98.

After each test item is over, the software shows change physical connection/setup dialog window, select **I** have completed these instructions and click **Next** to start new test in Figure 99.

- 5. After "Transmitter Eye Short Channel Test" is end, then begin to the "Transmitter Eye Far End Test" automatically. the software shows change physical connection/setup dialog window, select "I have completed these instructions" and click "Next" to next step in Figure 100.
- 6. All the electrical compliance test is finished, save the test report from the menu "File"->"Save Project As" in Figure 101. And export results.

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Connect to USB 3.1 Device Under Test transmitter at TPO Steps 1. Connect your Device Under Test to the USB test fixture. Verify that VBUS is not applied to the test fixture. 2. Connect Tx+ and Tx- of the test fixture to Oscilloscope Channel 1 and Channel 3 using SMA cables 3. Connect Rx+ of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram Full Connect Connection Diagram Full Connection Diagr	change in the physical	al connection or set	p ip is required.	Please follow the ins	structions below to se	up for (Near End Transm	itter Eye):	Vie Sco
Steps 1. Connect your Device Under Test to the USB test fixture. Verify that VBUS is not applied to the test fixture. 2. Connect Tx+ and Tx- of the test fixture to Oscilloscope Channel 1 and Channel 3 using SMA cables 3. Connect Rx+ of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram Image: State of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram Image: State of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram Image: State of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram Image: State of the test fixture to the Aux Out of DSO 90000 scope sore cal Out from DSOX 90000 scopes. Connection Diagram Image: State of the test fixture to the Aux Out of DSO 90000 scope sore cal Out from DSOX 90000 scope scop		Connec	t to USB	3.1 Device Ur	ider Test transi	nitter at TP0		
 1. Connect your Device Under Test to the USB test fixture. Verify that VBUS is not applied to the test fixture. 2. Connect Tx+ and Tx- of the test fixture to Oscilloscope Channel 1 and Channel 3 using SMA cables 3. Connect Rx+ of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram 	Steps							
 2. Connect Tx+ and Tx- of the test fixture to Oscilloscope Channel 1 and Channel 3 using SMA cables 3. Connect Rx+ of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram Connection Diagram<td>1. Connect your</td><td>Device Under T</td><td>est to <mark>t</mark>he U</td><td>SB test fixture. V</td><td>erify that VBUS i</td><td>s not applied to the t</td><td>es<mark>t fixtu</mark>re.</td><td></td>	1. Connect your	Device Under T	est to <mark>t</mark> he U	SB test fixture. V	erify that VBUS i	s not applied to the t	es <mark>t fixtu</mark> re.	
3. Connect Rx+ of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes. Connection Diagram	2. Connect Tx+	and Tx- of the te	st fixture to	Oscilloscope Ch	annel 1 and Chan	nel 3 using SMA cab	oles	
Connection Diagram	3. Connect Rx+	of the test fixture	to the Aux	Out of DSO 900	00 scopes or Cal	Out from DSOX 90	0000 Scopes	2
Image: Contract of the second seco	Connection Dia	agram						
Cancel Ignore Next > Finish	Rx+ Cal Out (DSO90000) AUX Out (Da RIG: (Checking)	or so	I have com	pleted these instruction	ons			











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New Project Open Project							
Open Project							
	•	ure Connect Run Tests Automation Results Html Report					
Save Project							
Save Project A	IS						
Save Project (S	Settings-Only) As						
Export Results		USB3.1 Test Report					
User Defined		,					
User Denned	,	Overall Result: PASS					
Print							
Page Setup		Test Configuration Details					
Print Preview		Device Description					
Print Preview.		C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions\N7015A_DeembedTypC_TypC_14p1dbAt5GHz_Embed.tf4					
Recent Project	ts P	C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions\U7242A_DeembedUSB3_TX_Host_Channel.tf4					
Exit		Device 1					
AL.	AdaMada	set					
¥	Aucinoue DC Gain						
Run Tests	Reference Clock	SAC SAC					
	Device	Host					
	Device ID:	Device 1					
		Test Session Details					
	Infiniium SW Ver	sion 05.60.00603					
	Infiniium Model M	Iumber MSOV334A					
	Infiniium Serial N	Iumber MY55170109					
	Application SW V	fersion 3.00.0001					
	Debug Mode Use	at No					
	Compliance Limi	ts (official) USB 3.1 Specification version 1.0					
	Last Test Date	2018-07-29 15:34:45 UTC +08:00					

3.4.4 Device low frequency periodic signaling TX test

This test verifies that the low frequency periodic signal transmitter meets the timing requirements when measured at the compliance test port.

Test Instructions:

- Select the test items in the USB Automated Test Software on Oscilloscope as shown in <u>Figure 102</u> below, and make sure you set the Test Type configuration option in <u>Figure 103</u>. If the DUT is a Standard A port, "Configure Transfer Function" should be "**Std A to Std B**". If the DUT is a Type-C port, "Configure Transfer Function" should be "**C to C**".
- 2. Select the test items in the USB Automated Test Software in Figure 104
- 3. Set the test configures default in Figure 105.
- 4. Connect your Device Under Test to the Device Test Fixture 1. VBUS is not required. If the DUT is a Standard A port, we choose Test Topology of Standard-A Port in Figure 106. If the DUT is a Type-C port, we choose Test Topology of Type-C Port in Figure 107. And you need a Jumper to cover the CC pin to VCC on which path you choose.
- 5. Connect 5 Inch Device Test Fixture 2 to Device test Fixture 1 using type A to type B cable. When Type-C port is tested, a hub from type A to Type C is needed in Figure 109.
- Connect RX+ of the Test Fixture 2 to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes in Figure 108.

- Connect TX+ and TX- of the Test Fixture 1 to Oscilloscope Channel 1 and Channel 3 using SMA cables. The full connection diagram is show in <u>Figure 109</u>.
- 8. Click **Run Tests** in the USB Automated Test Software on Oscilloscope. After the test is finished, you can view the report in HTML Report page.

	9				
sure/Mark Math	Analyze Utilities Demos Help Gallery Quick Jitter Quick Eye Diagrams Histogram Mask Test	1:18 PM 5/22/2019 ₩ KEYSIGHT z T 0.0 V SC 4.0			
	Automated Test Apps Analysis Diagram Measurement Analysis (EZJIT) Jitter/Noise (EZJIT Complete) Real-Time Eye Launch VSA Unlicensed Apps	 U7233A/U7233B DDR1 Test App U7231B/U7231C DDR3 Test App N6462A/N6462B DDR4 Test App N6469A eDP Test App N5392B/N5392C Ethernet Test App N5399C/N5399D HDMI Test App N5413B/N5413C DDR2(+LP) Test App U7238E MIPI D-PHY Test App N5393F/N5393G PCIExpress Test App N5411B SATASC Test App 			
		U7243B USB3 Test App 0.0			

Figure 102. Automated Test Software for USB 3.0













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Figure 109. Full Connection Diagram of Host RX Test Topology with Type-C Port

In test execution, the test software will pop up the right image in <u>Figure 109</u>. Disconnect the DUT and USB test fixture, then **restart DUT**, and click **OK**.
 When the dialog information appears again, power on DUT normally, then connect DUT to USB test fixture,

and make sure that the LFPS signal is captured at the same time. If the captured waveform is the same with the reference, click "**OK**" in Figure 110.

10. The software will automatically complete the test in Figure 111 and Figure 112.

File	Control Setu	ıp Dis	play Trigge	er Measure	Math An	alyze Utilities Demo	s Help	2:41 PM Jul 29, 2016	KEYSIGHT	_) [
Run	Stop Single	∽]8	0.0 GSa/s	80.0 kpts		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	$\sim\sim$	12.0 GHz	T 0.0 V	
T.	1.00 V/	0.0 \	/ • 🕂							
e Meas										
/ertic	Running Test 1 of 22									
al M	Current Test: 5G LFPS Peak-Peak Differential Output Voltage									
leas			Completed							
					USB3.11	Information		100		
					0	Please disconnect the US Please exit/ close the HS	SB 3.0 test fixture fro ETT tool	om the DUT and reset or p	oower cycle the DUT.	j.
							OK			
		·····		Status: Perf	orming Autom	ated Step	_			
>				Progress:						
lea			Stop	1						
nsı			Pup Listil: apos	1						
Figure 110. Prompt Box in Test										




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3.4.5 Device transmitted SSC/ Eye short / Eye far end tests

Transmitted SSC test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with spec required TX equalization. In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Transmitted Eye Test at 5 GT/s verifies that the transmitter meets the eye width, deterministic jitter, and random jitter requirements when measured at the compliance test port with nominal transmitter equalization and after processing with the appropriate channels and post-processing as shown in <u>Table 17</u>.

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Table 17.	Channels and	Reference	Equalizer for	Testing	Device Types
-----------	--------------	-----------	---------------	---------	--------------

Connector Type	Channel	Reference Equalizer
Std-A	3 m Cable + 5" PCB	Long Channel
Std-B	3 m Cable + 11" PCB	Long Channel
Type-C(Host)	Device Under Test >> USB 3.1 Host Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB)	Long Channel

Connector Type	Channel	Reference Equalizer
	SSGen1_TxComp12p7dB_Embedding.s4p	
Type-C(Device)	Device Under Test >> USB 3.1 Device Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB) SSGen1_TxComp12p7dB_Embedding.s4p	Long Channel
Micro-B	1 m Cable + 11" PCB	Long Channel
Micro-AB (Host only)	1 m Cable + 5" PCB + Micro-A to Std-A Receptacle adapter	Long Channel
Micro-AB(DRD)	1 m Cable + 11" PCB (device mode) 1 m Cable + 5" PCB + Micro-A to Std-A Receptacle adapter (host mode) Both tests are required	Long Channel
Tethered (Standard A Plug)	11" PCB	Long Channel
All Types	No Channel (break-out fixture only)	Short Channel

Table 17. Channels and Reference Equalizer for Testing Device Types...continued

Note:

Note: Refer to <u>http://www.usb.orgusb.kavi.com/developers/estoreinfo/SuperSpeedTestTopologies.pdf</u>

Test Instructions:

- 1. The connection remains unchanged in Figure 113. After the "I have completed these instructions" is directly checked, click "Next". After LFPS TX test is over, continue to start "SSC Test" automatically.
- 2. In the stage of automatic test, if below dialog in <u>Figure 114</u> appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP1 test pattern** manually.

Make sure that the Cal output channel is connected to the SSRX port of fixture, then click "Toggle" button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click "OK" and continue to do next test.

- if below dialog in <u>Figure 115</u> appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP0 test pattern** manually. Make sure that the Cal output channel is connected to the SSRX port of fixture, then click **toggle** button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click "OK" and continue to do next test.
- 4. After SSC test is over, then continue to start **"Transmitter Eye Short Channel Test"** automatically in Figure 116.

After each test item is over, the software shows change physical connection/setup dialog window, select "I have completed these instructions" and click "Next" to start new test in Figure 117.

- 5. After "Transmitter Eye Short Channel Test" is end, then begin to the "Transmitter Eye Far End Test" automatically. the software shows change physical connection/setup dialog window, select "I have completed these instructions" and click "Next" to next step in Figure 118
- 6. All the electrical compliance test is finished, save the test report from the menu "File"->"Save Project As" in Figure 119. And export results.

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USB3.1 USB3 Devi	ice 1 *	
View Tools H	ielp	
New Project		
Open Project	ure C	onnect Run Tests Automation Results Html Report
Save Project		
Save Project As	>	
Save Project (Setti	ings-Only) As	
Export Results	•	USB3.1 Test Report
User Defined	+	
		Overall Result: PASS
Print		
Page Setup		Lest Contiguration Details
Print Preview		C:\Users\Public\Documents\Infinitium\Apos\USB3Test\TransferFunctions\N7015A_DeembedTvpC_TvpC_14n1dhAt5GHz_Embed_tf4
Recent Projects	•	C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions\U7242A Deembed USB3 TX Host Channel.tf4
1000 C		Device 1
Exit	. iet	
\mathbf{v}	AdcMode	AUTO
un Tosta	DC Gain	0
tun rests	Reference Clock	SSC
	Device	Host
	Device ID:	Device 1
		Test Session Details
	Infinitum SW Version	05.60.00603
	Infinitum Model Number	MV5012010
	Application SW Version	3.00.0001
	Debug Mode Used	No
	Compliance Limits (offici	al) USB 3.1 Specification version 1.0
	Last Test Date	2016-07-29 15:34:45 UTC +08:00
Su Tes P:	st Statistics Failed 0 assed 22	
2 Tests View/Save	e/Print detailed HTML results.	Connection: Far End Transmitter Eye
gure 120. S	Save Project	

3.5 USB3.0 super speed receiver compliance tests

TBD

4 Device framework test

4.1 Introduction of device framework test

When testing a USB device or hub, you should at least test USBCV (Command Verifier). It automatically tests the device framework and descriptor. All USB 2.0 peripherals seeking certification are required to demonstrate enumeration on the USB 3.0 PDK. So both USB20CV and USB30CV tests are required. These test tools are available on the USB.ORG, <u>http://www.usb.org/developers/tools/</u>. Read the installation guide carefully before you start testing.

For Hi-speed peripherals, the Chapter 9 tests must be executed twice – once in Full-speed mode, and once in Hi-speed mode. It is not necessary to run HID, Mass-Storage (MSC), Video Class (UVC) at both speeds.

Download the <u>*Company List*</u> and save as "usb.if" in the same directory where USBCV is installed. You can find the company ID from this list. Remember this list changes almost every day, be sure to get a fresh copy when you use the tools.

Test Items:

- USBCV Chapter 9
- USBCV Class Test
- USBCV Current Measurement Test

4.2 USBCV Chapter 9 test

The Chapter 9 tests cover the device support of the commands set in Chapter 9 of the USB specification.

To see the detailed description of test items, refer the documents **#Universal Serial Bus Revision 2.0 USB** Command Verifier Compliance Test Specification Revision 1.2 and **# Universal Serial Bus Revision 3.1** USB Command Verifier Compliance Test Specification Revision 0.7.

Test Items:

- TD 9.1: Device Descriptor Test
- TD 9.2: Configuration Descriptor Test
- TD 9.3: Interface Association Descriptor Test
- TD 9.4: Interface Descriptor Test
- TD 9.5: Endpoint Descriptor Test
- TD 9.7: BOS Descriptor Test
- TD 9.9: Halt Endpoint Test
- TD 9.12: Remote Wake-up Test
- TD 9.13: Set Configuration Test
- TD 9.14: Suspend/Resume Test
- TD 9.16: Enumeration Test
- TD 9.17: Other Speed Configuration Descriptor Test
- TD 9.18: Device Qualifier Descriptor Test
- TD 9.21: LPM L 1 Suspend Resume Test

Test Instructions:

- 1. Install USB20CV on the Test Bed Computer with USB2.0 ports, and USB30CV on the Test Bed Computer with USB3.0 ports.
- 2. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the **gold-tree20** HS Hub.
- 3. Run USB20CV 21 on Computer, select Chapter 9 Tests, and then click Run button to launch the tests.
- 4. Select the DUT device in the list, click Ok as shown in Figure 121 below.
- 5. After Chapter 9 tests are finished, USB20CV will pop out a window shows which other tests must be done, as shown in <u>Figure 122</u> below. i.MX series acts as Mass Storage in Device Mode, so if the pop-out box asks you to do tests more than MSC, you should check your configuration of supported Device Class.
- 6. Click Launch Report Viewer to view the test report. From the basic Chapter 9 Tests, you can get VID, PID, and other information of DUT, check that the VID should be your company VID. Remember MSC Serial number characters must be "0-9" or "A-F", in ASCII 0x0030-0x0039 or 0x0041-0x0046. For self-powered devices, verify that the "Device is currently SELF POWERED22", for bus-powered devices, verify that the "Device is currently BUS POWERED".
- 7. Change the HS hub to a gold-tree FS Hub, then run the test again in Full-speed mode.
- 8. Run USB30CV on Computer, do the Chapter 9 Tests again, both in Hi-speed and Full-speed modes



Select Test Mode © Compliance Test © Debug	Prompt for Test Parameters	Now Starting Test: Endp OtherSpeedConfigurati Start time: Wed Dec 03	voint Descriptor Test (Configuration Index 0 ion Index 0) 14-59-01 2014
Select Test Suite Chapter 9 Tests Current Measurement Test Device Summary HID Tests HUD Tests MSC Tests OTC Tests		Testing Interface number : Endpoint descriptor length : Endpoint descriptor type : 5 Endpoint descriptor type : Endpoint descriptor aw Mai Endpoint descriptor interval Endpoint descriptor interval Endpoint descriptor interval	0 Alternate setting : 0 ; 7 ; 7 er : 1, Direction : IN butes : 2 *PacketSize : 200 : 0 : 7
Chapter 9 Tests Chapter 9 Test	Tested state	mmand Verifier C Tests on this device	LT : (Configuration Index 0 ngs (0)]
Interface Descriptor Test Interface Descriptor Test Endpoint Descriptor Test Set Configuration Test Suspend/Resume Test Remote Wakeup Test - En Remote Wakeup Test - En Remote Wakeup Test - En Other Speed Configuration	- Configured Stat - Addressed State sabled ration: riptor Test - Addressed State scriptor Test - Addressed State iptor Test - Addressed State iptor Test - Addressed State	DK Device speed is Full Beginning enumeration minutes to complete. 25 enu 50 enu 75 enu 100 eru 125 er 150 eru 125 er 150 eru 150 eru 150 eru 150 eru 150 eru 150 eru	peat 150 times) test with 150 enumerations. This may take several umerations umerations numerations numerations evice 29, function 0
Optional Test Description	1		

Figure 122. Prompt box after USB20CV Chapter 9 Tests

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elect Test Mode	
Compliance Test Prompt for Test Parameters Debug	Validating "Chapter 9 Tests [USB 2 devices].cvtests" with MSXML Version 6 Validation succeeded!
elect Test Suite Ilboard Tests [xHCI] (beta) Ilboard Tests [USB 2 devices] Inapter 9 Tests [USB 3 Gen X devices] Irrent Measurement Test [USB 2 devices] Irrent Measurement Test [USB 3 Gen X devices] evice Summary ID Tects	
Test Passed Test Not Run Chapter 9 Tests Cha	
 TD 9.1: Device Descriptor Test TD 9.2: Configuration Descriptor Test TD 9.3 Interface Association Descriptor Test TD 9.4: Interface Descriptor Test TD 9.5: Endpoint Descriptor Test TD 9.7: BOS Descriptor Test Addressed State 	
 TD 9.1: Device Descriptor Test TD 9.2: Configuration Descriptor Test TD 9.3 Interface Association Descriptor Test TD 9.4: Interface Descriptor Test TD 9.5: Endpoint Descriptor Test TD 9.7: BOS Descriptor Test Configured State 	
TD 9.1: Device Descriptor Test	
Optional Test Description	
Dura Laurah Darash Visuan Cata Durash Dirasha	A Undate Display Evit

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Figure 124. Prompt box after USB30CV Chapter 9 Tests

Note:

- See gold-tree devices list in Chapter 4.
- When you run USBCV, it replaces the standard Microsoft EHCI host driver with its own test stack driver, so all standard peripherals on computer, such as mouse, U-disk are invalid at this moment.
- i.MX series acts as Self-Powered Device in device mode.

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4.3 USBCV class test

Appropriate class tests (HID, HUB, MSC, UVC, PHDC, and so on,...) should be done according to the prompt of Chapter 9 Tests, as shown in Figure 122 above.

To see the detailed description of test items, refer the documents **#Universal Serial Bus Revision 2.0 USB** Command Verifier Compliance Test Specification Revision 1.2 and **# Universal Serial Bus Mass Storage** Class Compliance Test Specification Revision 1.1.

Note: i.MX series is enumerated as Mass Storage in device mode, so only must implement MSC Test.

4.3.1 MSC test

It is intended that all devices which report a Mass Storage Class interface is required to pass this test in order to receive logo certification. The tests described herein shall be run on all interfaces that report themselves as MSC.

Test Items:

- TD 1.1: Interface Descriptor Test
- TD 1.2: Serial Number Test
- TD 1.3: Class-Specific Request Test
- TD 1.3: Error Recovery Test
- TD 1.5: Case 1 Test
- TD 1.6: Case 2 Test
- TD 1.7: Case 3 Test
- TD 1.8: Case 4 Test
- TD 1.9: Case 5 Test
- TD 1.10: Case 6 Test
- TD 1.11: Case 7 Test
- TD 1.12: Case 8 Test
- TD 1.13: Case 9 Test
- TD 1.14: Case 10 Test

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- TD 1.15: Case 11 Test
- TD 1.16: Case 12 Test
- TD 1.17: Case 13 Test
- TD 1.18: Power-Up Test
- TD 1.19: CB Length Test
- TD 1.19: CB Length Test
- TD 2.1: Required Commands Test
- TD 2.2: Optional Commands Test

Test Instructions:

- 1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
- 2. Run USB20CV on Computer, select **MSC Tests**, and then click **Run** button to launch the tests.
- 3. Select the DUT device in the list, click Ok as shown in Figure 126 below.
- 4. During the test, a pop-out dialog asks you to disconnect and power off DUT, and then repower it, as shown in <u>Figure 127</u> below.
- 5. After the test is done, click Launch Report Viewer to view the test report.
- 6. Change the HS hub to a gold-tree FS Hub, then run the test again in Full-speed mode
- 7. Run USB30CV on Computer, do the MSC Tests again.

Select Test Mode C Compliance Test Debug	st Parameters Test log initialized. Log Level: Normal	
	Windows 7 Enterprise (Build 7601, 18717	7.x86fre.win7sp1_gdr.150113-1808)
Hect Test Suite hapter 9 Tests urrent Measurement Test evice Summary ID Tests ub Tests SC Tests SC Tests	CVExe.exe ver 1.5.0.0 CVExe.exe ver 1.5.0.0 CommandVerifierLog.dll ver 1.5.0.0 TSMFCGuiDialogHelperDLL.dll ver 1.5.0.0 TestSuiteEngine.dll ver 1.5.0.0 EhciDevIOCTL.dll ver 1.4.14.0 EhciTestServices.dll ver 1.4.14.0	0
Test Passed USI	B 2.0/eHCI Command Verifier	
lect Test MSC Tests MSC Tests ✓ For each Configuration: ✓ If this an MSC Configuration ✓ If this Configuration is MSC ✓ Serial Number Test - Device Addressed ✓ Serial Number Test - Device Configured ✓ Interface Descriptor Test - Device Add ✓ Interface Descriptor Test - Device Configured ✓ Interface Descriptor Test - Device Configured ✓ Class Request Test - Device Configured ✓ Class Request Test - Device Configured	Please select device to test HS_Device (MSC/BOT) addr=2: VID=15a2, PID=007b	14.0 ction 0
 ✓ Case 1 - Device Configured ✓ Case 2 - Device Configured ✓ Case 3 - Device Configured ✓ Case 4 - Device Configured 	OK	1
 ✓ Case 5 - Device Configured ✓ Case 6 - Device Configured ✓ Case 7 - Device Configured ✓ Case 8 - Device Configured ✓ Case 9 - Device Configured 	-	
Optional Test Description		
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Note: Not necessary to run these tests at both High Speed and Full Speed once, basing on the explanation in USB-IF Compliance Updates.

4.3.2 HID test

It is intended that all devices which report a Human Interface Device interface is required to pass this test in order to receive logo certification. The tests described herein shall be run on all interfaces that report themselves as HID.

Test Items:

- HID Descriptor Test
- HID Get/Set Idle Test
- HID Get/Set Protocol Test
- HID Report Descriptor Test

HID Specification Version Test Test Items:

- HID Descriptor Test
- HID Get/Set Idle Test
- HID Get/Set Protocol Test
- HID Report Descriptor Test
- HID Specification Version Test

Test Instructions:

- 1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
- 2. Run USB20CV on Computer, select **HID Tests**, and then click **Run** button to launch the tests.
- 3. Select the DUT device in the list, click Ok as shown in Fig4-8 below.
- 4. After the test is done, click Launch Report Viewer to view the test report.
- 5. Change the HS hub to a gold-tree FS Hub, then run the test again in Full-speed mode 25.
- 6. Run USB30CV on Computer, do the HID Tests again.

Test log initialized. User Input module initialized Windows 7 Enterprise (Build 7601.18717.x86fre.win7sp1_gdr.150113-1808) Service Pack 1.0 CVExe.exe ver 1.5.0.0 CommandVerifier.log.dll ver 1.5.0.0 TestSuiteEngine.dll ver 1.5.0.0 TestSuiteIngine.dll ver 1.5.0.0 TestSuiteIngine.dll ver 1.4.15.0 USB CommandVerifier.dll ver 1.4.15.0 USB CommandVerifier.dll ver 1.4.15.0 USB CommandVerifier.dll ver 1.4.15.0 TestSuiteEngine.dll ver 1.4.15.0 USB CommandVerifier.dll ver 1.4.15.0 Current Host: PCI bus 0, device 29, function 0 Number of ports: 3 Hots selected: PCI bus 0, device 29, function 0 VISB 2.0/eHCI Command Verifier Please select device to test HS Device (HID) addr=2: VID=15a2, PID=008c DK
ctory Update Display Exit

Note: Not necessary to run these tests at both High Speed and Full Speed once, basing on the explanation in USB-IF Compliance Updates.

4.4 USBCV current measurement test

In order to measure the power distribution of a USB device, the average current is measured during **unconfigured**, **configured**, **active**, and **suspend** state with a digital multimeter and fixture to measure the

VBUS current. The circumstances for measuring the average current are dependent on the speed of the device and the power mode the device is in (for example, self-powered, bus-powered).

For a Hi-Speed device, the average current is measured in Hi- Speed and Full-Speed mode. All Hi-Speed measurements are performed by connecting the DUT after one self-powered Hi-Speed hub. A Full-Speed self-powered hub is connected to the first Hi-Speed hub in order to force a Hi-Speed DUT to enter its Full-Speed mode.

A device must also be measured using the supported power mode in the following circumstances:

- 1. When a device is only capable of operating in self-powered mode, all measurements are performed in selfpowered mode. It means that the device is unable to enumerate without being connected to an external power.
- 2. When a device is capable in operating in bus-powered mode, all measurements are performed in buspowered mode even when the device claims to be self-powered (in its device descriptor).
- 3. When a device has battery-charging capabilities over USB, the power measurements are performed in worst case scenario, most probably it is when the product has a dead battery.

Test Items:

- Unconfigured Current
- Configured Current
- Active Current
- Suspend Current

Test Requirements:

Table 18. USBCV Current requirements

Device State	Measurement Current	Requirement	Device Feature
Unconfigured	0.17 mA	<=100 mA	All peripheral devices
Configured		<=bMaxPower 26 <=100 mA	Low-power Bus-powered Device
	0.17 mA	<=bMaxPower<=100 mA	Self-powered Device
		<=bMaxPower<=500 mA	High-power Bus-powered Device
Active		<=100 mA	Low-power Bus-powered Device
		<=500 mA	High-power Bus-powered Device
	0.17 mA	<=100 mA	Self-powered Device
Suspend		<0.5 mA	Remote Wake-up Unsupported Device
	0.17 mA	<2.5 mA	Remote Wake-up Supported Device
Powered' State Suspend	0.17 mA	<2.5 mA	Battery Charging Not supported Device
		<100 mA	Battery Charging supported Device

Note:

- bMaxPower is defined as the maximum power consumption of the USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units.
- i.MX series acts as a Self-powered device in Device Mode.

4.4.1 Unconfigured/Configured current test

The USB 2.0 DUT is set in unconfigured/configured state by using the tool USB20CV. For a USB 3.0 device, the unconfigured/configured state can be forced by using <u>USB30CV</u>.

Test Instructions:

1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, as shown in <u>Figure 129</u> below, be sure to use the gold-tree HS Hub.

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- 2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
- 3. Run USB20CV on Computer, select **Current Measurement Test**, and then click **Run** button to launch the tests.
- 4. Select the DUT in the list, click OK.
- 5. A pop-out dialog asks you to measure the **Unconfigured Current**, as shown in <u>the figure</u> below. After recording the maximum current value, click OK.
- 6. Another pop-out dialog asks you to measure the **Configured Current**, as shown in the figure below.
- 7. Record the maximum current value, then click OK to finish the test.



Select Test Mode	
Compliance Test Prompt for Test Parameters Debug	Test log initialized. User Input module initialized Windows 7 (Build 7601) Service Pack 1.0
Select Test Suite Chapter 9 Tests Current Measurement Test Device Summary HID Tests Hub Tests MSC Tests CTC Tests Select Test Select Test CTC Tests CTC Tests CTC Tests CTC Tests CTC Tests CTC Configuration CTC Tests CTC Configuration Descriptor Test - Devic Configured Current CTC Configured Current CTC Configured Current CTC Configured Current	CVExe.exe ver 1.4.7.0 CommandVerifierLog.dll ver 1.4.8.0 TSMFCGuiDialogHeiperDLL.dll ver 1.4.7.0 TestSuiteEngine.dll ver 1.4.7.0 EhoTestServices.dll ver 1.4.10.2 USBUtlities.dll ver 1.4.10.2 USBUtlities.dll ver 1.4.5.0 StackSwitcher.dll ver 1.4.5.1 USBCommandVerifier.dll ver 1.4.10.2 Correct Host. DCL bus 0. device 30 Section ion 0 a5c, PID=5800 red Current now. Hit OK to proceed OK
	evice to Unconfigured state: Number of: Fails (0); Aborts (0); Warnings (0)]
Optional Test Description Abort Launch Report Viewer Goto Reports Directory	Update Display Exit
Figure 130.	,

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Select Test Mode Compliance Test Debug	EhdTestServices.dll ver 1.4.10.2 USBUtilities.dll ver 1.4.5.0 StackSwitcher.dll ver 1.4.5.1
elect Test Suite	USBCommandVerifier.dll ver 1.4.10.2 Current Host: PCI bus 0, device 29, function 0
urrent Measurement Test evice Summary	Number of ports: 2 = Host selected: PCI bus 0, device 29, function 0 DUT selected: FS Device addr=2: VID=0a5c, PID=5800
USB 2.0/eHCI Comma ISC Tests ISC Tests IS	nd Verifier Current for configuration [0] now. Validate with ue reported in Config Descriptor shown in the DK to proceed evice to Unconfigured state: ngs (0)]
Display Check Unconfigured Current Messa Display Check Unconfigured Current Messa Origuration: Origuration Descriptor Test - Device Con Origured Current	OK Invalid configuration value : 0
Online of Test Description	 (1.1.2) Devices must support being set to Addressed/Configured state. Stop time: Tue Jul 07 17:35:12 2015 Duration: 1 second. Stopping Test [Configuration Descriptor Test (Configuration Index 0): Number of: Fails (1); Aborts (1); Warnings (0)]
Abort Launch Report Viewer Goto Reports Director	V Undate Display

4.4.2 Active current test

The USB 2.0 DUT is operating correctly and during operation, the device current is measured in worst-case power consumption mode. The active current must remain below the value defined in the bMaxPower field of the descriptor.

Test Instructions:

- 1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
- 2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
- 3. Operation the DUT, for example: Copy a file from computer to DUT which is enumerated as MSC Device, after the copy is finished, recopy the file to computer, in the meantime, copy another file from computer to DUT.
- 4. Record the maximum current value during the bi-direction copying period.

4.4.3 Suspend current test

The USB 2.0 DUT is suspended after it is correctly enumerated by the host system. If the device supports remote wake-up, this feature must be enabled during measurement.

Test Instructions:

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- 1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
- 2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
- After DUT is enumerated as MSC device, enter following command in Linux console to force DUT into suspend mode.
 echo mem > /sys/power/state
- 4. Record the maximum current value.

4.4.4 Suspend current powered state

Peripherals are required to support the suspend state whenever VBUS is powered, even if bus reset has not occurred.

This measurement is not the regular suspend current measurement as described above. Do not forget it!

Test Instructions:

- 1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
- 2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
- 3. Run USB20CV on Computer, select **Current Measurement Test**, and then click **Run** button to launch the tests.
- 4. Select the DUT in the list, click OK.
- 5. After the unconfigured and configured states are ended, do not switch off USBCV, deattach, and reattach the device and then measure the current.
- 6. Record the maximum current value, then click OK to finish the test.

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5 Interoperability tests

5.1 Device interoperability test

Device Interoperability test evaluates the device's ability to interoperate with the host system and coexist with other USB devices. It also provides some insight into usability issues of the device and associated software. See the detailed description of Embedded Host Interoperability Test, you can refer "**Interoperability**" part of "**Gold Suite Summary Test Procedure V1.35 Draft**".

Interoperability makes use of an arrangement of USB peripherals known as the "Gold Tree". The Gold Tree consists of these characteristics:

- · Provides isochronous, bulk, interrupt, and control traffic
- · Tests the device behind 5 levels of nested hubs the maximum allowed
- Tests the device up to 30 meters from the host the maximum allowed
- · Contains a high-speed branch and full-speed speed branch
- EHCI, UHCI, and OHCI controllers available for testing

The Gold Tree is supposed to consist of USB-IF certified consumer devices that are widely available in the market. Unfortunately, the shelf-life of consumer products is limited and some items become difficult to find as time goes by. So if a specific gold tree device cannot be obtained, it may be substituted with a similar, certified device.

Item	Class	Description	Example Product	Qty
USB Host System		Multicore processor Certified USB EHCI with integrated UHCI Certified USB xHCI	DELL XPS8700 (example)	1
EHCI / OHCI		PCI Host Adapter using certified USB EHCI with integrated OHCI	Adaptec, model AUA 4000 PCI adapter	1
xHCI (SuperSpeed host adapter)		PCI Host Adapter using certified USB xHCI	USB-IF SuperSpeed PDK	1
HS Hub (Self-powered)	Hub	Hi-speed hub. Minimum of 4 exposed downstream ports	Belkin F5U233	6
FS Hub (bus-powered)	Hub	Full-speed hub. Minimum of 2 exposed downstream ports (Likely to be a compound device)	Targus Numeric Keypad with 2-port Hub, model PAUK10U	1
USB mouse	HID	Low-speed using interrupt transport	Microsoft Basic Optical Mouse	1
HS Mass Storage	MSC	Hi-speed using bulk transport	Memorex TravelDrive model 3 2509051	2
PC Camera	UVC	Hi-speed using isochronous transport	Logitech QuickCam Ultra Vision P/N: 961471-0403	1
average current draw test jig		Fixture to measure current consumed from VBus	http://www.usb.org/ developers/adapters/	1
one meter (or shorter) USB cable		any listed on USB-IF Cables and Connectors Integrators List		1
4.5 meter USB cable with mini B-plug		any listed on USB-IF Cables and Connectors Integrators List		1

Table 19. Gold Tree Device List

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Item	Class	Description	Example Product	Qty
2 meter USB cable with micro USB B-plug		any listed on USB-IF Cables and Connectors Integrators List		1
five meter USB cables		any listed on USB-IF Cables and Connectors Integrators List		8

Table 19. Gold Tree Device List...continued

Test Items:

- Enumeration and driver installation
- Operation with default drivers
- Interoperability
- Hot Detach and Reattach
- Warm boot
- Remote wake-up Test 28
- S3 Active Suspend Test
- S3 Active Suspend Resume Test
- Root Port Test
- S4 Active Hibernate Test
- S4 Active Hibernate Resume Test
- Topology change UHCI 2 9
- Topology change OHCI 29
- Topology change XHCI

Test Report:

 Table 20. Device Interoperability Test Report

Num	Test Item	Result
1	Enumeration and driver installation	Pass
2	Operation with default drivers	Pass
3	Interoperability	Pass
4	Hot Detach and Reattach	Pass
5	Warm boot	Pass
6	Remote wake-up Test	N/A
7	S3 Active Suspend Test	Pass
8	S3 Active Suspend Resume Test	Pass
9	Root Port Test	Pass
10	S4 Active Hibernate Test	Pass
11	S4 Active Hibernate Resume Test	Pass
12	Topology change UHCI	Pass
13	Topology change OHCI	Pass
14	Topology change XHCI	Pass

Note:

- If the DUT supports Remote Wake-up, enable it to wake the system. If not, this test could be dismissed. i.MX is enumerated as MSC Device, so it does not support Remote Wake-up.
- Interoperability test on OHCI or UHCI is informational only and not required for the purposes of certification.

5.1.1 Enumeration and driver installation

Test Instructions:

- 1. Construct a tree of USB devices as shown in **Fig5-1 below**. Attach Hub HS1 to a root port on the **EHCI** motherboard. Attach the gold tree, via Hub HS2, to Hub HS1.
- 2. Plug in the DUT into the open port on the multi-TT Hub HS5.
 - Do NOT install any drivers or software prior to attaching the device
 - Use a 5 meter cable if the device does not have a captive cable
- If OS does not possess a native driver, follow OS instructions to install the driver. If driver still does not load

 install software as directed by vendor.
 - If driver loads, PASS with waiver and recommend the driver load via .INF file
 - If reboot is requested or required as a result of driver (or application) installation PASS with waiver and recommend removing reboot requirement
- 4. Check if DUT and other devices are enumerated.
- 5. **Pass** is considered when all following items meet:
 - DUT enumerates behind HS5 using a 5 meter cable or its own captive cable.
 - Driver installs with an *.INF* file (provided on a floppy or a CD) or is enumerated automatically by the system (class driver).
 - DUT does not require a reboot
 - DUT is correctly identified by Device Manager and no yellow exclamation point is shown for any device.
- 6. Fail is considered when any of the following items meets:
 - DUT cannot be installed because it requires driver installation or application software before DUT is ever plugged in.
 - DUT does not enumerate below hub #5.
 - Driver blue screens during enumeration.
 - DUT requires reboot.
 - DUT is incorrectly identified by Device Manager or a device is flagged as not operational (yellow exclamation point).

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5.1.2 Operation with default drivers

Test Instructions:

- 1. DUT demonstrates correct operation using default driver connected to Hub #5 with the 5 meter cable (if cable not captive).
- 2. Check if DUT and other devices are enumerated.
- 3. Pass is considered when all following items meet:
- DUT operates as expected with the 5 meter cable (if cable not captive).
- 4. Fail is considered when any of the following items meets:
 - DUT cannot be installed because it requires driver installation or application software before DUT is ever plugged in.

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- DUT fails to operate.
- Device/ Application blue screens or crashes system.
- Device fails to operate as expected below Hub #5.

5.1.3 Interoperability

Test Instructions:

- 1. Operate all the devices in Gold Tree. Verify that the DUT functions correctly while all other devices are operating concurrently.
 - · Operate the device under test
 - View live video from the Veo camera
 - Transfer a large file between the Maxtor drive and the JumpDrive Pro
 - Strike keys on the Logitech keyboard
 - Disconnect and reconnect the Logitech mouse in the same port on Hub FS3
 - Move the Logitech Mouse verifying it still works
- 2. **Pass** is considered when all following items meet:
 - DUT operates as expected.
 - Gold Tree all devices operate well.
- 3. Fail is considered when any of the following items meets:
 - DUT fails to operate as expected.
 - One or more Gold Tree devices fail to operate.

5.1.4 Hot Detach and Reattach

Test Instructions:

- 1. Stop DUT operation!
- 2. Detach and reattach DUT to same hub port.
- 3. Test functionality of DUT only.
- 4. **Pass** is considered when all following items meet:
 - DUT operates as expected.
- 5. Fail is considered when any of the following items meets:
 - DUT fails to operate as expected.

5.1.5 Warm boot

Test Instructions:

- Stop operation of all devices!
- Restart the computer.
- · Check operation of all USB devices including DUT.
- Pass is considered when all following items meet:
 DUT operates as expected.
- Fail is considered when any of the following items meets:
 - Device fails to operate as expected.
 - One or more Gold Tree devices fail to operate.
- 5.1.6 Remote wake-up test

Test Instructions:

Application note

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- 1. If the [DUT] supports remote wake-up, enable the DUT to wake the system (Computer->Manage->Device Manager->DUT->Power Management); otherwise, go to S3 Active Suspend Tests.
- 2. While device under test is actively operating, suspend the system. (Start->Shutdown->Sleep, wait 5 10 seconds after monitor is dark)
- 3. If the system does not go into suspend, then a message must appear saying that the active DUT will not allow suspend to occur.
- 4. Use DUT to wake the system, check operation of all USB devices including DUT.
- 5. **Pass** is considered when all following items meet:
 - · System suspends and wakes up well.
 - All devices including DUT operate as expected.
- 6. Fail is considered when any of the following items meets:
 - System blue screens or locks up.
 - System can't suspend and wake up.
 - DUT fails to operate as expected.
 - One or more Gold Tree devices fail to operate.



5.1.7 S3 active suspend test

Test Instructions:

1. Disable remote wake-up on all USB devices, including DUT.

- 2. Operate the DUT while placing the system in suspend. (Start->Shutdown->Sleep, wait 5 10 seconds after monitor is dark)
- 3. If the system does not go into suspend, then a message must appear saying that the active DUT will not allow suspend to occur.
- 4. **Pass** is considered when all following items meet:
 - System suspends well.
 - System notifies user that it can't go into suspend.
- 5. Fail is considered when either of the following items meets:
 - System does not enter suspend without notification.
 - System blue screens or locks up.

5.1.8 S3 active suspend resume test

Test Instructions:

- 1. Place the system in suspend as **5.1.7** describes.
- 2. Wake the system.
- 3. Check operation of the DUT.
- 4. **Pass** is considered when all following items meet:
 - System resumes well.
 - Active operation initiated in previous step continues without error.
- 5. Fail is considered when either of the following items meets:
 - System does not resume.
 - System blue screens or locks up.
 - DUT is not functional or does not continue operation in the previous step.

5.1.9 Root port test

5.1.10 S4 active hibernate test

Test Instructions:

- 1. Stop operation of all devices!
- 2. Plug DUT into a root port of the system's motherboard.
- 3. Operate the DUT while the system enters hibernation (Start->Shutdown->Hibernate, wait 5 10 seconds after monitor is dark)
- 4. **Pass** is considered when all following items meet:
 - System hibernates well.
- 5. Fail is considered when any of the following items meets:
 - System fails to hibernate.
 - System blue screens or locks up.

5.1.11 S4 active hibernate resume test

Test Instructions:

- 1. Place the system in hibernation as **5.1.10** describes.
- 2. Turn on the system.

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- 3. Check operation of all USB devices including DUT.
- 4. **Pass** is considered when all following items meet:
 - System resumes well.
 - Active operation initiated in previous step continues without error.
- 5. **Fail** is considered when either of the following items meets:
 - System does not resume.
 - System blue screens or locks up.
 - DUT is not functional or does not continue operation in the previous step.

5.1.12 Topology change to UHCI

Test Instructions:

- 1. Change the **EHCI** motherboard to **UHCI** motherboard. Other connections are all the same. See Figure 133 above.
- 2. Run the whole tests from 5.1.1 to 5.1.11.
- 3. Record the test result.

5.1.13 Topology change to OHCI

Test Instructions:

- Change the **EHCI** motherboard to **OHCI** motherboard. Other connections are all the same. See Figure 133 above.
- Run the whole tests from 5.1.1 to 5.1.11.
- Record the test result.

5.1.14 Topology change to XHCI

Test Instructions:

- Change the **EHCI** motherboard to **XHCI** motherboard. Other connections are all the same. See Figure 133 above.
- Run the whole tests from 5.1.1 to 5.1.11.
- Record the test result.

5.2 Embedded host interoperability test

Targeted Hosts or OTG acting as a Host, are tested for interoperability with peripherals from the device's own Targeted Peripheral List plus other retail USB products which could be attached to the Targeted Host.

Silent failures are not allowed and therefore a clear message shall be generated when any sort of error situation occurs. For example, where hubs are non-supported, a clear "Hub not supported" or similar error message appears and not a generic "not supported" or similar error message.

See the detailed description of Embedded Host Interoperability Test, you can refer **Chapter 7** of "**USB On-The-Go and Embedded Host Automated Compliance Plan**".

Test Items:

- A-UUT Functionality B-device
- A-UUT Category Functionality B-device
- A-UUT Boot Test
- 7A-UUT Legacy Speed Test

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- A-UUT Concurrent and Independently Test
- A-UUT Unsupported device Message Test
- A-UUT Hub Error message Test
- A-UUT Hub Functionality Test
- A-UUT Hub maximum tier Test
- A-UUT Hub Concurrent and Independent Test
- A-UUT Bus powered hub power exceeded Test
- A-UUT Maximum concurrently device exceed message Test
- A-UUT Standby Test
- A-UUT Standby Disconnect Test
- A-UUT Standby Attach Test
- A-UUT Standby Remote Wake-up Test

Test Report:

Table 21. Embedded Host Interoperability Test Report

Num	Test Item	Result
1	7.3.1 A-UUT Functionality B-device 30	N/A
2	7.3.2 A-UUT Category Functionality B-device	Pass
3	7.3.3 A-UUT Boot test	Pass
4	7.3.4 A-UUT Legacy Speed test	Pass
5	7.3.5 A-UUT Concurrent and Independently test 31	N/A
6	7.3.6 A-UUT Unsupported device Message test	Pass
7	7.3.7 A-UUT Hub Error message test 3 2	<i>N/A</i>
8	7.3.8 A-UUT Hub Functionality test	Pass
9	7.3.9 A-UUT Hub maximum tier test	Pass
10	7.3.10 A-UUT Hub Concurrent and Independent test	Pass
11	7.3.11 A-UUT Bus powered hub power exceeded test	Pass
12	7.3.12 A-UUT Maximum concurrently device exceed message test	Pass
13	7.3.13 A-UUT Standby test	Pass
14	7.3.14 A-UUT Standby Disconnect test	Pass
15	7.3.15 A-UUT Standby Attach test	Pass
16	7.3.16 A-UUT Standby Topology Change test	Pass
17	7.3.17 A-UUT Standby Remote Wake-up test	Pass

Note:

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- *i.MX* does not support peripherals identified by their VID/PID, so this test is not needed.
- Concurrent and Independently test is only applied to EH with multi ports, i.MX6 EVK only have one downstream port, so this test is not needed.
- *i.MX* supports Hub, so this test is not needed.

5.2.1 A-UUT functionality B-device

Table 22. A-UUT Functionality B-device

Purpose	Prove the functionality of an OTG A-device or EH
Applies to	OTG A-devices and EH's that perform VID/PID detection of TPL peripherals
Description	Test the functionality of the TPL peripherals
Test setup	At least one TPL device corresponding to each supported category
Preconditions	The A-UUT is powered ON

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Table 22.	A-UUT	Functionality	B-device	continued
	A-001	i unctionality	D-ucvicc	commueu

	Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	TPL2-4, TPL7
Pass Criteria	Prove the functionality of all TPL B-devices in combination with the A-UUT

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a B-device taken from the TPL and prove functionality.
- 3. Detach the B-device and see if the device is disconnected correctly.
- 4. Attach the B-device and prove functionality.
- 5. Repeat the above steps for each of the different supported category.
- 6. End of test.

5.2.2 A-UUT category functionality B-device

Table 23.	A-UUT	Category	Functionality	B-device
		outogoi j		

Purpose	Prove the category functionality of an OTG A-device or EH
Applies to	OTG A-devices and EH's that support a certain category of device
Description	Test the functionality of each of the supported categories
Test setup	 One B-device of each supported category with 500 mA in their descriptor, if not available use a device with highest max power descriptor value. If available one B-device of each supported category with an additional interface(s) (composite device). If not available use a device with one interface.
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	MSG2, MSG3, TPL2-4, TPL7
Pass Criteria	Prove the functionality of the B-devices in combination with A-UUT For the composite device, it is not mandatory to prove functionality however if the device does not operate a clear message shall be generated by the A-UUT. If a device does not work a clear error message shall be shown to the user.

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a B-device taken and prove functionality.
- 3. Detach the B-device and see if the device is disconnected correctly.
- 4. Attach the B-device and prove functionality.
- 5. Repeat the above steps for each of the different supported category with five different peripherals.
- 6. End of test.

5.2.3 A-UUT boot test

Table 24. A-UUT Boot Test

Purpose	Prove the functionality of an OTG A-device or EH after boot	
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Table 24. A-OOT DOOL Testcommuned	
Applies to	OTG A-devices and EH's
Description	Observe boot behavior while a B-device is attached
Test setup	One B-device of each supported category.
Preconditions	The A-UUT is powered OFF Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C3
Pass Criteria	Prove the functionality of the B-devices in combination with A-UUT For the composite device it is not mandatory to prove functionality however if the device does not operate a clear message shall be generated by the A-UUT. If a device does not work a clear error message shall be shown to the user.

Table 24. A-UUT Boot Test...continued

Test Instructions:

- 1. Power OFF the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a B-device taken and prove functionality.
- 3. Power ON the A-UUT.
- 4. Prove functionality of the B-device.
- 5. Repeat the above steps for each of the different supported category.
- 6. End of test.

5.2.4 A-UUT legacy speed test

Table 25. A-UUT Legacy Speed Test

Purpose	Prove the functionality of the OTG A-device or EH in Full or Low-Speed
Applies to	High-Speed OTG A-devices and EH's that have a Full or Low-Speed device on their TPL. Perform this test only if it not has been performed in one of the previous tests.
Description	Test the functionality of the Full or Low-Speed TPL device
Test setup	One supported Full Speed (Full Speed support is mandatory) or Low-speed device
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	E15, E18
Pass Criteria	The functionality of the full or low-speed device is proven. If a device does not work a clear error message shall be shown to the user.

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a Full Speed B-device and prove functionality.
- 3. End of test.

5.2.5 A-UUT concurrent and independently test

Table 26. A-UUT Concurrent and Independently Test

Table 20. A doll denoutont and macponaently root						
Purpose Prove the functionality of all downstream ports						
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Table 26.	A-UUT	Concurrent	and	Independently	Testcontinue	d
-----------	-------	------------	-----	---------------	--------------	---
-----------	-------	------------	-----	---------------	--------------	---

Applies to	EH with multiple ports
Description	Test the concurrent and independent functioning of the TPL peripherals on each downstream port.
Test setup	For each downstream port, a similar device from the TPL. If detection is made using VID/PID and/or for category support the number of B-devices is equal to the number of ports. This test shall be performed on each supported category.
Preconditions	The A-UUT is powered ON
Checklist	E17
Pass Criteria	The A-UUT can operate the device concurrently and independently or a selection method is available for the end-user to select a device. An A-UUT is allowed to handle a limited number of concurrent peripherals

Test Instructions:

- 1. Power ON the A-UUT.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a B-device to Port 1.
- 3. Attach another B-device of the same category to an available downstream port.
- 4. Continue attaching B-devices of the same category until all ports are full.
- 5. Prove functionality of each attached B-device.
 - Do they operate concurrently and independently.
 - Or is a selection method available such that the user can select the active B-device.
- 6. Remove one device and replace it with a device of another category if multiple categories are supported.
- 7. Remove all peripherals.
- 8. Repeat the above steps for each of the different supported category.
- 9. End of test.

5.2.6 A-UUT unsupported device message test

Table 27. A-UUT Unsupported device Message Test

Purpose	Prove that the OTG A-device or EH generates the correct error message when attaching an unsupported device
Applies to	OTG A-devices and EH's
Description	Observe error messages when attaching unsupported peripherals
Test setup	 One unsupported Low-speed device One unsupported Full-speed device One unsupported High-speed device One unsupported Super-speed device One unsupported composite device with more than 8 interfaces
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	E15, E18
Pass Criteria	The functionality of the full or low speed device is proven. If a device does not work a clear error message shall be shown to the user.

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach one of the peripherals listed above.

- 3. Observe if a clear message is generated to the end-user.
- 4. Repeat the above steps for each of the peripherals listed in the Test setup.
- 5. End of test.
- 6. Note that an error message should be generated when attaching a device in a device class which is not already covered by a product on the TPL. It is not permitted to support device classes without listing corresponding products on your TPL.

5.2.7 A-UUT hub error message test

Table 28.	A-UUT	Hub	Error	message test	t

Purpose	Prove that the OTG A-device or EH generates the correct error message when attaching an unsupported device
Applies to	OTG A-devices and EH's
Description	Observe error messages when attaching unsupported peripherals
Test setup	 One unsupported Low-speed device One unsupported Full-speed device One unsupported High-speed device One unsupported Super-speed device One unsupported composite device with more than 8 interfaces
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	E15, E18
Pass Criteria	The functionality of the full or low speed device is proven. If a device does not work, a clear error message shall be shown to the user.

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach the hub.
- 3. A clear hub not supported message should appear.
- 4. Attach a TPL device downstream from the hub.
- 5. Check that the device does not function downstream from the hub.
- 6. End of test.

5.2.8 A-UUT hub functionality test

Table 29. A-UUT Hub Functionality test

Purpose	Prove that a hub attached to an OTG A-device or EH hub either functions or causes a hub error message
Applies to	OTG A-devices and EH's which support hub(s)
Description	Test the hub functionality with TPL peripherals
Test setup	 One 4-port High-Speed Self-Powered Hub (If hub support is performed by VID/PID in TPL use this Hub) At least one TPL device from each category FS device if listed on TPL (for TT stress)
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	TPL4, MSG2, MSG3, MSG5
Pass Criteria	Prove the functionality of the all device categories listed in TPL attached downstream from one hub
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Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach the hub.
- 3. Attach one supported High-speed device downstream from the hub and prove its functionality.
- 4. Prove the functionality of each supported category downstream from one hub.
- 5. Detach the high-speed device.
- 6. Attach one supported Full speed device (if supported) downstream from the hub and prove its functionality.
- 7. Detach the full speed device.
- 8. End of test.

5.2.9 A-UUT hub maximum tier test

Table 30. A-UUT Hub maximum tier test

Purpose	Prove that a hub attached to an OTG A-device or EH hub either functions or causes a hub error message
Applies to	OTG A-devices and EH's which support hub(s)
Description	Test the hub functionality with TPL peripherals
Test setup	 One 4-port High-Speed Self-Powered Hub (If hub support is performed by VID/PID in TPL use this Hub) At least one TPL device from each category FS device if listed on TPL (for TT stress)
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	TPL4, MSG2, MSG3, MSG5
Pass Criteria	Prove the functionality of the all device categories listed in TPL attached downstream from one hub

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
- 2. Attach hubs up to the maximum tier.
- 3. Attach one TPL device downstream from the last hub and prove functionality.
- 4. Attach another hub downstream from the max tier of hubs.
- 5. Check that an appropriate error message is generated.
- 6. End of test.

5.2.10 A-UUT hub concurrent and independent test

Table 31. A-UUT Hub Concurrent and Independent test

Purpose	Prove that a hub attached to an OTG A-device or EH hub either functions or causes a hub error message
Applies to	OTG A-devices and EH's which support hub(s)
Description	Test the hub functionality with TPL peripherals
Test setup	 One 4-port High-Speed Self-Powered Hub (If hub support is performed by VID/PID in TPL use this Hub) At least one TPL device from each category

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	- FS device if listed on TPL (for TT stress)	
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.	
Checklist	TPL4, MSG2, MSG3, MSG5	
Pass Criteria	Prove the functionality of the all device categories listed in TPL attached downstream from one hub	

Table 31. A-UUT Hub Concurrent and Independent test...continued

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a B-device to the hub's downstream port 1.
- 3. Attach similar peripherals to available downstream hub ports.
- 4. Prove the functionality of each attached device.
 - · Do they operate concurrently and independently
 - Or is a selection method available such that the user can select the active device?
- 5. Detach one device and replace it with a device of another category if multiple categories are supported.
- 6. Detach all peripherals.
- 7. Repeat the above steps for each of the different supported category.
- 8. End of test.

5.2.11 A-UUT bus-powered hub power exceeded test

Table 32. A-UUT Bus powered hub power exceeded test

· ·	
Purpose	Prove that the host generates an appropriate error message when connecting a high-power device downstream from a bus-powered hub.
Applies to	OTG A-device and EH's which support bus powered hubs.
Description	Check that the A-UUT is able to detect and prevent an over current event on a bus-powered hub.
Test setup	A bus powered hub. High-power device from the TPL (Max power descriptor >100 mA). If no high-power device is available on TPL, use other high-power devices.
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C5
Pass Criteria	An appropriate error message was generated.

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a bus powered Hub.
- 3. Attach a high-power device downstream from a bus powered hub.
- 4. Check that an appropriate error message is generated by the A-UUT.
- 5. End of test.

5.2.12 A-UUT maximum concurrently device exceed message test

Table 33. A-UUT Maximum concurrently device exceed message test

Purpose	OTG A-devices and EH's which support a limited number of peripherals concurrently
Applies to	Test the A-UUT for appropriate behavior when exceeding the maximum number of supported concurrent peripherals up to a maximum of four.
Description	May require hubs to be attached in order to exceed maximum number of peripherals. The number of similar peripherals that the A-UUT is able to handle concurrently plus one up to a maximum of four.
Test setup	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Preconditions	MSG1, MSG2, MSG7
Checklist	Prove that the specified maximum number of concurrent peripherals function correctly, and either that an error message is given when exceeding this number or that it is able to handle 4 peripherals.
Pass Criteria	An appropriate error message was generated.

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a B-device and prove its functionality.
- 3. Keep increasing the number of similar peripherals attached until the maximum number is reached, proving their functionality each time.
- 4. Attach an additional similar peripherals.
- 5. Check that an appropriate error message is generated by the A-UUT or that it is able to handle 4 peripherals without error.
- 6. End of test.

5.2.13 A-UUT standby test

Table 34. A-UUT Standby test

Purpose	Prove that the host can handle standby correctly
Applies to	OTG A-devices and EH products which support standby
Description	With a B-device connected, verify standby operation of the A-UUT.
Test setup	At least one TPL device from each category
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a B-device and prove its functionality.
- 3. Place the A-UUT in standby (follow the A-UUT vendor guidelines to force the host into standby mode).
- 4. Take the A-UUT out of standby mode (A-UUT may also come out of standby automatically on detach).

- 5. Prove the functionality of the B-device.
- 6. Repeat the above steps for each of the different supported category.
- 7. End of test.

5.2.14 A-UUT standby disconnect test

 Table 35. A-UUT Standby Disconnect test

Purpose	Prove the standby functionality of the OTG A-device or EH when a peripheral is detached during standby mode
Applies to	OTG A-devices and EH's which support standby
Description	Detach TPL peripheral while A-UUT is in standby mode. Verify that the A-UUT operates correctly after the A-UUT leaves standby mode.
Test setup	At least one TPL peripheral
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed.

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a peripheral and prove its functionality.
- 3. Place A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
- 4. Detach Peripheral.
- 5. Take the A-UUT out of standby (A-UUT may also come out of standby automatically on detach).
- 6. Verify that A-UUT operates correctly.
- 7. If different types of standby modes are supported repeat the test until all modes have been tested.
- 8. End of test.

5.2.15 A-UUT standby attach test

Table 36. A-UUT Standby Attach test

Purpose	Prove the standby functionality of the OTG A-device or EH when a peripheral is attached during standby mode
Applies to	OTG A-devices and EH's which support standby
Description	Attach a TPL peripheral while the A-UUT is in standby mode. Verify that A-UUT operates correctly after the A-UUT leaves standby mode
Test setup	At least one TPL peripheral
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed.

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.

- 2. Place the A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
- 3. Attach Peripheral.
- 4. Take the A-UUT out of standby mode (A-UUT may also come out of standby automatically on attach).
- 5. Verify that A-UUT behaves normally.
- 6. Prove the functionality of the peripheral.
- 7. If different types of standby modes are supported repeat the test until all modes have been tested.
- 8. End of test.

5.2.16 A-UUT standby topology change test

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Purpose	Prove the standby functionality of the OTG A-device or EH when the topology changes during standby.
Applies to	OTG A-devices and EH's which support standby
Description	Switch the topology of TPL peripherals while the A-UUT is in standby, verify that the A-UUT does not behave abnormally after the A-UUT leaves standby mode
Test setup	At least one TPL peripheral
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed.

Table 37. A-UUT Standby Topology Change test

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach a hub (if necessary)
- 3. Attach the B-device and prove functionality.
- 4. Place the A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
- 5. Detach the B-device and attach it to another EH port or another downstream hub port.
- 6. Take the A-UUT out of standby mode standby (A-UUT may also come out of standby automatically on attach).
- 7. Verify that A-UUT behaves normally.
- 8. Prove functionality of the B-device.
- 9. If different types of standby modes are supported repeat the test until all modes have been tested.
- 10. End of test.

5.2.17 A-UUT standby remote wake-up test

· · · · · · · · · · · · · · · · · · ·	
Purpose	Prove the remote wake-up functionality of an OTG A-device or EH
Applies to	OTG A-devices or EH's which support standby and remote wake-up.
Description	Perform a USB remote wake-up event and verify that the A-UUT operates correctly after the A-UUT leaves standby mode.
Test setup	At least one TPL peripheral which supports remote wake-up.
Preconditions	The A-UUT is powered ON. Use Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2

Table 38. A-UUT Standby Remote Wake-up test

Table 38. A-UUT Standby Remote Wake-up test...continued

	-	-	
Pass Criteria			Compliant standby behavior is observed when a remote wake-up event is performed during
			standby.

Test Instructions:

- 1. Power ON the A-UUT.
 - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
 - If the B-device requires external power, power on the B-device.
- 2. Attach the B-device.
- 3. Prove the functionality of the A-UUT with the B-device.
- 4. Put the A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
- 5. Perform a USB remote wake-up event from the B-device.
- 6. Prove the functionality of the A-UUT with the B-device.
- 7. End of test.

6 Auto PET tests

6.1 Introduction of PET

The PET (Protocol and Electrical Tester) is a unit, designed to perform compliance testing or assist with development work leading toward compliance testing on On-the-Go, Battery Charging and other general USB applications.

The tests in this section test only a partial list of all the possible parameters and compliant behavior. The tests should not be considered as a full validation test plan. See the detailed description of PET Test, you can refer **Chapter 6** of "**USB On-The-Go and Embedded Host Automated Compliance Plan**".

The Packet-Master USB-PET is used by most of the Compliance Test Labs, which is delivered complete with MQP's Windows application *GraphicUSB* for generating the test reports, and also analyzer-style captures.



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6.2 Test environment

6.2.1 Test cables required

The cables required by the PET tester are described below.

Each cable should be labeled, and specify the lead loop resistance value, required to be entered into the test dialog, if the cable is replaced. The tester application contains a checkbox to specify whether the UUT has a captive cable, as in this case the captive test cable is deemed to be part of the unit under test.

Table 39. Special Test Cable A

Micro-B plug to Micro-B plug			
Micro-B plug (PET)	Micro-B plug (UUT)	Purpose	
1	1	VBUS	
2	2	D-	
3	3	D+	
4	4	ID	
5	5	GND	

Table 40. Special Test Cable B

Micro-B plug to Standard-A plug			
Micro-B plug (PET)	Standard-A plug (UUT)	Purpose	
1	1	VBUS	
2	2	D-	
3	3	D+	
nc			
5	4	GND	

6.2.2 Test setups

The cables required by the PET tester are described below.

Each cable should be labeled, and specify the lead loop resistance value, required to be entered into the test dialog, if the cable is replaced. The tester application contains a checkbox to specify whether the UUT has a captive cable, as in this case the captive test cable is deemed to be part of the unit under test.

OTG device as Unit-Under-Test

When running a test-suite relating to an OTG device, the first test prompts you to attach it to the PET using 'Special Cable A'.

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Embedded Host as Unit-Under-Test

When running a test-suite relating to an Embedded Host using a Standard-A receptacle, the first test prompts you to attach it to the PET using 'Special Cable B'.

When running a test-suite relating to an Embedded Host using a Micro-AB receptacle, the first test prompts you to attach it to the PET using 'Special Cable A'.

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Peripheral Only as Unit-Under-Test

When running a test-suite relating to a Peripheral-Only OTG device, the first test prompts you to attach it to the PET using 'Special Cable A'.

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6.2.3 User input before test runs

Before running any test suite, the PET must be informed of a number of parameters by the test operator. Most of the information should be available from the Checklist supplied by the vendor. The following tables describe the information required. Typically, PET software would modify the available options to the ones applying to the currently chosen device type.

Input	Туре	Purpose	Checklist Ref
OTG Device	Mutually exclusive check boxes	Automatically selected by UUT items OTG-A or OTG-B.	PI2
Embedded Host		Automatically selected by UUT item Embedded Host.	
Peripheral Only		Automatically selected by UUT item Peripheral Only.	
Uses Micro-AB	Checkbox	Check this box for an EH which uses a Micro-AB receptacle instead of a Standard-A receptacle. It is automatically selected for OTG devices.	PI5a
Supports Sessions	Checkbox	Check this box if the OTG A-UUT or EH with Micro-AB receptacle does not keep VBUS enabled all the time that the ID pin is held low. Check this box for an EH with Standard-A receptacle which does not keep VBUS high all the time it is powered up. In either case, it is assumed that SRP or ADP is available to detect the presence of a device.	PI10
SRP as A-device	Checkbox	Check this box if the UUT, as an A-device, supports detecting, and acting on, an SRP pulse generated by a connected device.	PI13
HNP as A-device	Checkbox	Check this box if the UUT, as an A-device, supports HNP to enable the connected B-device to become host if it so requires.	PI13
HNP Polling as A-device	Checkbox	Check this box if the UUT, as an A-device, supports HNP polling. If it does, it is allowed to remain as host, for as long as the other device does not set its Host Request Flag.	PI13

Table 44	Information			Charleliat
Table 41.	information	Optained	From	Checklist

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Input	Туре	Purpose	Checklist Ref
ADP as A-device	Checkbox	Check this box if the UUT, as an A-device, supports ADP probing to detect the presence or otherwise of a connected device.	PI13
SRP as B-device	Checkbox	Check this box if the UUT, as a B-device, supports generating an SRP pulse in order to start a session (cause the connected A-device to turn on VBUS).	PI20
HNP as B-device	Checkbox	Check this box if the UUT, as a B-device, supports HNP to allow it to become host if it so requires.	PI20
ADP as B-device	Checkbox	Check this box if the UUT, as a B-device, supports ADP sensing and probing to detect the presence or otherwise of a connected device.	PI20
FS Not Available	Checkbox	Check this box if UUT does not fully support full-speed operation. This is not permitted for an OTG device, but may be for an Embedded Host.	PI11, PI18
IA_VBUS_RATED	Edit box	The rated output current of an A-device in mA units.	PI8
bMaxPower	Edit box	bMaxPower (sic) is the highest current, in mA, declared in any of the device's Configuration Descriptors. This value ignores current drawn under the Battery Charging provisions.	PI17
TPWRUP_RDY	Edit box	Maximum time, in seconds, specified by vendor from powering on the UUT until it is ready to perform USB functionality. By default it is set to 30 seconds, but a vendor is permitted to specify a longer time.	PI24
TA_WAIT_BCON max	Edit box	The maximum time, in seconds, that VBUS is left on for by an A-device, in the absence of a B-device connecting. The default value is 30 seconds. A vendor is permitted to specify a longer time, but should be aware that this will have an impact on the time taken for, and therefore possibly the cost of, compliance testing.	PI10
Unknown Dev (No HNP)	Edit boxes	The test uses the VID/PID combination specified during tests for error messages, when an unknown B-device, not capable of HNP, is connected. A default value (1A0A/0201) is used, but any other device not on the UUT's TPL may be defined here.	-
Unknown Dev (HNP)	Edit boxes	The test uses the VID/PID combination specified during tests for error messages, when an unknown B-device, capable of HNP, is connected. A default value (1A0A/0202) is used, but any other device not on the UUT's TPL may be defined here.	-

Table 41. Information Obtained From Checklist...continued

6.3 A-UUT tests

Test Items:

- A-UUT VBUS Voltage and Current Measurements
- A-UUT Bypass Capacitance
- A-UUT SRP
- A-UUT ADP
- A-UUT Leakage
- EH, Capable of ADP and SRP, State Transition Test (Standard-A)
- EH, Capable of ADP but not SRP, State Transition Test (Standard-A)
- EH, Capable of SRP but not ADP, State Transition Test (Standard-A)
- EH with no Session Support State Transition Test (Standard-A)
- EH, Capable of ADP and SRP, (Micro-AB) or OTG-A, Capable of ADP and SRP but not HNP, State Transition Test
- EH, Capable of ADP but not SRP, (Micro-AB) or OTG-A , Capable of ADP but not SRP or HNP, State Transition Test
- EH, Capable of SRP but not ADP, (Micro-AB) or OTG-A , Capable of SRP but not ADP or HNP, State Transition Test

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- EH with no Session Support State Transition Test (Micro-AB), or OTG-A with no Session or HNP Support
- A-UUT "Device No Response" for connection timeout
- A-UUT "Unsupported Device" Message
- A-UUT "Device No Response" for HNP enable
- EH using Micro-AB "Incorrect Connection"

Test Report:

Table 42. PET A-UUT Test Report

Num	Test Item	Result
1	6.7.2 A-UUT Initial Power-up Test	Pass
2	6.7.4 A-UUT VBUS Voltage and Current Measurements	Pass
3	6.7.5 A-UUT Bypass Capacitance	Pass
4	6.7.6 A-UUT SRP	Pass
5	6.7.8 A-UUT ADP	Pass
6	6.7.9 A-UUT Leakage	Pass
7	6.7.14 EH, Capable of ADP and SRP, State Transition Test (Standard-A)	N/A
8	6.7.15 EH, Capable of ADP but not SRP, State Transition Test (Standard-A)	N/A
9	6.7.16 EH, Capable of SRP but not ADP, State Transition Test (Standard-A)	N/A
10	6.7.17 EH with no Session Support State Transition Test (Standard-A) 33	Pass
11	6.7.18 EH, Capable of ADP and SRP, (Micro-AB) or OTG-A , Capable of ADP and SRP but not HNP, State Transition Test	N/A
12	6.7.19 EH, Capable of ADP but not SRP, (Micro-AB) or OTG-A , Capable of ADP but not SRP or HNP, State Transition Test	N/A
13	6.7.20 EH, Capable of SRP but not ADP, (Micro-AB) or OTG-A , Capable of SRP but not ADP or HNP, State Transition Test	N/A
14	6.7.21 EH with no Session Support State Transition Test (Micro-AB), or OTG-A with no Session or HNP Support	N/A
15	6.7.22 A-UUT "Device No Response" for connection timeout	Pass
16	6.7.23 A-UUT "Unsupported Device" Message	Pass
17	6.7.24 A-UUT "Device No Response" for HNP enable	N/A
18	6.7.25 EH using Micro-AB "Incorrect Connection" 34	N/A

Note:

- *i.MX* Embedded Host contains a standard Type A receptacle, and it does not support ADP, SRP, HNP, session. So, only 6.7.17 should be test.
- Only Embedded Host using Micro-AB receptacle must run this test.

- Install and run *GraphicUSB* on computer.
- Click Operation -> Compliance Tester on the menu bar. The Test Suite dialog appears as shown in Figure 139 below.
- Select the type of unit 1 to be tested using the **Unit Under Test** combo box.
- Then refer to the completed Compliance Checklist, and ensure that the other **Unit Under Test** checkboxes and parameters are correctly entered.
- The appropriate tests are loaded into the 'Selected Tests' list box. These tests are now ready to automatically run in sequence.
- Specify a Product name so that the reports can be saved into an appropriate folder.
- Click Run to start the test suite.
- A text report file is created, into which the test results are written, as shown in Fig6-5 below.

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LICD DET Test Suites
OTG 2.0 and BC 1.2 Device Emulator Command Verifier
Unit Under Test
Embedded Host IA_VBUS_RATED: 100 mA Image: Do Analyser Capture C OTG Device © Embedded Host Uses Micro-AB bMaxPower 100 mA Image: Dobug
C Peripheral Only Supports Sessions TPWRUP_RDY 30 sec Save Info Only C SRP as A-device LS TA_WAIT_BCON max 30 sec Cable A 230 mOhm HNP as A-device FS Not Available IMAX_BC: 1500 mA Cable B 500 mOhm HNP polling as A-device DM v VLGC during Prim.(Info Only) VID PID Product:/Folder Name SRP as B-device Secondary Detection VID PID Product Product
ADP as B-device ALA Detection ONIX Dev (NO HNP) TABLE (2010 h
UnKn Dev (HNP) 1AUA U2U2 h
Script Folder C:\Users\b38367\AppData\Roaming\GraphicUSB\PET Scripts - Official\OTG_2_0_BC_1_2\ Image: Complex state Available Tests Description CT_A_PUT.mpet A-UUT Power-Up Tests
CT_A_VB0S.mpet A-001 Volds voldage and current Measurement CT_A_CAP.mpet A-UUT Bypass Capacitance CT_A_SRP.mpet A-UUT SRP CT_A_HNP.mpet A-UUT HNP CT_A_ADP.mpet A-UUT ADP CT_A_KG.mpet A-UUT Leakage CT_A_ST_OTG_ADP.mpet A-OTG_capable of ADP and SRP. State Transition Test CT_A_ST_OTG_ADP.mpet A-OTG_capable of ADP and SRP. State Transition Test
Selected Tests Description V Remove Add Custom Remove All
CT_A_PUT.mpet A-UUT Power-Up Tests CT_A_VBUS.mpet A-UUT Vbus Voltage and Current Measurement CT_A_CAP.mpet A-UUT Bypass Capacitance CT_A_SRP.mpet A-UUT Bypass Capacitance CT_A_ADP.mpet A-UUT ADP CT_A_LKG.mpet A-UUT Leakage CT_A_ST_EH_ADP_motet EH (Standard-A), capable of ADP and SRP, State Transition Test CT_A_ST_EH_SPR_mpet EH (Standard-A), capable of ADP but not SRP, State Transition Test
High-speed Electrical Test Modes (Host)
SE0_NAK J K Test Packet SE0_NAK J Quick Check Suspend Dev_Desc Dev_Desc_Data K Test Packet Check
Run Cancel Apply Figure 139. USB-PET Test Suites

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20	iraphic	USB - [Re	port_Final_Test_0003*]		
;;;	<u>-</u> ile <u>E</u> dit	<u>⊻</u> iew <u>O</u>	perations <u>W</u> indow <u>H</u> elp		_ 8 ×
	🚅 🖡		. 💼 🚑 🐛 🖕 🛶 🔐 🗶 😤 🖳 🚖 🛅 🗛	G T 🕀 🔾 🤶 🛛	
1					
]]	/bus:	0.00	0V -		
Min	3129:				<u>^</u>
	3130:	ADP29:	When the A-device is ready to act in host or		
Ø	3131:		peripheral role does VBUS reach VOTG_SESS_VLD		
Ш	3132:		within TA_VBUS_ATT of an attachment event		
8	3133:		being detected by ADP unless an over-current		
-	3134:		condition is reached?	VFG (D)GG)	
	3136:			- ILS (FASS)	
	3137:	T18:	Is the device ready to perform USB activity at		
NAK	3138:		a time no longer than TPWRUP RDY from an		
Ш	3139:		identifiable powering on action or sequence of		
84	3140:		actions (e.g. switching on)?		
Max	3141:			- Vendor Declaration	
-	3142:		Number of untested checklist items = 0		
≚e	3143:		Number of failing checklist items = 1		
∇	3144:				
*	3145:	===End	of Script====================================		
	3146:		- 6 To - 1 Common		
27	3147:	===End	or lest sequence		
关	3140:		SIILT SIIMMARV		
筹	3150:	Pass -	CT & PUT.mpet		
	3151:	Pass -	CT A VBUS.mpet		
	3152:	Pass -	CT A CAP.mpet		
	3153:	Pass -	CT_A_SRP.mpet		
	3154:	Pass -	CT_A_HNP.mpet		
	3155:	Pass -	CT_A_LKG.mpet		
	3156:	Pass -	CT_A_ST_EH_ADP.mpet		
	3157:	Pass -	CT_A_ST_EH_ADP_NOSRP.mpet		
	3158:	Pass -	CT_A_ST_EHmpet		
	3159:	Pass -	CI_A_SI_EH_NOSESS.mpet		
	3161.	Page -	CT & UnsunDev mnet		
	3162:	Pass -	CT & NoResHnn.mnet		
	3163:	Pass -	CT & OTG REP.mpet		
	3164:				
	3165:	===End	of Report====================================		
	3166:				
	3167:				
	< 10				×
Ecr. 4	eln press	5 F1		In 3167, Col 0	
FOR H	eip, press	511		LI13167, COLU	

Figure 140. USB-PET Test Report

7 Type-C function/PD

TBD

8 Registers and operation guide

8.1 i.MX 6 USB PHY registers and software configurations

USB signal integrity depends on many factors, such as circuit design, PCB layout, Stack-up, Impedance. Each product might be different from another, so customers must fine-tune the parameters in order to obtain the best signal quality.

The test board has routed out two USB Ports: one OTG 33, one Host. Each of the port has several registers to adjust the signal voltage level, slew rate. See the detailed description of the registers in Freescale app note *AN4589: Configuring USB on i.MX 6 Series*.

Compared to standard Linux/Android release, you may need to do below software changes to implement the certification tests, i.MX 6 Series is applicable from imx_3.10.31_1.1.0 Linux BSP GA release, for the release before that, user may need to apply the related patches before doing below things, and some examples may be different for former releases, the user must change accordingly. See the detailed information in this document "How to do USB Compliance Test for 3.10.y kernel", you may download it from NXP community.

8.1.1 USBPHYx_TXn

The USB PHY Transmitter Control Register handles the transmit controls. Bit fields TXCAL45DP, TXCAL45DM, D_CAL are usually to adjust the output voltage amplitude.

Command samples:

```
/unit_tests/memtool 0x20c9010 1 // OTG Port Read register data35
/unit_tests/memtool 0x20cA010 1 // Host Port Read register data
/unit_tests/memtool 0x20c9010=0x1c060607 //write OTG PHY_TX36
/unit_tests/memtool 0x20cA010=0x1c060607 //write HOST_PHY_TX
```

Note:

- Software does not support full feature OTG currently, this port is used as Device or Embedded Host, selected by USB_ID.
- Remember connecting DUT to corresponding Host/Device before adjusting the registers, otherwise the
 operation might be invalid or cause system crash.

Name	USBPH	/x_TXn														
Description	The USE	8 PHY Tra	nsmitter C	ontrol Reg	gister han	dles the tr	ansmit co	ntrols.								
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
Field definitions	RSVD5			TX_EDG	ECTRL		TX_ SYNC_ INVERT	TX_ SYNC_ MUX	RSVD4		TXEN CAL 4 5DP	RSVD3	TXCAL4	5DP		
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	RSVD2 TXEN CAL 45DN RSVD1 TXCAL45DN RSVD0 D_CAL															
Signal Names	Descrip	tion														
TXCAL45DP	Bit fields increase Decode	TXCAL45 the DM/D to select a	DP and T P signals 45-Ohm	XCAL45D level. resistance	M allow f	or changir SB_DP ou	ng the resinted the resinted the test of t	stance of laximum r	the high-s esistance	peed term	nination. Ir	creasing	the termin	ation resis	stor value	will
TXCAL45DN	Decode	to select a	45-Ohm	resistance	to the US	SB_DN ou	tput pin. N	laximum r	esistance	= 0000.						
D_CAL	This field amplitud Resistor 0000 = 0 0111 = N 1111 = +	allows fo e of the tra Trimming 0.16 % lominal 25 %	r trimming ansmitted Code:	the curre signal will	nt referen increase	ce for the	high-spee	d driver. F	Reducing 1	the resista	nce increa	ases the d	river curre	ent and the	erefore the	2

Table 43. USBPHYx_TXn Register Settings

8.1.2 PMU_REG_3P0

This register defines the control and status bits for the internal LDO_USB module, which is powered by either of the two USB VBUS pins. This regulator supplies only low-speed and full speed transceivers of USB PHYs, so it only impacts the voltage level of Full-speed and Low-speed transmission, but not the Hi-speed.

Command samples:

/unit_tests/memtool 0x20c8120 1 //Read register data /unit_tests/memtool 0x20c8120=0x00011771 //write LDO_USB 3.2 V /unit_tests/memtool 0x20c8120=0x00010F71 // write LDO_USB 3.0 V /unit_tests/memtool 0x20c8120=0x00010071 // write LDO_USB 2.65 V



Table 44. USBPHYx_TXn Register Settings

Name	PMU_RI	EG_3P0														
Description	This regi	ister defin	es the cor	ntrol and s	tatus bits f	for the 3.0	V regula	tor powere	d by the h	iost USB '	VBUS pin	s.				
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserve	d													OK_ VDD3 P0	BO_ VDD3 P0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	1	1	1	1	0	1	1	1	0	1	1	0
Field definitions	Reserve	d		OUTPU	T_TRG				REG_ 3P0_ VBUS_ SEL	BO_OFF	SET		Reserved	IENABLE ILIMIT	ENABLE BO	ENA BLE_ LIN REG
Signal Names	Descript	ion														
OUTPUT_TRG	Control I 0x1F - 3 0x0F - 3 0x00 - 2 The chip	bits to adju .4 V .0 V .625 V o functiona	ust the reg ality may b	gulator out	put voltag	e in 25 m ^V aranteed	/ steps. near the e	extremes c	of the prog	ramming	range.					
ENABLE_LIN REG	Control I	bit to enab	le the reg	ulator out	put											

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8.1.3 USBC_n_PORTSC1

Port control is used for status port reset, suspend, and current connect status. It is also used to initiate test mode or force signaling and allows software to put the PHY into low power suspend mode and disable the PHY clock.

0x2184184 1 //OTG Port Read register data
0x2184184=0x18441205 //OTG Port Test packet
0x2184184=0x18411205 //OTG Port J STATE
0x2184184=0x18421205 //OTG Port K STATE
0x2184184=0x18431205 //OTG Port SEO (host) /
0x2184184=0x18401305 //OTG Port Reset
0x2184184=0x18401285 //OTG Port Suspend
0x2184184=0x18401245 //OTG Port Resume
0x2184384 1 //Host Port Read register data
0x2184384=0x18441205 //Host Port Test packet
0x2184384=0x18411205 //Host Port J STATE
0x2184384=0x18421205 //Host Port K STATE
0x2184384=0x18431205 //Host Port SEO (host) /
0x2184384=0x18401305 //Host Port Reset
0x2184384=0x18401285 //Host Port Suspend
0x2184384=0x18401245 //Host Port Resume

Table 45.	USBC_n	PORTSC1	Register	Settings

Name	USBC_	n_PORTS	C1													
Description	This reg It is als	gister defin o used to ir	es the cont nitiate test r	rol and stat mode or for	tus bits for ce signalin	the 3.0 V re g and allow	egulator po /s software	wered by t to put the	he host US PHY into lo	B VBUS pir w power su	n. Jspend moe	de and disa	ble the PH	Y clock.		
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1		STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	PTC			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PIC		PO	PP	LS		HSP	PR	SUSP	FPR	000	OCA	PEC	PE	CSC	CCS
Field	Descri	ption														
	Refer to FORCE ENABL the por NOTE: Any oth Value S 0000 T 0010 K 0011 S 0100 P 0101 F 0110 F 0111 F 0111 F 0100-1	D Port Test <u>E</u> NABLE <u>E</u> (HS/FS) t state mac Low-speec ter value th Specific Tes EST_MOD <u>S</u> TATE <u>S</u> STATE E0 (host) / acket ORCE_EN ORCE_EN DRCE_EN DRCE_EN	Mode for th FS and Fr LS} values hines to priving an zero inc t: E_DISABL NAK (device ABLE_HS ABLE_FS ABLE_LS ed	ne operatio ORCE ENA force the p ogress norms s are not su dicates that E	nal model f BLE_LS a port into the maily from i upported as the port is	or using the re extension connected that point. a a peripher operating i	ese test mo ins to the te I and enabl ral device. n test mode	odes and th est mode su ed state at	e USB Spe pport spec the selecte	ecification F	Revision 2.C), Chapter 7 ification. W PTC field ba	' for details riting the P lock to TEST	on each te TC field to f [_MODE_C	st mode. Ti any of the F JISABLE wi	he ORCE_ II allow
PR	Port Re In Host When s the rese the driv	eset - Read Mode: Rea software wr et sequenc er. In Devie	/Write or R ad/Write. 1= ites a one t e is comple ce Mode: T	ead Only. E =Port is in F to this bit th ete. This be his bit is a	Default = 0b Reset. 0=Po le bus-rese havior is di read-only s	o. ort is not in t sequence fferent from tatus bit. D	Reset. Det as defined EHCI whe evice reset	fault 0. I in the USI ere the hos from the L	B Specifica t controller JSB bus is a	tion Revisio driver is re also indicat	on 2.0 is sta quired to se ed in the U	arted. This b at this bit to SBSTS reg	bit will autor a zero afte ister.	matically ch r the reset	nange to ze duration is t	ro after timed in
SUSP	Susper	nd - Read/V	Vrite or Rea	ad Only. De	efault = 0b.											
AN12409					All	information p	provided in thi	s document i	is subject to le	egal disclaime	ers.			© 2023 N	XP B.V. All rig	hts reserved.
									0000							

Name	USBC_n_PORTSC1
	1=Port in suspend state. 0=Port not in suspend state.
	In Host Mode: Read/Write.
	Port Enabled Bit and Suspend bit of this register define the port states as follows:
	Bits [Port Enabled, Suspend] Port State
	0x Disable
	10 Enable
	11 Suspend
	When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the host controller will unconditionally set this bit to zero. The host controller ignores a write of zero to this bit. If host software sets this bit to a one when the port is not enabled (that is, Port enabled bit is a zero) the results are undefined.
FPR	Force Port Resume -Read/Write. 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. Default = 0.
	Software sets this bit to one to drive resume signaling. The Host Controller sets this bit to one if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J to K transition is detected, the Port Change Detect bit in the USBSTS register is also set to one. This bit will automatically change to zero after the resume sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the resume duration is timed in the driver. In Device mode:
	After the device has been in Suspend State for 5 ms or more, software must set this bit to one to drive resume signaling before clearing. The Device Controller sets this bit to one if a J-to-K transition is detected while the port is in the Suspend state. The bit is cleared when the device returns to normal operation. Also, when this bit is cleared because a K-to-J transition detected, the Port Change Detect bit in the USBSTS register is also set to one.

Table 45. USBC_n_PORTSC1 Register Settings...continued

8.1.4 Other useful commands and scripts

Command samples:

```
# Let the system enter suspend (standby) mode
echo mem > /sys/power/state
#Set Console as the system wakeup source
echo enabled > /sys/class/tty/ttymxc0/power/wakeup
#USB remote wakeup (as system wakeup source) is not enabled by default, user can
enable this feature by using this script, after plugging in the USB device
for i in $(find /sys -name wakeup | grep usb);do echo enabled > $i;echo "echo
enabled > $i";done;
```

8.2 i.MX 7ULP USB PHY registers and software configurations

The test board has routed out two USB Ports: one Type-C, one Debug. Only the Type-C port has several registers to adjust the signal voltage level, slow rate.

8.2.1 USBPHY_TXn

The USB PHY Transmitter Control Register handles the transmit controls. Bit fields TXCAL45DP, TXCAL45DM, D_CAL are usually to adjust the output voltage amplitude.

Command samples:

```
/unit_tests/memtool 0x40350010 1 // Read register data
/unit_tests/memtool 0x 40350010=0x1c060607 //write USBPHY_TX
```

Table fer eest fink_introgreter eettinge
--

Name	USBPH	Yx_TXn														
Description	The USE	3 PHY Trar	smitter Cor	ntrol Regist	er handles	the transm	it controls.									
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
Field definitions	Reserved			Reserved			Reserved	Reserved Reserved			TXEN CAL 45DP	Reserved	d TXCAL45DP			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	USBPH	Yx_TXn														
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	Reserve	d	TXEN CAL 45DN	Reserved	TXCAL45	DM			Reserved				D_CAL			
Signal Names	Descrip	tion														
TXCAL45 DP	Decode Trimmin	to trim the g this resist	nominal 45 tance impa	Ω series te cts both the	rmination r overshoot	esistance /undershoo	to the USB ot of the Fu	_DP output II Speed TX	: pin. Maxin K output an	num resista d the ampli	ance = 0000 tude of the). Resistan High-Spee	ce is cente ed TX outpu	red by desig it.	gn at 1000.	
TXCAL45 DM	Decode Trimmin	to trim the g this resist	nominal 45 tance impa	Ω series te cts both the	rmination r overshoot	esistance /undershoo	to the USB ot of the Fu	_DM outpu II Speed TX	t pin. Maxir K output an	numresista d the ampl	nce = 0000 tude of the). Resistan High-Spee	ce is cente ed TX outpu	red by desiç ıt.	gn at 1000.	
D_CAL	Decode High-Sp 0000 Ma 0111 No 1111 Mir	to trim the eed TX eye aximum cur minal nimum curre	nominal 17 e diagram. rent, appro ent, approx	.78 mA cur ximately 19 imately 19	rent source % above r % below no	for the Hig nominal.	gh-Speed T	X drivers c	n USB_DP	e andUSB_	DM. This c	urrent is dir	ectly propo	rtional to th	e amplitud	e of the

Table 46. USBPHYx_TXn Register Settings ...continued

8.2.2 Other useful commands and scripts

Command samples:

```
# Let the system enter suspend (standby) mode
echo mem > /sys/power/state
#Set Console as the system wakeup source
echo enabled > /sys/class/tty/ttymxc0/power/wakeup
#USB remote wakeup (as system wakeup source) is not enabled by default, user can
enable this feature by using this script, after plugging in the USB device
for i in $(find /sys -name wakeup | grep usb);do echo enabled > $i;echo "echo
enabled > $i";done;
```

8.3 i.MX 8QXP/8QM USB PHY registers and software configurations

The test board has routed out two USB Ports: one Type-C, one Micro-AB.

8.3.1 Operation steps

8.3.1.1 Type C host mode

- 1. Power up board
- 2. At uboot console (When displaying 3, 2, 1, press the enter key to enter the uboot mode), input as shown in Figure 142.

```
>setenv fdt_file fsl-imx8qxp-mek-host.dtb
```

```
Note: fsl-imx8qxp-mek-host.dtb
```

For DRP application, the test fixture works abnormal if we configure controller as dual-role. So, the user must use host-only mode to pass signal test. Below are change for dts:

```
diff--git a/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
b/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
index d340e7065f6d..049c161d8974 100755
--- a/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
+++ b/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
@@ -909,7 +909,7 @@
};
& usbotg3 {
- dr_mode = "otg";
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```

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```
+ dr_mode = "host";
extcon = < & typec_ptn5110>;
status = "okay";
```

};



SCOM48:115200baud - Tera Term VT	-	Ø	\times
Ele Edit Setup Control Window Help			
[0.212453] smp: Brought up 1 node, 4 CPUs			
[0.264427] SMP: Total of 4 processors activated.			
U.2691191 CPU features: detected feature: GIC system register CPU interface			
1 0.2762441 UPU features: detected feature: 32-bit EL0 Support			
1 0.28200641 CPU features: detected feature: Kernel page table isolation (KPII)			
L 0.294201J CPU; HII CPU(S) started at EL2			
L 0.29002J alternatives: patching kernel code			
1 0.3032021 devimpts, initialized			
[0, 32865] ratio $[0, 2865]$ ratio $[0, 2865]$ and $[0, 2865]$ rate $[0, 32865]$ ratio $[0, 2865]$ ratio $[0, 2865]$ rate			
(0.32000) futay hash table entries: (0.171) (order 5 131072 hutes)			
9.3669071 pinctrl core: initialized pinctrl subsystem			
[0.374077] DMI not present or invalid.			
[0.377994] NET: Registered protocol family 16			
[0.384814] cpuidle: using governor menu			
[0.389864] vdso: 2 pages (1 code @ ffff000008da6000, 1 data @ ffff0000094c5000)			
[0.396958] hw-breakpoint: found 6 breakpoint and 4 watchpoint registers.			
U.4095461 DMH: preallocated 256 KiB pool for atomic allocations			
U 9,4162481 Serial: HMBH PLUII UHRT driver			
1 0.42/2043J MU and Power domains initialized			
U 4205005 ***** IMX60XP_CIOCKS_INIT *****			
1 0.490304 Improved the shallow of the second s			
0.5200411 MXS_phy objected 2.050000.050000.0500000.050000 suppry phy ope for round, using dummy regulator			
A 5868131 ACPT. Interneter disabled			
0.5979491 mxs-dma 5b810000.dma-apbh: initialized			
[0.606831] ygaarb: loaded			
[0.609496] SČSI subsystem initialized			
[0.613440] usbcore: registered new interface driver usbfs			
[0.618669] usbcore: registered new interface driver hub			
[0.623970] usbcore: registered new device driver usb			
NAP 1.MX Release Distro 4.14-sumo imxödxpmek ttyLP0			
inv&gypmek login: root			
TurkoqApmek 10911. Foot			_
Figure 143, Root			
boots up and log in (When the board boots up, type root, as shown in <u>Figure 143</u>): root			

4. then, input below commands:

Note: write the command and then connect the test fixture.

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on
> $i";done;
```

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#For usb3.0 enter compliance mode/loopback mode.
/unit tests/memtool 0x5b130490=0x0a000340

Note: echo -1 > /sys/module/usbcore/parameters/autosuspend Disable USB bus enters suspend state Note: For i in \$(find /sys -name control | grep usb);do echo on > \$i;echo "echo on > \$i";done; Disable USB runtime suspend, in that case, the controller, and PHY will not enter low-power mode, and we can visit the register even there is no device on the port. Note: (/unit_tests/memtool 0x5b130490=0x0a000340) Set Link is in the Compliance Mode State Search PORTSC1USB3. Refer to Adjust USB3.0 to compliance mode registers--PORTSC1USB3_(offset: 1_0490h)

8.3.1.2 Type C device mode

- 1. Power up board,
- 2. Boots up and login (When the board boots up, type root, as shown in Figure 4): root
- 3. Input below commands:

```
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on >
$i";done;
./configfs.sh
```

Note: (./configfs.sh)

Refer to <u>Software Configuration</u> to complete .configfs.sh.

8.3.1.3 Micro-AB host mode

- 1. Power up board,
- 2. Boots up and login: root

8.3.1.4 Micro-AB device mode

- 1. power up board,
- 2. boots up and login: root
- 3. then, input below commands:

./configfs.sh "" ci

8.3.2 Update image

8.3.2.1 Download the uuu tool and software

Download the uuu tool from https://github.com/NXPmicro/mfgtools/releases

You can find the released SW on the Official website.

For example,(8QM Linux)

From the official website <u>https://www.nxp.com/</u>, choose your selected product, then select "Software & tools", find the Linux version for the board, select" Embedded Linux for i.MX Applications Processors", and you can find the SW for your board.

The final link for 8QM Linux is <u>https://www.nxp.com/webapp/sps/download/preDownload.jsp</u>, you can find what you want here.

8.3.2.2 Burn release image into SD card

- 1. Dial code switch to Serial download mode, plug in Type C wire and serial port wire, open serial port.
- 2. Copy the two files: .sdcard and .bin file to mfgtools\uuu\Windows:

////uuu user guide in command

	∠ » migt	ools > uuu > Willdows				v 0	技糸 VVIII
	^	名称	修改日期	类型	大小		
☆ 快速访问		imx-boot-imx8gmmek-sd.bin-flash b	0 2018/11/5 14:09	BIN-FLASH B0 文件	946 KB		
	*	S libusb-1.0.dll	2018/10/17 14:17	应用程序扩展	154 KB		
▶ 下载	*	test-internal-qt5-imx8qmmek.sdcard	2018/11/5 15:06	SDCARD 文件	5,931,008 KB		
▶ 图片	*	🔳 uuu.exe	2018/10/17 14:17	应用程序	281 KB		
📒 8mmini							
📕 USB							
📒 报价8QM							
🔜 桌面							
🌮 OneDrive - NXP							
NXL53277							
🔳 视频							
🔚 图片							
📔 文档							
🜗 下载							
🜗 音乐							
声 桌面							
📣 OSDisk (C:)							
👽 nxf47730 (\\wbi.nxp.c	om\L 🗸						
4 个项目 已洗择 2 个项目	5.65 GB						1
	Suido						

uuu -b sd all imx-boot-imx8qxpmek-sd.bin test-internal-qt5-imx8qxpmek.sdcard

4. Wait for the downloading over.

tool at)

uuu

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C	🖪 选择命令提示符 - u	uu -b emmc_all imx-boot-imx8qmmek-sd.bin-flash_b0 fsl-image-validation-imx-imx8qmmek.sdcard	_	đ	×
M (icrosoft Windo c) 2017 Micros	ws [版本 10.0.15063] oft Corporation。保留所有权利。			^
Н	:\Xc:				
С	:\>pd C:\Users	\nxf47730\Desktop\EMMC\mfgtools\uuu\Windows			
C u	:\Users\nxf477 uu (Universal	30\Desktop\EMMC\mfgtools\uuu\Windows\ <mark>uuu</mark> Update Utility) for nxp imx chips — libuuu_1.1.81-0-ge39adc4			
u		$V] \leq bootloader cmdlists cmd >$			
	bootloader cmdlist -d -v -V -m	download bootloader to board by usb run all commands in cmdlist file If it is path, search uuu.auto in dir If it is zip, search uuu.auto in zip Run one command, use -H see detail example: SDPS: boot -f flash.bin Deamon mode, wait for forever. verbose mode, -V enable libusb error\warning info USBPATH Only monitor these pathes. -m 1:2 -m 1:3			
u		Enter shell mode. uuu.inputlog record all input commands you can use "uuu uuu.inputlog" next time to run all commands			
u		show help, -H means detail helps			
u	uu [-d -m -v] Run Bui emmc emmc_al qspi sd sd_all	-b[run] <emmc_emmc_all qspi sd sd_all spl> arg lt-in scripts burn boot loader to eMMC boot partition arg0: _flash.bin arg0: _flash.bin arg1: _rootfs.sdcard burn boot loader to qspi nor flash arg1: _flexspi.bin bootloader arg1: _flexspi.bin bootloader burn boot loader to sd card arg0: _flesh.bin burn boot loader to sd card arg0: _flash.bin burn whole image to sd card</emmc_emmc_all qspi sd sd_all spl>			~
	Figure 14	5. UUU Guide			

8.3.3 Software configuration

1. After the board boots up, input the following commands:

```
nano configfs.sh
Example configfs.sh
if [ "$1" == "" ]; then
export FUNC="mass_storage"
else
export FUNC=$1
fi
#38100000.dwc3 for imx850D Synopsys USB3 IP
#gadget-cdns3 for imx8qm and imx8qxp Cadence USB3 IP
#ci hdrc.0 for Legacy NXP USB2 IP
if [ "$2" == "" ]; then
export CONTROLLER="gadget-cdns3"
else
export CONTROLLER="ci hdrc.0"
fi
if ! mount|grep -sq '/sys/kernel/config'; then
mount -t configfs none /sys/kernel/config
fi
cd /sys/kernel/config/usb gadget
mkdir g1
cd gl
echo "0x1fc9" > idVendor
echo "0x0200" > idProduct
mkdir strings/0x409
echo "12345678ABCD" > strings/0x409/serialnumber
echo "NXP Semiconductors" > strings/0x409/manufacturer
echo "i.MX Reference Board" > strings/0x409/product
```

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```
mkdir configs/c.1
mkdir functions/$FUNC".0"
ln -s functions/$FUNC".0" configs/c.1
if [ "$FUNC" == "mass_storage" ]; then
echo "/home/root/storage.img" > functions/mass_storage.0/lun.0/file
echo 1 > functions/mass_storage.0/lun.0/removable
echo 0xc0 > configs/c.1/bmAttributes
fi
if [ "$FUNC" == "ncm" ]; then
echo 10 > functions/ncm.0/qmult
fi
echo $CONTROLLER > /sys/kernel/config/usb gadget/g1/UDC
```

2. Quit and save when finish typing. Input:

```
chmod +x configfs.sh
dd if=/dev/zero of=/home/root/storage.img bs=1M count=256
mkfs.vfat /home/root/storage.img
reboot
```

8.3.4 8QXP/8QM register

```
Type-C port base address: USB3_PHY3P0 (5B16_0000)
USB3 (5B12_0000)
USB2PHY(5B19_8000)
Micro-AB port base address: USBOH_OTG(5B0D_0000)
Register address: base address+offset
```

8.3.4.1 Register to adjust the Type-C eye pattern--AFE_TX_REG1

Offset: 04h

```
#Read register data
/unit_tests/memtool 0x5b198004 1
# Write AFE_TX_REG1 register data
/unit_tests/memtool 0x5b198004=0x3f
```

Table 47. HS TX Amplitude Tune bits control Register

Register Name	Register Address (offset)	Register Bit	Description FastChar	Value
AFE_TX_REG1	0x 0004	<7:6>	UNUSED	00
		<5>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<4>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<3>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<2>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<1>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<0>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0

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Register Name	Register Address (offset)	Register Bit	Description FastChar	Value
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
AFE_TX_REG12	0x 0030	<7:2>	UNUSED	000000
		<1>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<0>	HSTX DEEMP AMPLITUDE CANNOT BE CONTROLLED BY ANALOG TEST BITS IN AFE_TX_REG1	0
			HSTX DEEMP AMPLITUDE CAN BE CONTROLLED BY ANALOG TEST BITS IN AFE_TX_REG1	1

Table 47. HS TX Amplitude Tune bits control Register...continued

Table 48. HS TX Slew Rate control Register

Register Name	Register Address	Register Bit	Description FastChar	Value	
AFE_TX_REG5	0x00 14	<7>	Reserved	0	
AFE_TX_REG5	0x00 14	<6:1>	HSTX Slew Rate control code	<000000> to <111111> 64 steps	
AFE_TX_REG5	0x00 14	<0>	HSTX Slew control set to default code<111000>	0	
			HSTX Slew control Set by control code AFE_TX_REG<6:1> value	1	

For USBOTG2 (type C port) of imx8QXP/IMX8QM, the default disconnection threshold is 575 mv when $AFE_RX_REG0[7:6] == 0$. For customers who are using a cable or daughter card on this USB port, it is recommended to increase 35 mv by setting AFE_RX_REG0[7:6] to 2'b10 or 2'b01.

Table 49. Adjust the trip point for the disconnect detector

Register Name	Register Address	Register Bit	Description	Value
AFE_RX_REG0	X_REG0 0x5B198034 [7:6] By default, the threshold is 575 mv		By default, the threshold is 575 mv	00
			Increase threshold by ~35 mv	01.10
			Increase threshold by ~70 mv	11

8.3.4.2 Register to adjust micro-AB eye pattern --USBPHY_TX /USBPHY_RX

#Offset:10h	
/unit tests/memtool	0x5b0d0010 1
#Write USBPHY TX	
/unit tests/memtool	0x5b0d0010=0x10080803

Table 50. USBPHYx_TXn Register Settings

Name	USBPHY	x_TXn		-	-											
Description	The USB	PHY Trans	smitter Con	trol Registe	er handles	the transmi	t controls.									
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
Field definitions	Reserved			Reserved			Reserved	Reserved	Reserved		TXEN CAL 45DP	Reserved	TXCAL45	DP		
											4301					
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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USBPHYx_TXn Name Field Reserved TXEN Reserved TXCAL45DM Reserved D_CAL definitions CAL 45DN Signal Names Description TXCAL45 Decode to trim the nominal 45 Ω series termination resistance to the USB_DP output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. DP Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output. TXCAL45 DM Decode to trim the nominal 45 Ω series termination resistance to the USB_DM output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output. D_CAL Decode to trim the nominal 17.78 mA current source for the High-Speed TX drivers on USB_DP and USB_DM. This current is directly proportional to the amplitude of the High-Speed TX eye diagram. 0000 Maximum current, approximately 19 % above nominal. 0111 Nominal 1111 Minimum current, approximately 19 % below nominal.

Table 50. USBPHYx_TXn Register Settings...continued

Table 51. Table3-1. USBPHYx_RXn Register Setting

Name									USBPH	IYx_RXn									
Description	The U	SB PHY F	Receiver C	Control Re	gister han	dles the re	eceive cor	ntrols.											
Bit #	31	30	29	28	27	26	25	24	23		22	21	20	19		18	17	16	
Reset value	0	0	0	0	0	0	0	0	0		0	0	0	0		0	0	0	
Field definitions	Reser	ved									RX_RXD Reserved BYPASS								
Bit #	15 14 13 12 11 10 9 8 7									6	5	4	3		2	1	0		
Reset value	0	0	0	0	0	0	0	0	0		0	0	0	0		0	0	0	
Field definitions	Reser	ved								RX_DISC	ISCONADJ reserved RX_ENVADJ								
Signal Names	Descri	ption																	
RX_DIS							/	Adjust thre	shold of c	lisconnect	ion detec	tor							
CONADJ								000 = Ti	ip-Level V	/oltage is (0.57500 V	,							
								001 = 10 $010 = T_1$	ip-Level v	oltage is (J.55000 V 1 58750 V	,							
								011 = Ti	ip-Level V	oltage is (0.007 00 V	,							
								5 1	1XX = F	Reserved									

Note: The default value is "000", "011" is recommended to get the maximum margin for the disconnection detection for customer with a long cable on USB controller.

8.3.4.3 Registers that entry into USB2.0 test mode for MicroAB --USB_x_PORTSC1

#Offset:184h				
memtool 0x5b0d0184 1				
# Force to output Test Packet	for	Eye Dia	gram	Test
memtool 0x5b0d0184=0x18441205				
#Force to output J STATE				
memtool 0x5b0d0184=0x18411205				
#Force to output K STATE				
memtool 0x5b0d0184=0x18421205				
#Force to output SE0 (host) /	NAK	(device)	
memtool 0x5b0d0184=0x18431205				
# Force to output Reset				
memtool 0x5b0d0184=0x18001305				
#Force to output Suspend				
memtool 0x5b0d0184=0x18001285				
#Force to output Resume				
memtool 0x5b0d0184=0x18001245				

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Name									PORTSC	1							
Description	Device C	Controller															
Bit #	31	30	29	28	27	26	25	24	23	22	21		20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
Field definitions	PTS_1		STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKDC		PTC		-	
Bit #	15	14	13	12	11	10	9	8	7	6	5	5		3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0		0	0	1	1	1
Field definitions	PIC		PO	PP	LS	·	HSP	PR	SUSP	FPR		000	OCA	PEC	PE	CSC	ccs
Signal Names									Descriptio	on							
PTC	Refer to Revision The FOF the EHC the port TEST_M NOTE: L Any othe Value Sp 0000 TE 0010 K_ 0010 SE 0100 Pa 0101 FC 0110 FO 0111 FO 0100-111	Port Test a 2.0, Cha RCE_ENA l specific: into the ci loope_Dis ow speed er value th becific Tes ST_MOD STATE STATE 0 (host) / cket PRCE_EN RCE_EN RCE_EN 11 Reserv	Mode for pter 7 for vBLE_FS vation. Writ connected SABLE wit d operation an zero in st E_DISAB NAK (dev vABLE_HS ABLE_FS ABLE_LS red	ite Default the operation details on and FORC ing the PT and enable II allow the ns are not indicates the LE	in a post of the second	el for usin mode. E_LS are any of the the select machine as a peri t is operat	g these test extensions FORCE_E ted speed. s to progre pheral dev ing in test i	st modes a s to the te:: NABLE_{ Writing th writing the ss normal ice. mode.	and the US st mode su HS/FS/LS he PTC fiel ly from the	B Specifi pport spe } values w Id back to it point.	cation cified in ill force						

Table 52. USB_PORTSC1 field descriptions

8.3.4.4 Registers that entry into USB2.0 test mode for TypeC

At uboot console:

```
setenv fdt_file fsl-imx8qxp-mek-host.dtb
boot
```

In kenel:

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on >
$i";done;
```

Note: For detailed settings, refer to Operation Steps

```
#USB3:5B12_0000h
#PORTSC1USB2:1_0480h
/unit_tests/memtool 0x5b130480 1
/unit_tests/memtool 0x5b130480=0xa0
#PORTSC1USB3:1_0490h
/unit_tests/memtool 0x5b130490=0xa0
#USBCMD:1_0080h
/unit_tests/memtool 0x5b130080=0x804
#PORTPMSC1USB2:1_0484h
# enable Test mode
/unit tests/memtool 0x5b130484=0x8000000
```

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<pre># Test Packet/ Test</pre>	J/ Test K Mode/Test Nek Mode
/unit tests/memtool	0x5b130484=0x40000000
/unit_tests/memtool	0x5b130484=0x10000000
/unit_tests/memtool	0x5b130484=0x20000000
/unit_tests/memtool	0x5b130484=0x30000000

Table 53. PORTSC1USB2/ PORTSC1USB3 field descriptions

Name	PORTS	C1USB2/ I	PORTSC1U	SB3												
Description	USB2/3	Port Statu	s and Contr	ol												
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	WPR	DR	Reserved	Reserved	WOE	WOE	WOE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC PortSpeed						PP	PLS				PR	OCA	Reserved	PED	CCS
Signal Names	Descrip	otion														
9 PP	Port Po switchin attaches read PF Powere switche	² ² ³ ² ³ ² ³ ² ³ ² ³ ² ⁴ ² ⁵ ² ⁴ ² ⁴ ² ⁵ ⁴ ⁴ ⁴ ⁴ ⁴ ⁵ ⁴ ⁴ ⁴ ⁴ ⁴ ⁴ ⁴ ⁴ ⁴ ⁴														

Table 54. USBCMD field descriptions

Name	USBCMD	USBCMD														
Description	USB Com	USB Command														
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved															
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved				EU3S	EWE	CRS	CSC	LHCRST	Reserved	Reserved HSEE INTE HC				HCRST	R_S
Signal Names	Descripti	on														
0 R_S	Run/Stop (R/S), RW. Default = '0'. '1' = Run. '0' = Stop. When set to a '1', the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. Refer to section 5.4.1.1 of xHCI specification for more information on how R/S shall be managed. The xHC shall halt within 16 ms after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (that is, HCH in the USBSTS register is '1). Doing so may yield undefined results. Writing a '0' to this flag when the xHC is in the Running state (that is, HCH = '0') and any Event Rings are in the Event Ring Full state (refer to section 4.9.4 of xHCI specification) may result in lost events. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected V/E. Refer to Section 6.4 VHCI negatification for more information.															

Table 55. USBCMD field descriptions

Name	PORTPM	PORTPMSC1USB2														
Description	USB2 Port Power Management Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTC				Reserved	Reserved									HLE	
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 55. USBCMD field descriptions...continued

Field definitions	L1DS	BESL	RWE	L1S
Signal Names	Description			
9 PP	Port Test Control, RW. Default = '0'. When this field is '0', the port is NOT operating in specific test mode is indicated by the specific value. A non-zero Port Test Control value is not in this state, the xHC shall respond with the Port Test Control field set to Port Test modes. The encodings of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled 1: Test J_STATE 2: Test K_STATE 3: Test SE0_NAK 4: Test Packet 5: Test FORCE_ENABLE 6-14: Reserved. 15: Port Test Control Error.	a test mode. Anon-zero value indicates tha le is only valid to a port that is in the Power st Control Error. Refer to section 4.19.6 for	t it is opera ed-Off state the operat	ating in test mode and the e (PLS = Disabled). If the port ional model for using these test

8.3.4.5 Adjust USB3.0 to compliance mode registers--PORTSC1USB3

#Offset: 1_0490h /unit_tests/memtool 0x5b130490=0x0a000340

Table 56. PORTSC1USB3 field descriptions

Name	PORTSC1USB3															
Description	USB3 Port Status and Control															
Bit #	31 30 29 28 27 26 25 24 23 22 21 20 19									19	18	17	16			
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	WPR	DR	Reserved	Reserved	WOE	WOE	WOE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC PortSpeed						PP	PLS				PR	OCA	Reserved	PED	CCS
Signal Names								Desc	ription							
8-5 PLS	Image: Port Link State (PLS), RWS. Default = RxDetect (5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Values: 0: The link shall transition to a U0 state from any of the U states. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: If the port is in the Disabled state (PLS = Disabled, PP = '1'), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1-2,4,6-15: Ignored. State Encoding: 0: Link is in the U0 state, 1: Link is in the U2 state, 3: Link is in the U3 state (Device Suspended), 4: Link is in the Disabled State, 5: Link is in the RxDetect State, 6: Link is in the Polling State, 8: Link is in the Resume State. Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field. This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete. Refer to section 4.19 of xHCl specification for PLS transition conditions. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field														ed state, port. suspends to resume on to the the U3 s in the e Resume t states more	

8.4 i.MX 8M USB PHY Registers and Software Configurations

8.4.1 Operation steps

8.4.1.1 Type C port

8.4.1.1.1 USB3.0 Host mode

- 1. When the board boots up, press Enter, and then type: root.
- 2. Input below commands:
 - a. RX Test

Connect the test fixture, and then write the command.

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
echo "host" >>/sys/kernel/debug/38100000.dwc3/mode
/unit tests/memtool -32 0x38100430=0x0A010340
```

Note:

- Disable USB bus enters suspend state
- Set Link is in the Compliance Mode State
- Search PORTSC_30 at usb3_block_.guide (https://jira.sw.nxp.com/browse/MXEM-2? filter=27819&jql=project%20%3D%20MXEM) to find the register.
- b. TX Test

Write the command, and then connect the test fixture.

```
echo "host" >> /sys/kernel/debug/38100000.dwc3/mode
/unit tests/memtool -32 0x38200430=0x0A010340
```

8.4.1.1.2 USB3.0 Device mode

- 1. Power up board,
- 2. Boots up and log in: root
- 3. Input below commands:

./configfs.sh

Note: (./configfs.sh)

Refer to Software Configuration to complete .configfs.sh.

8.4.1.1.3 USB2.0 Host mode

1.power up board

2.boots up and log in: root

8.4.1.1.4 USB2.0 Device mode

- 1. power up board,
- 2. boots up and log in: root
- 3. then, input below commands:

./configfs.sh

8.4.1.2 Type A port

8.4.1.2.1 USB3.0 Host mode

- 1. When the board boots up, press Enter, and then type: root.
- 2. Input below commands:
 - a. RX Test

Connect the test fixture, and then write the command.

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
echo "host" >>/sys/kernel/debug/38100000.dwc3/mode
/unit tests/memtool -32 0x38100430=0x0A010340
```

Note:

- Disable USB bus enters suspend state
- Set Link is in the Compliance Mode State
- Search PORTSC_30 at usb3_block_.guide (https://jira.sw.nxp.com/browse/MXEM-2? filter=27819&jql=project%20%3D%20MXEM) to find the register.
- b. TX Test

Write the command, and then connect the test fixture.

```
echo "host" >> /sys/kernel/debug/38100000.dwc3/mode
/unit tests/memtool -32 0x38200430=0x0A010340
```

8.4.1.2.2 USB3.0 Device mode

- 1. Power up board,
- 2. Boots up and log in: root
- 3. Input below commands:

./configfs.sh

Note: (./configfs.sh)

Refer to Software Configuration to complete .configfs.sh.

8.4.1.2.3 USB2.0 Host mode

1.power up board

2.boots up and log in: root

8.4.1.2.4 USB2.0 Device mode

- 1. power up board,
- 2. boots up and log in: root
- 3. then, input below commands:

./configfs.sh

8.4.2 Update image

8.4.2.1 Download the uuu tool and SW

1. Dial code switch to Serial Download mode, plug in Type C wire and serial port wire, open serial port.

2. Copy the two files: .sdcard and .bin file to mfgtools\uuu\Windows:

📕 🛃 📜 🗸 Windows						- 🗆 X
文件 主页 共享	查看					~ 🕐
🗧 🔶 🔶 🕆 📜 > EN	/IMC > mfg	tools > uuu > Windows				♥ ひ 捜索"Win ♪
水 帕达达问	^	名称	修改日期	类型	大小	
→ 大座の円 で → か 地		imx-boot-imx8qmmek-sd.bin-flash_b0	2018/11/5 14:09	BIN-FLASH_B0 文件	946 KB	
	*	libusb-1.0.dll	2018/10/17 14:17	应用程序扩展	154 KB	
▶ ▶ 靫	*	test-internal-qt5-imx8qmmek.sdcard	2018/11/5 15:06	SDCARD 文件	5,931,008 KB	
■ 图片	*	📧 uuu.exe	2018/10/17 14:17	应用程序	281 KB	
📜 8mmini						
📕 USB						
▶ 报价8QM						
■ 桌面						
\land OneDrive - NXP						
🧢 NXL53277						
📓 视频						
▶ 图片						
🗋 文档						
📜 下载						
▶ 音乐						
▶ 桌面						
📣 OSDisk (C:)						
< nxf47730 (\\wbi.nx	p.com\L					
4 个项目 <1 已洗择 2 个项	间 5 65 GB					
Figure 146. UUL	J Guide					
5. Open cmd. inc	out					
<u> </u>						

- c: cd C:\Users\nxf47730\Desktop\EMMC\mfgtools\uuu (The path is where the uuu tool at) uuu ////uuu user guide in command uuu -b sd all imx-boot-imx8qxpmek-sd.bin test-internal-qt5-imx8qxpmek.sdcard
- 4. Wait for the downloading over.

3.

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	🖬 选择命令提示符 - u	uu -b emmc_all imx-boot-imx8qmmek-sd.bin-flash_b0 fsl-image-validation-imx-imx8qmmek.sdcard	_	0)	×
Ν	licrosoft Windo c) 2017 Micros	ws [版本 10.0.15063] oft Corporation。保留所有权利。			^
I	i:\>c:				
0	:\>cd C:\Users	\nxf47730\Desktop\EMMC\mfgtools\uuu\Windows			
0	:\Users\nxf477; uu (Universal)	30\Desktop\EMMC\mfgtools\uuu\Windows\uuu Update Utility) for nxp imx chips libuuu_1.1.81-0-ge39adc4			
l		$^{\circ}$ \rightarrow $^{\circ}$ $^{\circ$			
	bootloader cmdlist cmd -d -v -V -m	download bootloader to board by usb run all commands in cmdlist file If it is path, search uuu.auto in dir If it is zip, search uuu.auto in zip Run one command, use -H see detail example: SDPS: boot -f flash.bin Deamon mode, wait for forever. verbose mode, -V enable libusb error\warning info USBPATH Only monitor these pathes. -m 1:2 -m 1:3			
ι		Enter shell mode. uuu.inputlog record all input commands you can use "uuu uuu.inputlog" next time to run all commands			
l		show help, -H means detail helps			
t	uuu [-d -m -v] · Run Bui emmc emmc_al qspi sd sd_all	-b[run] <emmc_enmc_all qspi sd sd_all spl> arg lt-in scripts burn boot loader to eMMC boot partition arg0: _flash.bin </emmc_enmc_all qspi sd sd_all spl>			v
	Figure 147	7. UUU Guide			

8.4.3 Software configuration

1. After the board boots up, input the following commands:

```
nano configfs.sh
Example: .configfs.sh
if [ "$1" == "" ]; then
export FUNC="mass_storage"
else
export FUNC=$1
fi
#38100000.dwc3 for imx850D Synopsys USB3 IP
#gadget-cdns3 for imx8qm and imx8qxp Cadence USB3 IP
#ci hdrc.0 for Legacy NXP USB2 IP
if [ "$2" == "" ]; then
export CONTROLLER="38100000.dwc3"
else
export CONTROLLER="ci hdrc.0"
fi
if ! mount|grep -sq '/sys/kernel/config'; then
mount -t configfs none /sys/kernel/config
fi
cd /sys/kernel/config/usb gadget
mkdir g1
cd gl
echo "0x1fc9" > idVendor
echo "0x0200" > idProduct
mkdir strings/0x409
echo "12345678ABCD" > strings/0x409/serialnumber
echo "NXP Semiconductors" > strings/0x409/manufacturer
echo "i.MX Reference Board" > strings/0x409/product
mkdir configs/c.1
```

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```
mkdir functions/$FUNC".0"
ln -s functions/$FUNC".0" configs/c.1
if [ "$FUNC" == "mass_storage" ]; then
echo "/home/root/storage.img" > functions/mass_storage.0/lun.0/file
echo 1 > functions/mass storage.0/lun.0/removable
echo 0xc0 > configs/c.17bmAttributes
fi
if [ "$FUNC" == "ncm" ]; then
echo 10 > functions/ncm.0/qmult
fi
echo $CONTROLLER > /sys/kernel/config/usb gadget/g1/UDC
```

```
2. Quit and save when I finish typing. Then to input:
```

```
chmod +x configfs.sh
dd if=/dev/zero of=/home/root/storage.img bs=1M count=256
mkfs.vfat /home/root/storage.img
reboot
```

8.4.4 8M register

Type-C port base address: 3810 0000h

Type-A port base address: 3820 0000h

Register address: base address+offset

8.4.4.1 Registers that entry into USB2.0 test eye diagram mode for Type A -- PORTPMSC 20

```
#offset:420h
# Test Packet/ Test J/ Test K/ Test SE0 NAK Mode
/unit tests/memtool 0x38200424=0x40000000 // Force to output Test Packet for Eye
Diagram Test
/unit tests/memtool 0x38200424=0x10000000 //Force to output J STATE
/unit_tests/memtool 0x38200424=0x20000000 //Force to output K_STATE
/unit_tests/memtool 0x38200424=0x30000000//Force to output SEO (host) / NAK
 (device)
```

Table 57. PO	RTPMSC	_20 field	descriptions
--------------	--------	-----------	--------------

Name	PORTPMSC_20															
Description	USB2 P	ort Power I	Manageme	nt Status a	nd Control											
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	u	u	u	u	0	0	0	0	0	0	0	0	0	0	0	u
Field definitions	PRTTSTCTRL				Reserved	Reserved_27 _17										HLE
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u
Field definitions	L1DSLOT HIRD RWE L1S															
Signal Names								Desc	ription							
PRTTST CTRL	Port Test Control, RW. Default = '0'. When this field is '0', the port is NOT operating in a test mode. Anon-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encodings of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled 1: Test J_STATE 2: Test K_STATE 3: Test SE0_NAK 4: Test Packet													the the port these		
AN12409					All ir	nformation pr	ovided in this	document is	subject to leg	jal disclaime	rs.			© 2023 N	KP B.V. All rig	hts reserved
Annillantia							Dave 4	0 1	- 0000							
Table 57. PORTPMSC_20 field descriptions...continued

Name	PORTPMSC_20
	5: Test FORCE_ENABLE
	6-14: Reserved.
	15: Port Test Control Error.

8.4.4.2 Register to adjust the Type-A eye pattern-- PHY_CTL3_ADDR

Offset: 0x4Ch Base Address for GLUE registers Type-A port base address -382F0000 /unit_tests/memtool 0x382F004C 1 // Read register data /unit_tests/memtool 0x382F004C =94DCE6E4 // Write PHY_CTL3_ADDR register data

Table 58. PHY_CTL3_ADDR register

Name	PHY_CTL3_ADDR															
Description	USB3.0	PHY State	us bits Reg	ister												
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0
Field definitions	tx_vbo	ost_lvl		ios_bias		-	TXREFTU	INE0		_	TXRISET	UNE0	TXRESTI	JNE0	TXP REEM PULSET UNE0	TXP REEM PMPT UNE0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0
Field definitions	TXP REEM PMP TUN E0E0	TXSHXST	UNE0	TXFSLST	UNE0			SQRXTU	NEO		OTGTUN	EO		COMPIDI	STUNE	
Parameter Controls	TXPRE Function defined TXPRE current TXRES Function officers • 11: So • 11: So • 01: Do • 00: So Note: A specific TXRISI Function change	EMPULSE in terms of EMPAMPT duration if STUNEO : U on: Some a source imper- source impe-	TUNE0: Hina controls f unit armou UNE<#>[1] TXPREEM SB Source oplications edance is de dance is de dance is de dance is into bother than t . If this bus IS Transmit the rise/fall a -4 % incr	S Transmitt the duratic nts. One ur] or TXPRE Impedance require add ompensate creased by creased by creased by the default of is not used: ther Rise/Fa times of th emental ch	er Pre-Emj in for which int of pre-er- EMPAMPT JNE<#> is Adjustmen itional devi for added approxima approxima approxima approxima () lave it a II Time Adj e high-spec ange in the	shasis Dura t the HS primphasis dura UNE<#>[0] not used, s it ces to be a series resisis tely 4 Ω . ately 2 Ω . tely 1.5 Ω . in source int t the defaul ustment de dwaveform. HS rise/fa	ation Contre e-emphasis ration is ap] is set to 1 et it to 1'b0 dded on th stance on th stance on th stance v. t setting. m. To enabl II time. A ne	ol c current is : proximately b1. • 1: 1X e USB, suc ne USB. ariation acr e tuning at egative bina	sourced on 580 ps an short pre- h as a serie oss process the board I rry bit settin	to DP<#> o d is defined emphasis o es switch, v s, voltage, evel, conne ig change i	or DM<#>. d as 1X pre- surrent dura which can a and tempe ect this bit t results in a	The HS Tra- emphasis tion • 0: 22 dd significa rature conc o a registe +4 % incre	ansmitter p duration. 1 ((design d ant series r ditions that r. Note: A p mental cha	re-emphasi 'his signal i efault), long esistance. does not m positive bina inge in the	is duration s valid only g pre-emph This bus ac neet USB 2 ary bit settii HS rise/fall	is if either lasis djusts the .0

8.4.4.3 Registers that entry into USB2.0 test mode for Type C

```
# Test Packet/ Test_J/ Test_K/ Test SE0_NAK Mode
/unit_tests/memtool 0x38100424=0x40000000 // Force to output Test Packet for Eye
Diagram Test
/unit_tests/memtool 0x38100424=0x10000000 //Force to output J_STATE
/unit_tests/memtool 0x38100424=0x20000000 //Force to output K_STATE
/unit_tests/memtool 0x38100424=0x30000000//Force to output SE0 (host) / NAK
(device)
```

Table 59. PORTPMSC_20 field descriptions

Name								PORTP	NSC_20							
Description	USB2 Po	rt Power M	anagemen	t Status an	d Control											
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AN12409					All infor	mation provi	ded in this do	ocument is su	ıbject to lega	l disclaimers.				© 2023 NX	P B.V. All rig	hts reserved.

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Name								PORTP	MSC_20							
Reset value	u	u	u	u	0	0	0	0	0	0	0	0	0	0	0	u
Field definitions	PRTTST	CTRL			Reserved	_27 _17	1	1	I	1	1	1	1	1		HLE
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u
Field definitions	L1DSLO	T							HIRD				RWE	L1S		
Signal Names								Desci	ription							
PRTTST CTRL	Port Tesl specific t port is no these tes 0: Test m 1: Test J 2: Test K 3: Test S 4: Test P 5: Test F 6-14: Re 15: Port	Control, F est mode i ot in this st tode not en _STATE _STATE E0_NAK acket ORCE_EN served. Test Contro	RW. Default is indicated ate, the xH The encodi nabled NABLE ol Error.	: = '0'. Whe by the spe C shall resp ngs of the ⁻	n this field i cific value. cond with th fest Mode b	is '0', the p A non-zen ne Port Tes bits for a U	ort is NOT o Port Test st Control f SB2 protoc	operating i Control va ield set to F col port are	in a test mo ilue is only Port Test C :	ode. Anon- valid to a j ontrol Erro	zero value port that is r. Refer to	indicates t in the Pow section 4.1	hat it is op ered-Off st 9.6 for the	erating in te ate (PLS = operationa	est mode a Disabled). I model for	nd the If the using

Table 59. PORTPMSC_20 field descriptions...continued

8.4.4.4 Register to adjust the Type C eye pattern-- PHY_CTL3_ADDR

```
#Offset: 0x4Ch
#Base Address for GLUE registers Type-C port base address:381F0000
/unit_tests/memtool 0x381F004C 1 // Read register data
/unit_tests/memtool 0x381F004C =94D4E464 //Write PHY_CTL3_ADDR register
data
```

Name								PHY_CTL	.3_ADDR							
Description	USB3.0 P	HY Status	bits Regist	er												
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0
Field definitions	tx_vboost	_lvl		ios_bias			TXREFTU	JNE0			TXRISET	UNE0	TXREST	JNE0	TXP REEM PULSET UNE0	TXP REEM PMPT UNE0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0
Field definitions	TXP REEM PMPT UNE0E0	TXSHXST	UNE0	TXFSLST	UNE0			SQRXTU	NE0		OTGTUN	E0		COMPIDI	STUNE	
Parameter Controls	TXPREEM onto DP< is defined emphasis TXRESTU Function: driver sou • 11: Sour • 11: Sour • 01: Desi • 00: Sour Note: Any specificati TXRISET Function: results in	WPULSET(#* or DM< as 1X pre- current du JNE0: USE Some appl rice impeda ce impeda ce impeda ce impeda default ce impeda setting off ion limits. II UNE0: HS Adjusts the a –4 % incc	JNE0: HS ³ ⇒. The HS emphasis is emphasis aration • 0: 2 Source Im- ications reaching ince to con- nce is decr- nce is decr- nce is increa- this bus is Transmittle rese/fall tir remental ch-	Transmitter Transmitter Transmitted duration. TI 2X (design uppedance A quire additi uppensate for eased by a eased by a e default ca not used, r Rise/Fall mes of the l nange in th	Pre-Emph er pre-emp inis signal is default), loo kdjustment onal device or added se pproximate pproximate pproximate n result in eleave it at t Time Adjus high-speed e HS rise/fr	asis Durati hasis durat s valid only ng pre-emp as to be ad- pries resista ly 4 Ω . ly 1.5 Ω . source imp he default : trenent waveform all time. A r	ion Control ion is defin if either T> shasis curre ded on the ance on the edance var setting. To enable negative bir	Function: 1 ed in terms (PREEMPA ant duration USB, such USB, uSB, itation across tuning at the terms tuning at the terms	This signal of unit am MPTUNE- If TXPREI as a series as process he board le ing change	controls the ounts. One #>[1] or T; EMPPULS s switch, wi , voltage, a vel, connect r results in	e duration f unit of pre KPREEMP ETUNE<# hich can ac nd temper ct this bit to a +4 % inc	or which th -emphasis AMPTUNE is not use Id significa ature condi a register remental c	e HS pre-e duration is <#>[0] is si d, set it to nt series re tions that c	emphasis c approxima at to 1'b1.• 1'b0. I'sistance. T loss not me ositive bina e HS rise/f	urrent is so tely 580 p 1: 1X, sho his bus ad eet USB 2.0 ry bit settin all time.	urced s and rt pre- justs the 0 g change

Table 60. PHY_CTL3_ADDR register

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8.4.4.5 Adjust USB3.0 to compliance mode registers--PORTSC_30

#Offset: 430h
/unit tests/memtool -32 0x38200430=0x0A010340

Table 61.	POR	TSC_3	0 field d	escrip	tions											
Name								POF	RTSC_30							
Description	Port Stat	tus and Co	ntrol Registe	er Bit Defini	itions The	PORTSC	Register									
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	u	u	0	0	u	u	u	0	u	u	u	u	u	u	u	u
Field definitions	WPR	DR	Reserved	Reserved	WOE	WDE	WCE	CAS	CEC	PLC	PRC	occ	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	u	u	u	u	u	u	1	0	1	0	1	0	0	1	u	0
Field definitions	PIC		PortSpeed	Ł			PP	PLS				PR	OCA	Reserved	PED	CCS
Signal Names								Des	scription							
8-5 PLS	Port Link system s Write Va the devic signaling Disconne State (D Recover State. Ne are not r informati	software main software main lues: 0: This ce connector from the p ected state evice Susp y State, 9: obte: The Po- effected un ion on the p	S), RWS. De ay set the line e link shall tr ed to this po port. 5: If the ended), 4: L Link is in the ort Link State titl the transii use of this fie	efault = RxI k U state b ansition to rt. While th port is in th d. 1-2,4,6- ink is in the Hot Rese e Write Stro- cion is com eld	Detect ('5 oy writing a U0 sta e Port Lir he Disabl 15: Ignore e Disable t State, 1 obe (LWS plete. Re	¹). This field. S the from any the State = 0 ed state (P ed. State E d State, 5: 0: Link is in) shall also fer to section	d is used to System soft of the U s J3, the hub LS = Disab ncoding: 0 Link is in the the Comp be set to ' on 4.19 of y	ware may ware may tates. 3: T o does not oled, PP = : Link is in ne RxDete liance Moo 1' to write (HCI spec	anage the p also write t he link shal propagate '1'), then th the U0 Sta ct State, 6: de State, 11 this field. TI ification for	oort and ref this field to Il transition downstrea le link shall te, 1: Link Link is in t Link is in t Link is in his field is PLS transi	lects its cu force a Dis to a U3 sta m-directed I transition is in the U1 he Inactive the Test M undefined i tion conditi	rrent link st abled to Di ate from the traffic to th to a RxDete State, 2: L State, 7: L ode State, f PP = '0'. N ons. Refer	ate. When isconnected 0 U0 state. is port, but ect state an ink is in the ink is in the 12-14: Res Note: Trans to sections	the port is in d state transi This action s the hub shall d the port sh U2 State, 3 Polling State erved, 15: Li titions betwee 4.15.2 and 4	the Enabl tion of the electively I respond all transiti : Link is in e, 8: Link i nk is in th en differen 1.23.5 for	ed state, port. suspends to resume on to the othe U3 s in the e Resume t states more

8.5 i.MX 8MM USB PHY registers and software configurations

The test board has routed out two USB-Type C Ports, The register base address: Base 0x32e40000 + 230h offset, Base 0x32e50000 + 230h offset.

8.5.1 USB OTG PHY configuration register 1(USBNC_n_PHY_CFG1)

Most of these signals are used for parametric tuning of the USB transceiver functions.

Name							ι	JSBNC_n	_PHY_CFG	i1						
Description	The USB	_OTGx_PH	IY_CFG1 r	egister allo	ws control	of selecte	d inputs to tl	he USB O	tg Phy.							
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	1	0	1	0	0	1	1	0	0	1	1
Field definitions	CHRG DET _ Megamix	TXPRE EMPPUL SET UNE0	TXPRE E UNE0	MPAMPT	TXREST	JNE0	TXRISET	UNE0	TXVREF	TUNE0			TXFSLST	TUNE0		
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	1	1	1	0	0	0	1	1	1	0	0	1	0	1	1
Field definitions		TXHSXV	TUNE0	OTGTUN	E0		SQRXTU	NE0		COMPDI	STUNE0		FSEL			COMMON ONN
Signal Names							•	Desc	ription							
25–24	HS Trans	mitter Rise	/Fall Time	Adjustment												
TXRI SET	This bus a	adjusts the	rise/fall tim	ies of the h	igh-speed	transmitte	r waveform.									
UNEO	00 -10 %															
	01 Desigr	n default														
AN12409					All i	nformation p	provided in this	document is	s subject to le	gal disclaime	rs.			© 2023 N	XP B.V. All rig	phts reserved.

Table 62. USBNC_n_PHY_CFG1 field descriptions

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Name	USBNC_n_PHY_CFG1
	10 +15 %
	11 +20 %
23–20	HS DC Voltage Level Adjustment
TXV REFT	This bus adjusts the high-speed transmitter DC level voltage.
UNE0	0000 -6 %
	0001 -4 %
	0010 -2 %
	0011 Design default
	0100 +2 %
	0101 +4 %
	0110 +6 %
	0111 +8 %
	1000 +10 %
	1001 +12 %
	1010 +14 %
	1011 +16 %
	1100 +18 %
	1101 +20 %
	1110 +22 %
	1111 +24 %

Table 62. USBNC_n_PHY_CFG1 field descriptions...continued

8.5.2 Registers that entry into USB2.0 eye diagram test mode for Type C -- USBx_nPORTSC1

Name									USBx_	nPORTS	C1						
Bit #	31	30		29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0		0	1	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1			STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	PTC			
Bit #	15	14		13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PIC			PO	PP	LS		HSP	PR	SUSP	FPR	000	0CA	PEC	PE	CSC	CCS
Signal Name	s								Des	scription							
PTC			Port Test Cor The FORCE_ field to any of PTC field bac NOTE: Low s Value Specific 0000 TEST_1 0001 J_STAT 0010 K_STAT 0011 SE0 (hc 0100 Packet 0101 FORCE 0110 FORCE 1000-1111 Ref	htrol - Rea ENABLE f the FOR k to TES speed ope c Test MODE_D TE TE sst) / NAK E_ENABLE E_ENABLE ESENABLE ESENABLE	Id/Write. D _FS and F CE_ENAE T_MODE_ rations ard ISABLE (device) E_HS E_FS E_FS E_LS	efault = 0 ORCE Ef ILE_(HS/f DISABLE e not supp	000b. NABLE_LS 'S/LS} val will allow ported as a	S are exte ues will fo the port s a peripher	nsions to rce the pc tate mach al device.	the test m ort into the ines to provide the test of te	ode suppr connecte ogress no value tha	ort specifie d and ena rmally fror n zero inc	ed in the E abled state n that poi licates tha	EHCI spece a at the secont. at the port	cification. '	Writing the	PTC ig the mode.

Table 63. USBx_nPORTSC1 field descriptions

8.5.3 Other useful commands and scripts

1. Change u-boot bootargs for USB Certification (optional) We may need to load USB certification dtb

```
setenv fdt_file_usb_certi imx6ul-14x14-evk-usb-certi.dtb
setenv loadfdt_usb_certi 'fatload mmc ${mmcdev}:${mmcpart} ${fdt_addr}
${fdt_file_usb_certi}'
setenv usb_certi_boot 'run mmcargs;run loadimage; run loadfdt_usb_certi;bootz
${loadaddr} -
${fdt_addr};'
setenv bootcmd run usb_certi_boot
save
boot /* boot the board */
```

Note: The above command changes dtb file name for USB certification. To use normal MMC board again, the user may need to run below command at u-boot:

```
setenv mmcboot 'run mmcargs; run loadimage;run loadfdt;bootz ${loadaddr} -
    ${fdt_addr};'
save
run mmcboot
```

2. For peripheral only or otg peripheral certification test

```
dd if=/dev/zero of=/home/root/storage.img bs=1M count=256
mkfs.vfat /home/root/storage.img
/home/root/configfs.sh
```

The user can also add above operation to initialization script:

```
vi /etc/rc.local
add "/home/root/configfs.sh" before "exit 0"
```

3. Other Software Configurations (optional)

Below configurations may be needed during certification test.

a. Enable USB wake-up

USB wake-up (as system wake-up source) is not enabled by default, so after plugging in the USB device, the user must enable USB wake-up using below script.

```
for i in $(find /sys -name wakeup | grep usb);do echo enabled > $i;echo
"echo enabled >
$i";done;
echo enabled > /sys/bus/platform/devices/5b110000.cdns3/power/wakeup
```

b. Let the system enter suspend (standby) mode For standard Linux BSP, the user can use below commands:

echo mem > /sys/power/state

- c. Operations for creating wake-up event Remote wake-up, disconnect and connect event will trigger wake-up event to let the system leave suspend (standby) mode.
 Note: imx850D does not support USB wake-up from system suspend.
- d. Disable runtime power management

```
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo
    on > $i";done;
```

e. Set another wake-up source for suspend mode Below is the example to wake up from console.

echo enabled > /sys/class/tty/ttymxc0/power/wakeup

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```
Or
echo enabled > /sys/class/tty/ttyLP0/power/wakeup
```

8.6 i.MX 8DXL USB PHY registers and software configuration

The test board has routed out two USB ports: two Type C ports named USB-OTG1 and USB-OTG2.

8.6.1 Hardware configuration

As shown in the figure, the power supply of the board is connected, the debug port is connected to the computer with a serial cable, and the serial port is opened (set the serial port baud rate to 115200)



Figure 148. Hardware configuration

8.6.2 Software configuration

There are several steps to follow to adjust the software configuration:

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- 1. Update the image
- 2. Download the uuu tool and software.
 - a. Download the uuu tool from github.
 - b. On the official <u>NXP</u> website, choose the selected product.
 - c. Select "Software and tools" and find the Linux version for the board.
 - d. Select" Embedded Linux for i.MX Applications Processors" and find the SW for your board.
- 3. Burn the release image into the SD card.
 - a. Bootmode switch to Serial download mode.
 - b. Plug in the Type C cable and the serial port cable.
 - c. Open the serial port tool.
 - d. Copy the two files: .rootfs.wic and .bin-flash to the same directory, as shown in the figure below.

II							-	□ × ^ (2)
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Clipboard	Organize	New	0	pen	Select			
← → × ↑ 📕 > EMMC > mfgtor	als > uuu		~ O	2	Search uuu			
Ouick access	Name		Date modified		ype	Size		
Documents +	image_dtb.tar		8/17/2022 2:47 Pf	4 I	AR File	27,620 KB		
Developer	imx-boot-imx8dxlb0-lpddr	4-evk-sd.bin-f	8/17/2022 1:57 Pf	4 I	IN-FLASH_SPL File	3,210 KB		
Downloads x	imx-image-multimedia-im	s8dxlb0-lpddr	8/17/2022 1:58 Pf	/ N	VIC File	2,189,417		
Pictures 🖈	imx-image-multimedia-im	s8dxlb0-lpddr	8/17/2022 1:58 Pf	4 I	Z2 File	298,313 KB		
2022	I UUU CKC		8/17/2022 1:57 Pf	4 N	Application	1,313 KB		
AlRobot								

Figure 149. Copying files to the directory

e. open cmd and input:

```
cd C:\Users\nxfxxxxx\Desktop\EMMC\mfgtools\uuu
uuu
uuu -b sd_all imx-boot-imx8dxlb0-lpddr4-evk-sd.bin-flash_spl imx-image-
multimedia-imx8dxlb0-lpddr4-evk-20220428145028.rootfs.wic
```

- f. After the download is finished, power off the board and set the bootmode into SD card mode.
- 4. Adjusting the software configuration
 - a. Power up the board and log in
 - i. Enter the following command to create the .sh script file:
 - \$ vi configfs.sh
 - ii. Enter the interface as shown in the Figure 150:

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~			
~			
- c	onfigfs1.sh 1/1 100%		

Figure 150. The interface

b. Copy the following script into the sh script: **Note:** The lines preceded by the "#" character are comments and have no effect.

```
#!/bin/sh
dd if=/dev/zero of=/home/root/storage.img bs=1M count=64
mkfs.vfat /home/root//storage.img
if [ "$1" == "" ]; then
export FUNC="mass storage"
else
export FUNC=$1
fi
#38100000.dwc3 for imx850D Synopsys USB3 IP
#5b110000.usb3 for imx8qm and imx8qxp Cadence USB3 IP
#ci hdrc.0 for Legacy NXP USB2 IP
if [ "$2" == "" ]; then
export CONTROLLER="ci hdrc.0"
else
export CONTROLLER="ci hdrc.1"
fi
if ! mount|grep -sq '/sys/kernel/config'; then
mount -t configfs none /sys/kernel/config
fi
cd /sys/kernel/config/usb gadget
mkdir gl
cd gl
echo "0x1fc9" > idVendor
echo "0x0129" > idProduct
```

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```
mkdir strings/0x409
echo "12345678ABCD" > strings/0x409/serialnumber
echo "NXP Semiconductors" > strings/0x409/manufacturer
echo "i.MX Reference Board" > strings/0x409/product
mkdir configs/c.1
mkdir functions/$FUNC".0"
ln -s functions/$FUNC".0" configs/c.1
if [ "$FUNC" == "mass storage" ]; then
echo "/home/root/storage.img" > functions/mass_storage.0/lun.0/file
echo 1 > functions/mass_storage.0/lun.0/removable
echo 0xc0 > configs/c.1/bmAttributes
fi
if [ "$FUNC" == "ncm" ]; then
echo 10 > functions/ncm.0/qmult
fi
echo $CONTROLLER > /sys/kernel/config/usb gadget/g1/UDC
```

- c. To save the script, type :wq after pressing esc.
- d. Enter the following commands in order:

```
$ chmod +x configfs.sh
$ dd if=/dev/zero of=/home/root/storage.img bs=1M count=64
```

```
$ mkfs.vfat /home/root//storage.img
```

e. To check that the process goes properly, enter the command \$:

```
root@imx8dxlb0-lpddr4-evk:~# ls
configfs.sh g_mass_storage.ko g_zero.ko storage.img testusb1.sh
testusb2.sh
```

When configfs.sh and storage.img appear, the configuration is successful.

8.6.3 Operation steps

8.6.3.1 USB OTG1 device mode

- 1. Power up the board.
- 2. Boot up or log in. After the board is booted, enter root, as shown in Figure 151:

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[0K [0K	Started Permit User Sessions.
[0K	
	Started Avahi mDNS/DNS-SD Stack.
0K	Started Getty on tty1.
0K	Started Seco blob process.
[0K]	Started Serial Getty on ttyLP0.
[0K]	Reached target Login Prompts.
	Starting Hostname Service
	Starting WPA supplicant
[0K]	Started WPA supplicant.
0K	Started Kernel Logging Service.
0K	Reached target Multi-User System.
	Starting Update UTMP about System Runlevel Changes
[0K]	Started Hostname Service.
0K	Started Update UTMP about System Runlevel Changes.
-	
NXP 1.M	Release Distro 5.4-zeus umx8dxlb0-lpddr4-evk ttyLP0
أسبده وليرا	0 ladded out login, cost
unxadxtt	o-tpdar4-evk togth: root

Figure 151. entering "root"

3. Enter the following command:

\$./configfs.sh

8.6.3.2 USB OTG2 device mode

- 1. Power up the board.
- 2. Boot up or log in.
- 3. Enter the following command:

\$./configfs.sh `' ci

8.6.3.3 USB OTG1 host mode

- 1. Power up the board.
- 2. Boot up or log in.

8.6.3.4 USB OTG2 host mode

- 1. Power up the board.
- 2. Boot up or log in.

8.6.4 8DXL register

USB2_PHY1 base address: 5B10_0000h USB2_PHY2 base address: 5B11_0000h USB02(USB_OTG1)port base address: 5B0D_0000h USB02(USB_OTG2)port base address: 5B0E_0000h Register address: base address+offset

8.6.4.1 Register to adjust USB 2.0 eye pattern --USBPHY_TX /USBPHY_RX

```
#Offset:10h
$/unit_tests/memtool 0x5b100010 1
#Write_USBPHY_TX
$/unit_tests/memtool 0x5b100010=0x10080802
```

USB2_PHY1 base address: 5B10_0000h

USB2_PHY2 base address: 5B11_0000h

Register address: base address+offset.

Table 64. USBPHYx_TXn register settings

Name	USBPHYx_TXn															
Description	The USB	The USB PHY Transmitter Control Register handles the transmit controls.														
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Field definitions	Reserved			Reserved		Reserved	Reserved	Reserved		TXE NCAL 45DP	Reserved	TXCAL45DP				
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
Field definitions	Reserved TXEN CAL 45DM CAL					Reserved	I			D_CAL						
Signal Names	Descriptio	on														
TXCAL 45DP	Decode to trim the nominal 45 Ω series termination resistance to the USB_DP output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.															
TXCAL 45DM	Decode to trim the nominal 45 Ω series termination resistance to the USB_DM output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.															
D_CAL	Decode to trim the nominal 17.78 mA current source for the High-Speed TX drivers on USB_DP and USB_DM. This current is directly proportional to the amplitude of the High-Speed TX eye diagram. 0000 Maximum current, approximately 19 % above nominal. 0111 Nominal 1111 Minimum current, approximately 19 % below nominal.															

#Offset:20h

USB2_PHY1 base address: 5B10_0000h

USB2 PHY2 base address: 5B11 0000h

Register address: base address+offset

Table 65. USBPHYx_RXn register setting

Name	USBPHY	JSBPHYx_RXn														
Description	The USB	The USB PHY Receiver Control Register handles the receive controls.														
Bit #	31	30	29	28	27	26	25	24	23	22	21 20 19 18 17 16					16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved									RXD BYPASS	Reserved					
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved								DISCONA	DJ		Reserved	ENVAD	J		
Signal Names	Description															
RX_DIS CO NAD J	J The DISCONADJ field adjusts the trip point for the disconnect detector. 000 Trip-Level Voltage is 0.56875 V															

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Table 65.	USBPHYx_RXn register settingcontinued
Name	USBPHYx_RXn
	001 Trip-Level Voltage is 0.55000 V
	010 Trip-Level Voltage is 0.58125 V
	011 Trip-Level Voltage is 0.60000 V
	1XX Reserved

8.6.4.2 Registers that entry into USB2.0 test mode-PORTSC1

#Offset:184h

USB OTG1 port base address: 5B0D 0000h USB OTG2 port base address: 5B0E 0000h Register address: base address+offset

\$/unit tests/memtool 0x5b0d0184 1 #Force to output Test Packet for Eye Diagram Test \$/unit tests/memtool 0x5b0d0184=0x18041205 #Force to output J STATE \$/unit_tests/memtool 0x5b0d0184=0x18011205 #Force to output K STATE \$/unit_tests/memtool 0x5b0d0184=0x18021205 #Force to output SE0 (host) / NAK (device)
\$/unit_tests/memtool 0x5b0d0184=0x18031205

Name	PORTSC1															
Description	Device controller															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1		STS	PTW	TW PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	PTC	PTC		
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PIC		PO	PP	LS		HSP	PR	SUSP	FPR	OCC	OCA	PEC	PE	CSC	CCS
Signal Names	Description															
19– 16 PTC	Port Test Refer to on each specific the sele <i>Note: I</i> Any oth Value S 0000b 7 0001b 2 0010b 4 0010b 5 0100b F 1000b-7	st Contro Port Te test mo ation. W coted spe Low-specific T FEST_M J_STATE &_STATE SE0 (hos Packet 1111b Re	ol - read/o st Mode ide. The riting the sed. Writi <i>ed opera</i> than zer rest ODE_DI: : : : : : : : : : : : : : : : : : :	write. De for the o FORCE PTC fie ing the F tions are o indicat SABLE (device)	fault = 00 perationa ENABLE_ Id to any TC field a not sup, es that th	200b. al model _FS and of the Fo back to <i>ported a</i> ne port is	for using FORCE I DRCE_EN TEST_MC s a perip s operatir	these to ENABLE_ IABLE_ { DE_ DIS <i>heral de</i> n ng in test	est mode LS are e HS/FS/ ABLE all <i>vice</i> .	s and the extension LS } valu ows the	e USB Specificati is to the test mod es forces the por port state machin	on Revis e suppor t into the les to pro	tion 2.0, t specifi connectogress no	Chapter ed in the ted and e ormally fi	7 for det EHCI enabled s rom that	ails state at point.

Table 66. USB_PORTSC1 field descriptions

8.7 Other i.MX 8 Serials USB PHY Registers and Software Configurations

TBD

9 Useful links

- 1. Freescale I.MX6 USB Certification Test Guide and Materials: https://community.freescale.com/docs/DOC-94923
- 2. USB Spec: <u>https://www.usb.org/document-library/electrical-compliance-test-specification-superspeed-usb-10-gbps-</u>rev-10
- 3. OTG and Embedded Host related documents: <u>http://www.usb.org/developers/onthego/</u>
- 4. OTG and Embedded Host Compliance Test Spec: <u>http://www.usb.org/developers/onthego/otgeh_compliance_plan_1_2.pdf</u>
- 5. Full and Low Speed Compliance Test Spec: <u>https://www.usb.org/document-library/usb-20-electrical-test-specification</u>
- 6. USB 2.0 Electrical Test Spec: https://www.usb.org/developers/compliance/USB-IF_USB_2_0_Electrical_Test_Spec081005.pdf
- Gold Tree Test procedure: <u>https://compliance.usb.org/resources/GoldSuite%20Test%20Procedure.pdf</u>
 Test software and tools:
- http://www.usb.org/developers/tools/
- 9. Checklist and TPL: <u>http://www.usb.org/developers/compliance/check_list/</u> <u>http://www.usb.org/developers/compliance/check_list/TPL_form_otgeh2_0_v1.0_-_fill-in.pdf</u> http://www.usb. org/developers/compliance/check_list/TPL_form_otgeh2_0_v1.0_-_fill-in.pdf
- 10. Electrical Test procedure for different Oscilloscopes: http://www.usb.org/developers/compliance/electrical_tests/
- 11. Detailed Electrical Test procedure for Keysight Oscilloscope with N5416A: <u>http://www.keysight.com/upload/cmc_upload/All/N5416A_USB2_Compliance_App_Testing_Notes.pdf</u>
- 12. USB-IF Compliance Updates: http://compliance.usb.org/index.asp?UpdateFile=Electrical&Format=Standardh
- 13. Search the TID for certified products: <u>http://www.usb.org/kcompliance/view</u>
- 14. Company VID List: http://www.usb.org/developers/tools/comp_dump
- USB-PET User Manual: <u>http://www.mqp.com/pdf/manuals/PET%20User%20Manual.pdf</u>
 USB-PET Software:
- http://www.mqp.com/dnld.htmh
- 17. Independent Test Labs http://www.usb.org/developers/compliance/labs/
- i.MX 8 Series Applications Processors Materials: <u>https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-app</u>
- 19. i.MX 7 Series Applications Processors Materials: https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applicationsprocessors/i.mx-7-processors:IMX7-SERIES

20. USB 3.2 Specification http://www.usb.org/developers/docs/

10 Abbreviations

Term	Definition
Client Computer	Controller computer networked to host PC for remote control desktop connection
DUT	Device Under Test
EHCI	Enhanced Host Controller Interface(USB2.0)
xHCI	Extensible Host Controller Interface(USB3.0)
ОНСІ	Open Host Controller Interface
UHCI	universal host controller interface(USB1.1)
Host Computer	Server platform operated by Client PC through remote desktop connection
HSETT	High Speed Electrical Test Tool
LAN	Local Area Network
Legacy-free	Any system that does not have PS/2 and other legacy ports
PCle	Peripheral Component Interconnect Express Bus
PID	Product Identification Number
PS/2 port	A legacy mouse or keyboard port located on some motherboards
UAC	User Account Control
USB	Universal Serial Bus
VID	Vendor Identification Number
TID	Product Test ID assigned by USB-IF after passing the USB Certification Test

11 Note about the source code in the document

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12 Revision history

<u>Table 67</u> provides a revision history for this application note. Note that this revision history table reflects the changes to this template, but it can also be used for your document's revision history.

Rev. Number	Date	Substantive Change
4	08 June 2023	Section 8.3.4.1 is updated
3	03/2023	Section 8.6 is added.
2	01/2019	Section 2.1 is modified to cover more i.MX series. Section 2.2 is modified to support the latest version of I.MX series. Section 2.3 and 2.4 add the corresponding equipment of USB 3.0 Super Speed compliance test. Section 2.8 update to the newest links. Section 3.2 is added to cover the software for i.MX 7/8. Section 3.4 is added to the USB 3.0 Super Speed Transmitter Compliance Test. Section 9 Useful links updated. The serial number of Figures are adjusted. Section 8 The USB PHY Registers and Software Configurations for some I.MX8 series are covered in this revision.
1	02/2017	Modified section 2.1 Modified section 2.2 Modified section 3.1 Section 7 Useful links updated
0	10/2015	Initial release

Table 67. Revision history

i.MX 6/7/8 series USB Certification Guide

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