AN13049

Wi-Fi/Bluetooth/802.15.4 M.2 Key E Pinout Definition

Rev. 4 — 30 May 2023

Application note

Document Information

Information	Content
Keywords	AN13049, Wi-Fi, Bluetooth, 802.15.4, M.2, Pinout, Tri-Radio
Abstract	This document defines M.2 usage for both NXP Wi-Fi/Bluetooth and Tri-Radio M.2 module design.



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1 Introduction

M.2 is a form factor for mobile adapters defined by the PCI-SIG (http://www.pcisig.com). The pinouts for M.2 sockets are defined in the PCI Express M.2 Specification.

M.2 sockets with mechanical Key E are used on platforms based on NXP MPUs and MCUs to support wireless connectivity modules based on NXP Wi-Fi/Bluetooth/802.15.4 radios.

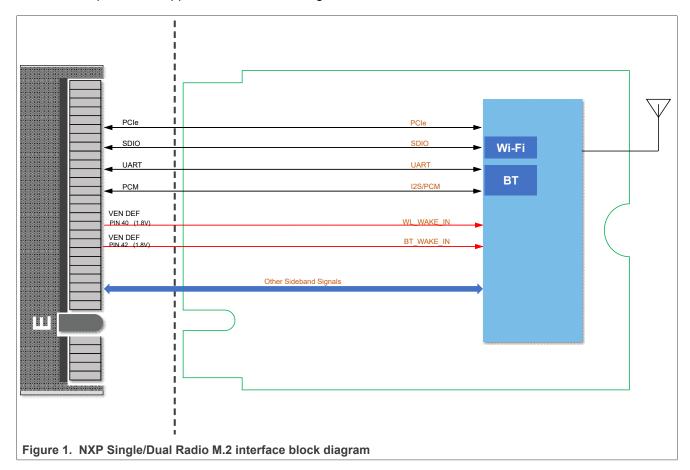
Some of the signals defined in the pinout are used to connect optional sideband and debug signals used by NXP Wi-Fi/Bluetooth/802.15.4 radios.

To ensure proper connection for the sideband and debug signals, this document defines the pin assignments for M.2 sockets (mechanical Key E) on platforms based on NXP MPUs and MCUs.

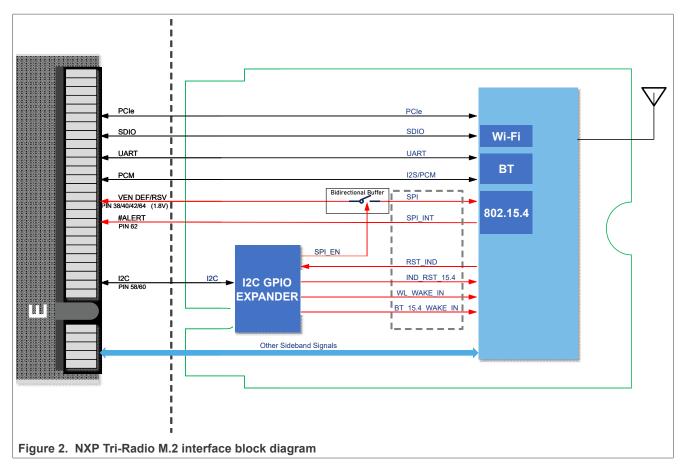
This document defines M.2 usage for both NXP Wi-Fi/Bluetooth and Tri-Radio M.2 module design.

Figure 1 shows NXP Single/Dual Radio M.2 interface block diagram.

<u>Figure 2</u> shows NXP Tri-Radio M.2 interface block diagram. It must add SPI interface for 802.15.4 device, and add an I/O expander to support sideband control signals.



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Before building your board, check the interface connector specification from the wireless module vendor to confirm the pinout used by the module.

For the full definition of the socket pinout, see the *PCI Express M.2 Specification*, available from PCI-SIG website (http://www.pcisig.com).

Note: All the pins that are not listed in this document are recommended to follow the PCI Express M.2 Type E specification or should not be connected.

2 Usage signals for Wi-Fi/Bluetooth and Tri-Radio

This section describes the NXP defined sideband control and SPI signals between the NXP Radio module and MPU/MCU.

Table 1 shows the pin assignments utilized for sideband and SPI signals.

Note: For details on the mandatory and optional lines, see the module data sheet.

Table 1. Sideband and SPI signals

Pin	PCIe M.2 Signal	Type ^[1]	Voltage	Usage for NXP Single/Dual Radio	Usage for NXP Tri-Radi
20	UART_ WAKE#	I		MPU/MCU.	BT_15.4_WAKE_OUT: Bluetooth radio to wake up the MPU/MCU.
					MPU/MCU. Active Low by default.

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Table 1. Sideband and SPI signals...continued

Pin	PCIe M.2 Signal	Type ^[1]	Voltage	Usage for NXP Single/Dual Radio	Usage for NXP Tri-Radi
				Connect to MPU/MCU GPIO opendrain. Pullup required on platform.	Connect to MPU/MCU GPIO opendrain. Pullup required on platform.
21	SDIO_WAKE#	ı	1.8 V	WL_WAKE_OUT: Wi-Fi radio to wake up the MPU/MCU. Active Low by default. Connect to MPU/MCU Open-drain. Pullup required on platform.	Same as single/dual radio.
23	SDIO_ RESET#	0	1.8 V	IND_RST_WL: Independent software reset for Wi- Fi. Active Low by default. Connect to MPU/MCU GPIO.	Same as single/dual radio.
38	VENDOR DEFINED	0	1.8 V	NC	SPI_TXD: SPI transmit signal.
40	VENDOR DEFINED	I/O	1.8 V	WL_WAKE_IN: MPU/MCU to wake up the Wi-Fi radio. Active Low by default. Connect to MPU/MCU GPIO.	SPI_RXD: SPI receive signal.
42	VENDOR DEFINED	0	1.8 V	BT_WAKE_IN: MPU/MCU to wake up the Bluetooth radio. Active Low by default. Connect to MPU/MCU GPIO.	SPI_CLK: SPI clock signal.
44 ^[2]	COEX3	I/O	1.8 V	Talk to NXP support team.	Same as single/dual radio.
46 ^[2]	COEX2	I	1.8 V	Talk to NXP support team.	Same as single/dual radio.
48 ^[2]	COEX1	0	1.8 V	Talk to NXP support team.	Same as single/dual radio.
54	W_ DISABLE2#	0	3.3 V	IND_RST_BT: Independent software reset for Bluetooth. Active Low by default Connect to MPU/MCU GPIO.	Same as single/dual radio.
56	W_ DISABLE1#	0	3.3 V	PDn: Full power down for the Wi-Fi/ Bluetooth radio or controls the PMIC ENABLE signal. High = Normal Low = Full Power-down mode Connect to MPU/MCU GPIO.	PDn: Full power down for the Tri-radio or controls the PMIC ENABLE signal. High = Normal Low = Full Power-down mode Connect to MPU/MCU GPIO.
58	I2C_DATA	I/O	1.8 V	NC	I2C SDA: I2C data for I/O expander. Open-drain. Pullup required on platform. See Table 2.
60	I2C_CLK	0	1.8 V	NC	I2C SCL:

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Table 1. Sideband and SPI signals...continued

Pin	PCIe M.2 Signal	Type ^[1]	Voltage	Usage for NXP Single/Dual Radio	Usage for NXP Tri-Radi
					I2C clock from MPU/MCU for I/O expander. See <u>Table 2</u> .
62	ALERT#	I	1.8 V	NC	SPI_INT: SPI interrupt signal. Open-drain. Pullup required on platform.
64 ^[3]	RESERVED	0	1.8 V	NC	SPI_FRM: SPI frame signal.

- [1] Type refers to the signal direction:
 - Type O means signal is an output from the MPU/MCU to the adapter.
 - Type I means that the signal is an input to the MPU/MCU from the adapter.
- [2] For future use, reserve the sideband signals of coexistence and audio trigger on the M.2 board.
 - To avoid the potential risk on which 1.8 V is designed on other platform, optionally add a serial 100-1K ohm resistor on the path from SPI_FRM to M.2 PIN64.
 - On the Tri-radio M.2 adapter side for the SPI signals, follow the SPI signal definitions based on M.2 Spec Rev 3.0 in the application note document. Do not follow the M.2 Spec Rev 4.0 signal definitions.
 - On the host side, the SPI signal definitions on M.2 connector should be consistent as mention in the application note document. Otherwise, the 802.15.4 transceiver of Tri-radio M.2 adapter cannot work normally. However, this does not impact the Wi-Fi and Bluetooth of the Tri-radio adapter.

2.1 I2C I/O expander for sideband signals

For a Tri-Radio M.2 module, it uses an I2C expander to support sideband control signals. It is important to use an NXP <u>PCAL6408A</u> part. It is an 8-bit general-purpose I/O expander that provides GPIO expansion via the I2C bus interface. See the I/O expander port assignment or the sideband signals in <u>Table 2</u>.

Table 2. I/O expander function

Symbol	Туре	Voltage	NXP Usage	Description
P0	0	VIO	SPI Buffer enable	Enable SPI Buffer when Tri-radio is designed. Active high by default. Pull down required on M.2 board.
P1	0	VIO	IND_RST_15.4	Independent software reset for 802.15.4 radio. Active low by default.
P2	0	VIO	WL_WAKE_IN	MPU/MCU to wake up the Wi-Fi radio. Active low by default.
P3	0	VIO	BT_15.4_W AKE_IN	MPU/MCU to wake up the Bluetooth and 802.15.4 radio. Active low by default.
P4	1	VIO	RST_IND	Independent software reset indicator output signal to host.
P5-P7	Reserved			Not used. Recommend to add test pads on P5-P7.

3 Host and audio interfaces

The wireless connectivity module may support an audio interface.

The modules may also support various host interfaces including SDIO, UART¹, or PCI Express.

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¹ CTS and RTS flow control lines are requested for Bluetooth control.

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For the pin assignments on these interfaces, see the PCI_Express_M.2_Spec document on http://www.pcisig.com.

4 JTAG debug signals

The JTAG debug signals JTAG_TDI, JTAG_TDO, JTAG_TCK, and JTAG_TMS are used to support Software development. Keeping a JTAG connector (<u>Hirose FH12-10S-0.5SH(55)</u>) or test pads on the M.2 module is recommended.

5 Revision history

Table 3 summarizes the changes to this document.

Table 3. Revision history

Revision number	Date	Substantive changes
1	12 November 2020	Initial release.
2	16 September 2021	Updated Section 1 and Section 2.
3	17 January 2022	Added the usage for Tri-Radio design. Removed the JTAG signals from the M.2 pins.
4	30 May 2023	Updated <u>Section 2</u> and added <u>Section 3</u> .

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