TN00029

LPC54018 DMA Linked Transfer from Memory to Memory

1.0 — 29 January 2018 Technical note

Document information

Info	Content
Keywords	LPC540xx, DMA Controller, Linked transfer, memory to memory
Abstract	This technical note describes an example that transfers data from memory to memory via DMA linked transfers.

Revision history

Rev	Date	Description
1.0	20180129	Initial version.

Contact information

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1. Introduction

The LPC540xx is a family of ARM Cortex-M4 based microcontrollers for embedded applications. The LPCXpresso Development Board for LPC540xx MCUs is used in this technical note. For details of the board, see:

https://www.nxp.com/demoboard/om40003

Fig 1. LPC54018 LPCXpresso Development Board

This technical note gives an overview of using on-chip DMA controller to perform memory to memory transfer using linked transfer descriptors.

2. Description

The example uses the LPC54018 on-chip DMA controller for memory to memory transfers. A linked transfer can use any number of descriptors to define a complicated transfer. This can be configured so that a single transfer, a portion of a transfer, one whole descriptor, or an entire structure of links can be initiated by a single DMA request or trigger.

In the example, based on the size of the source buffer to transfer and the transfer block size, the number of descriptors required in the link is calculated. The linked descriptors are setup and the DMA is software triggered to initiate the transfer.

This is a Plain Load example, where the application image is programmed into external SPI flash device on the LPC54018 LPCXpresso Board. On reset, the image is copied to SRAMX and executed from SRAMX. See the LPC540xx User Manual for more details.

Note: See “Getting Started with MCUXpresso SDK for LPC540xx.pdf” document in “docs” folder of SDK package. This document explains how to configure the IDEs for various debug configurations (SRAMX, Plain Load and XIP).

The example has BUFF_LENGTH = 3000 (indicates size of source and destination arrays used in the example; arrays are of type uint32_t), therefore, transfer of 12000 bytes. The TRANSFER_BLOCK_SZ is 4096 bytes and hence the complete transfer requires 3 DMA descriptors.

The “s_dma_descriptor_table” in the file “fsl_dma.c” is located at the SRAMBASE address, 0x20000800. See Fig 2. This table contains the first DMA descriptors of 30 DMA channels.
In the example, DMA channel 0 is used. The first descriptor of DMA channel 0 is located at s_dma_descriptor_table[0]. The “linkToNextDesc” indicates the location of the next descriptor in the DMA link. This location is a separate memory region in the SRAM address space.
A user defined descriptor table “g_linked_desc” in the example contains the remaining descriptors of the chain for DMA channel 0.
s_dma_descriptor[0] links to g_linked_desc[1] at 0x20000410 and g_linked_desc[1] links to g_linked_desc[2] at location 0x20000420.
g_linked_desc[2] is the last descriptor in this example and hence the “linkToNextDesc” is 0x0.

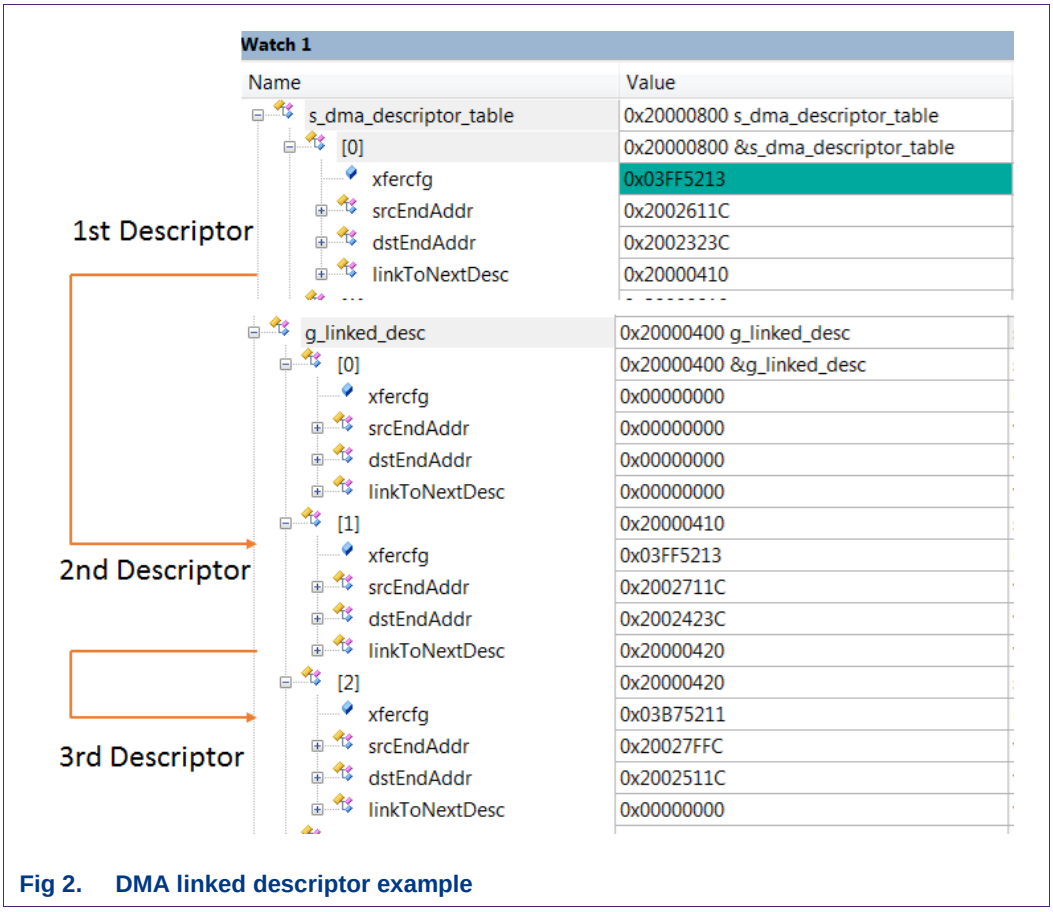

Fig 2. DMA linked descriptor example

The example is available in three tool chains:

- IAR embedded Workbench
- Keil MDK
- MCUXpresso

The Keil and IAR examples are found in:

lpc54018_dma_linked_transfer_keil_iar\boards\lpcxpresso54018\driver_examples\dma\dma_linked_transfer

The MCUXpresso example can be found in the zip file:

lpc54018_dma_linked_transfer_mcux.zip

Note: The MCUXpresso version used in this Tech Note is 10.1.1. In this version, to program a plain load image into Quad SPI device, a binary file must be created from the axf file and using the LinkServer GUI Flash Programmer, the binary file is programmed into the Quad SPI device at location 0x1000 0000. This procedure will change in the next release of MCUXpresso IDE.

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