



Errata

Valis X2ERR/D
Rev. B, 1/2002

Valis Microprocessor
Evaluation System
Errata



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1 Introduction

This document describes the known errata and limitations of the Valis MPMC card for the Sandpoint reference platform. In all cases, if an errata has a workaround, it is applied to the system before shipped to customers.

The errata revision (“A”, “B”, etc.) is updated every time a new problem is found and systems have been shipped. If your current system is a “Valis X2 rev ‘A’”, then it has all rev “A” fixes, but no rev “B” fixes.

The errata should be applied to the published schematics to determine the correct wiring of the MPMC+Sandpoint system (i.e. after changes are applied).

Lastly, note that some errata are not true errors but requests for minor modifications to improve the system. These errata are not performed but may be rolled into possible future revisions of the system, if any.



ERRATA

Table 1: Summary of Valis Errata

#	Type	Problem	Impact	Work-Around	Affects	Rev
1	Assy	L2 BIST runs. R36 should not be populated.	Little.	Remove R36 from BOM.. X3: Make no-pop.	X2	A
2	Des	PLL switch for CPU is scrambled. PLL switch and resistor are mirror image of what was intended. PLL0 should be to pulldown resistor, which PLL1-4 should be on the switch.	Some PLL combos are hard to configure.	None. X3: Redo switch.	X2	A
3	Des	PLL switches for MPC107 are mirror image of hardware spec table.	Little, must mentally flip bits.	None. X3: Redo switch.	X2	A
4	Chip	MCP pin is not OVDD-driven.	For 2.5V configured devices (MPC7410), excessive voltage may be applied.	None (inaccessible). X3: Route MCP* through voltage level buffer U11.	X2	B
5	-	CI*, GBL*, INT* not on logic analyzer header.	None.	None. X3: Connect.	X2	B
6	-	INTA* can be shared with IRQ*	No interrupts in if Winbond agent.	None. X3: Connect.	X2	B
7	Des	SRAM should be 1MB each.	Use 1MB parts.	Replace with K7D803671B-HC25. X3: Default to K7D803671B-HC25.	X2	B

Version	Date	Changes
A	2001 Oct 26	Initial Errata
B	2002 Jan 08	Updates



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