MCIMX8ULP-EVK-UM

MCIMX8ULP-EVK Board User Manual

Rev. 1 — 14 August 2023 **User manual**

Document information

Information	Content
Keywords	MCIMX8ULP-EVK-UM, MCIMX8ULP-EVK, i.MX 8ULP, MCIMX8ULP-BB, MCIMX8ULP-SOM, base board, SOM board
Abstract	MCIMX8ULP-EVK is a design and evaluation platform based on NXP i.MX 8ULP application processor (15 mm x 15 mm package).

1 Overview

MCIMX8ULP-EVK is a design and evaluation platform based on NXP i.MX 8ULP application processor (15 mm x 15 mm package).

MCIMX8ULP-EVK is designed as a system-on-module (SOM) board (MCIMX8ULP-SOM) that connects to an associated base board (MCIMX8ULP-BB).

The SOM board provides 2 GB LPDDR4 memory, 32 MB octal SPI NOR flash memory and 8 MB octal SPI pSRAM on real-time processor domain (RTD), 64 MB octal SPI NOR flash memory on application processor domain (APD), 32 GB eMMC memory, and an NXP PCA9460A power management IC (PMIC).

The base board provides other capabilities, including an M.2 Key-E slot for Wi-Fi/Bluetooth based on NXP IW416, an audio codec, multiple sensors, a 10/100 Mbit/s Ethernet RJ45 connector, a mini-SAS connector for camera, an EPDC connector, two USB 2.0 OTG with Type-C connectors, an HDMI connector, and an alternative MIPI display connector.

In addition, MCIMX8ULP-EVK facilitates software development with the ultimate goal of faster time to market, by supporting operating systems, including Linux, Android, and FreeRTOS.

For information on how to set up and boot MCIMX8ULP-EVK, see *i.MX 8ULP Evaluation Kit Quick Start Guide* provided in the MCIMX8ULP-EVK hardware kit.

This document provides details about MCIMX8ULP-EVK interfaces, power supplies, clocks, connectors, jumpers, push buttons, DIP switch, and LEDs.

1.1 Acronyms

Table 1 lists the acronyms used in this document.

Table 1. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
APD	Application processor domain
BCU	Board Control Utilities
CC	Configuration channel
CSI-2	Camera serial interface - 2
DAC	Digital-to-Analog Converter
DFP	Downstream-Facing Port
DIP	Dual inline package
DNP	Do not populate
dps	Degrees per second
DRP	Dual-Role Power
DSI	Display serial interface
EEPROM	Electrically erasable programmable read-only memory
EPD	Electrophoretic display
EPDC	Electrophoretic Display Controller
FD	Flexible data-rate
FlexCAN	Flexible Controller Area Network

Table 1. Acronyms...*continued*

Acronym	Description
HS	High-speed
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IoT	Internet of Things
LDO	Low-dropout regulator
LED	Light-emitting diode
LPDDR4	Low-Power Double Data Rate Controller
LPI2C	Low-Power Inter-Integrated Circuit
LPUART	Low-Power Universal Asynchronous Receiver/Transmitter
MAC	Medium access control
MIPI	Mobile Industry Processor Interface
MPSSE	Multiprotocol synchronous serial engine
NTC	Negative temperature coefficient
OTG	On-The-Go
PMIC	Power management integrated circuit
PMT	Power Measurement Tool
pSRAM	Pseudo static random-access memory
RTC	Real-time clock
RTD	Real-time processor domain
RTOS	Real-time operating system
SAI	Synchronous Audio Interface
SAS	Serial attached SCSI
SCSI	Small Computer System Interface
SDRAM	Synchronous dynamic random-access memory
SOM	System-on-module
SPDIF	Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
TFT	Thin film transistor
UART	Universal Asynchronous Receiver/Transmitter
UFP	Upstream-Facing Port
USB	Universal Serial Bus
uSDHC	Ultra Secured Digital Host Controller
WLAN	Wireless local area network

1.2 Related documentation

Table 2 lists and explains the additional documents and resources that you can refer to for more information on the board. Some of the documents listed below may be available only under a non-disclosure agreement

(NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Document	Description	Link / how to obtain
i.MX 8ULP Evaluation Kit Quick Start Guide	Provides information on how to set up and boot MCIMX8ULP-EVK.	Available in the MCIMX8ULP-EVK hardware kit
IMXEBOOKDC5 Board User Manual	Provides details of the IMXEBOOKDC5 board, which has an e-paper display.	Contact NXP FAE / sales representative
i.MX 8ULP Processor Reference Manual	Provides a detailed description about the i.MX 8ULP processor and its features, including memory maps, power supplies, and clocks.	
i.MX 8ULP Applications Processor—Consumer Products Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information.	
i.MX 8ULP Applications Processor—Industrial Products Data Sheet		
i.MX 8ULP Hardware Developer's Guide	Provides information about board layout recommendations and design checklists to ensure first-pass success and to avoid board bring-up problems. It is intended to help hardware engineers design and test their i.MX 8ULP processor-based designs.	
i.MX 8ULP Errata	Lists the details of all known silicon errata for i.MX 8ULP.	
MCIMX8ULP-EVK design files	Board schematics, assembly layout	
Board Control Utilities Release Notes	Provides release information about BCU software.	GitHub
i.MX Power Measurement Tool Application Note (AN13119)	Describes i.MX Power Measurement Tool (PMT).	AN13119.pdf
PTN5150A Product Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information.	PTN5150A.pdf
TJA1057 Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information.	TJA1057.pdf
i.MX Linux User's Guide	Describes how to build and install the i.MX Linux board support package (BSP) on the i.MX platform. It also covers special i.MX features and how to use them.	IMX_LINUX_USERS_GUIDE.pdf

1.3 Kit contents

Table 3 lists the items included in the MCIMX8ULP-EVK hardware kit.

Table 3. Kit contents

Item	Quantity
MCIMX8ULP-EVK hardware assembled with two separate boards, MCIMX8ULP-SOM and MCIMX8ULP-BB	1

Table 3. Kit contents*...continued*

Item	Quantity
5 V DC, 5 A power adapter with 2.1 mm x 5.5 mm plug	1
USB Type-A to USB micro-B cable	1
USB Type-A to USB Type-C cable	1
Quick Start Guide	1

1.4 Block diagram

Figure 1 shows the MCIMX8ULP-EVK block diagram.

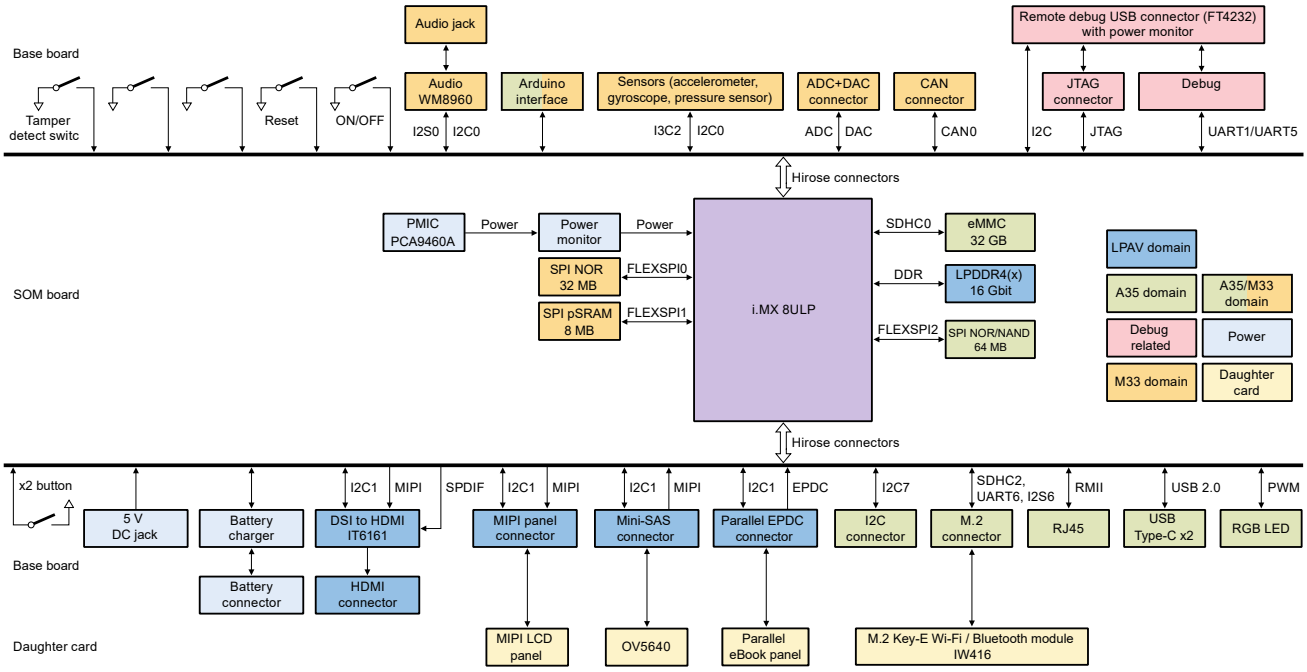


Figure 1. MCIMX8ULP-EVK block diagram

1.5 Board pictures

Figure 2 shows the top view of MCIMX8ULP-EVK.

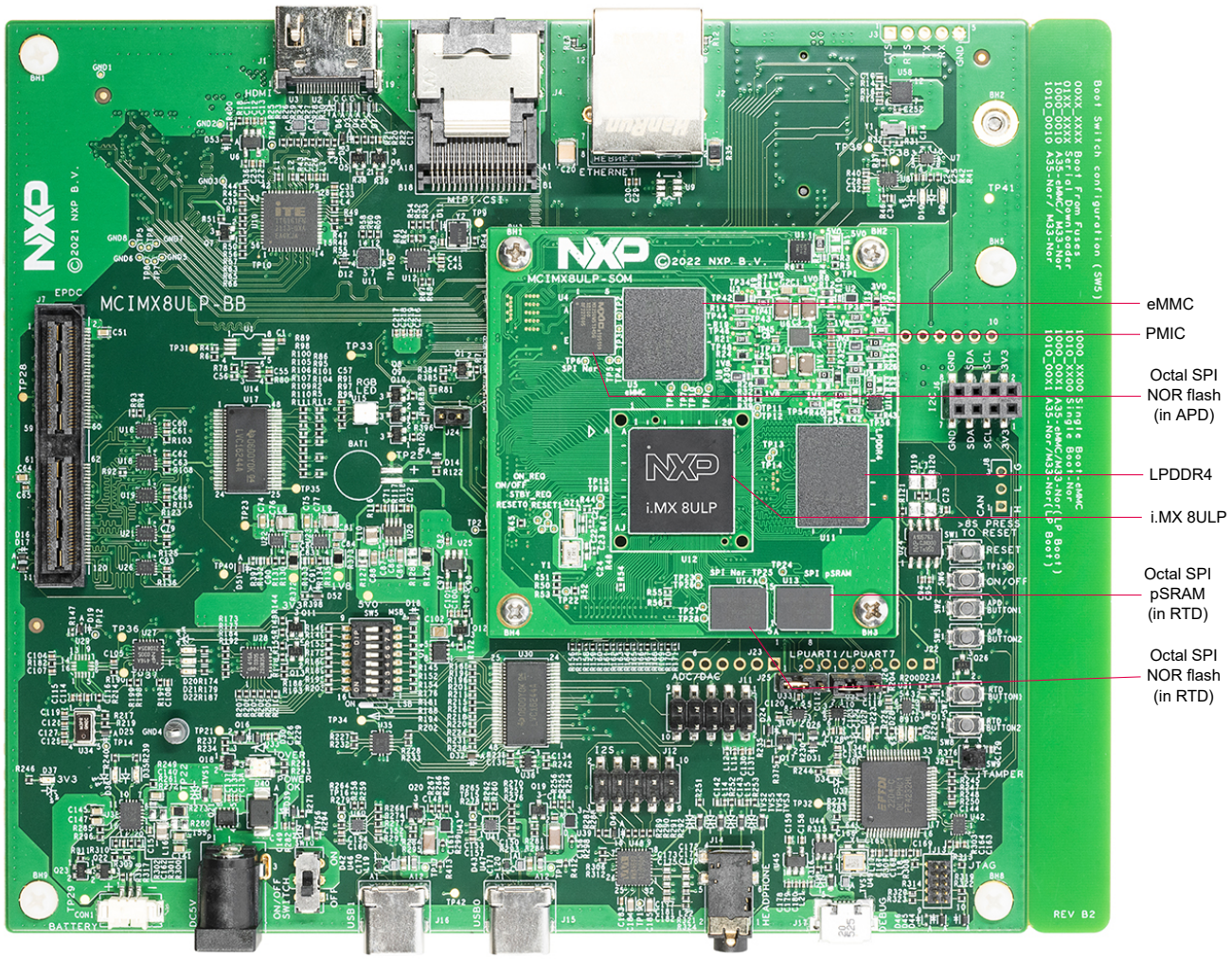


Figure 2. MCIMX8ULP-EVK top view

Figure 3 and Figure 4 show the connectors on the MCIMX8ULP-EVK top and bottom views.

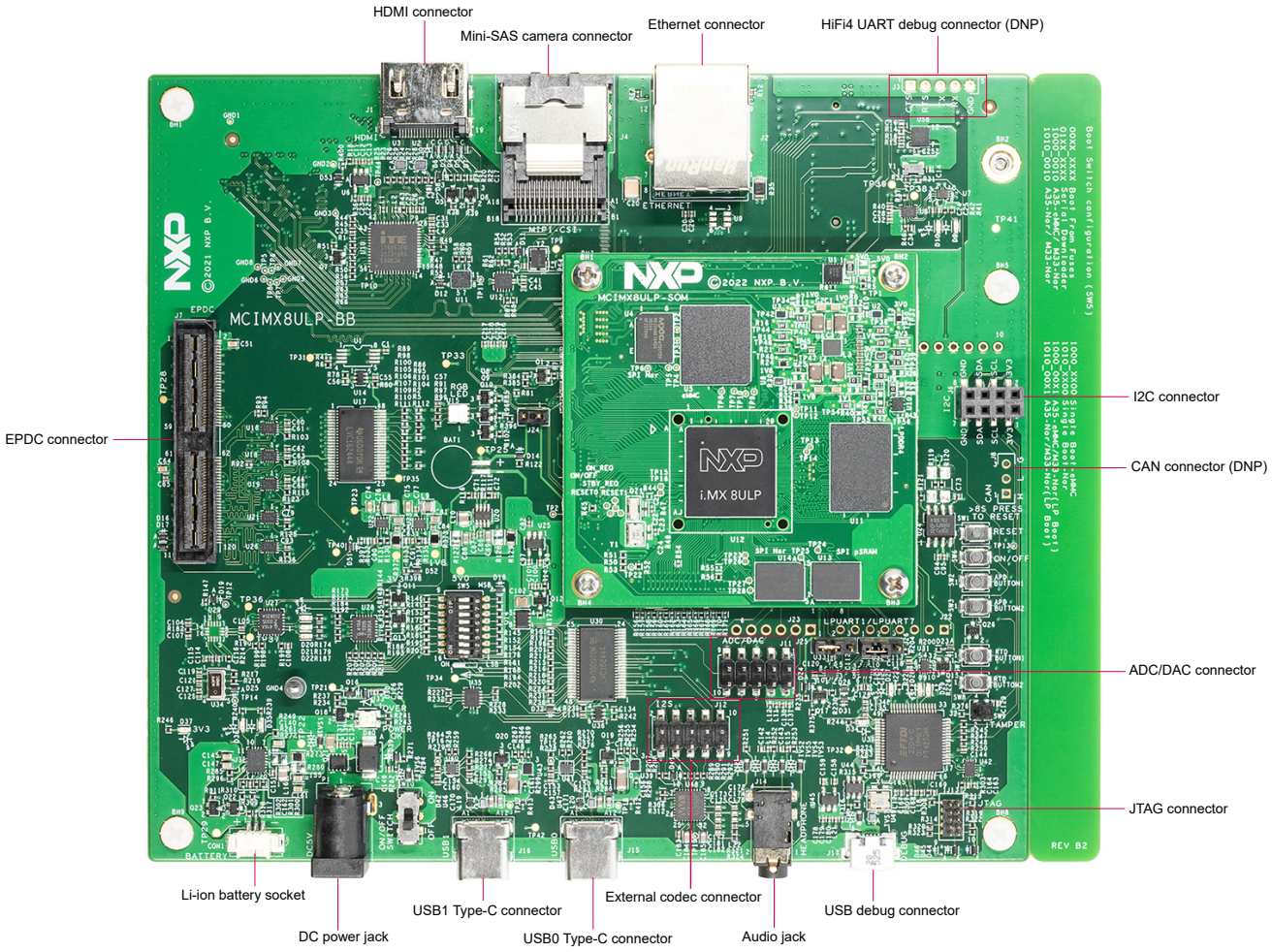


Figure 3. MCIMX8ULP-EVK connectors (board top view)

Note: *In Figure 3, board-to-board connectors between base board and SOM board are hidden.*

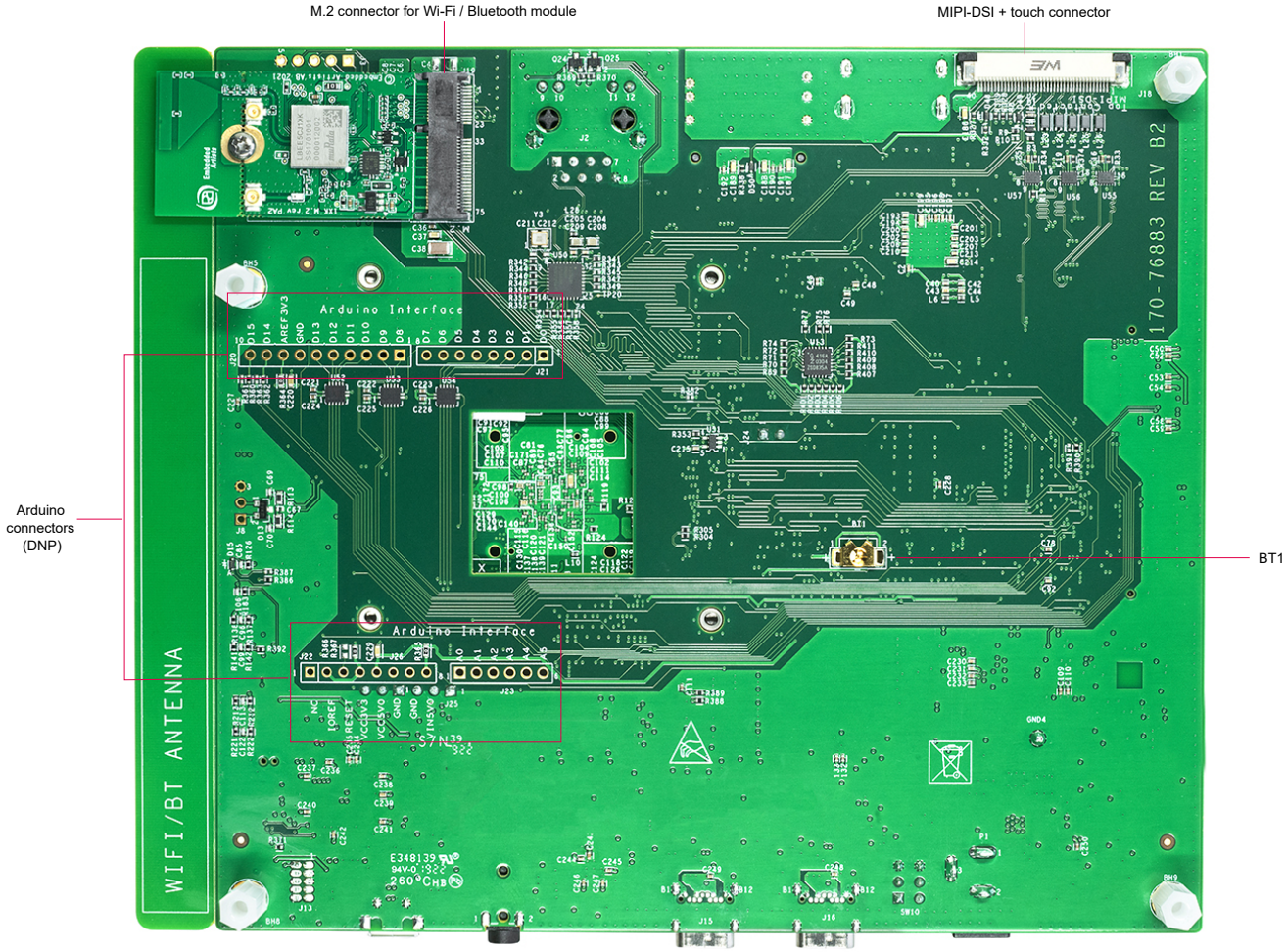


Figure 4. MCIMX8ULP-EVK connectors (board bottom view)

Figure 5 shows the jumpers on MCIMX8ULP-EVK.

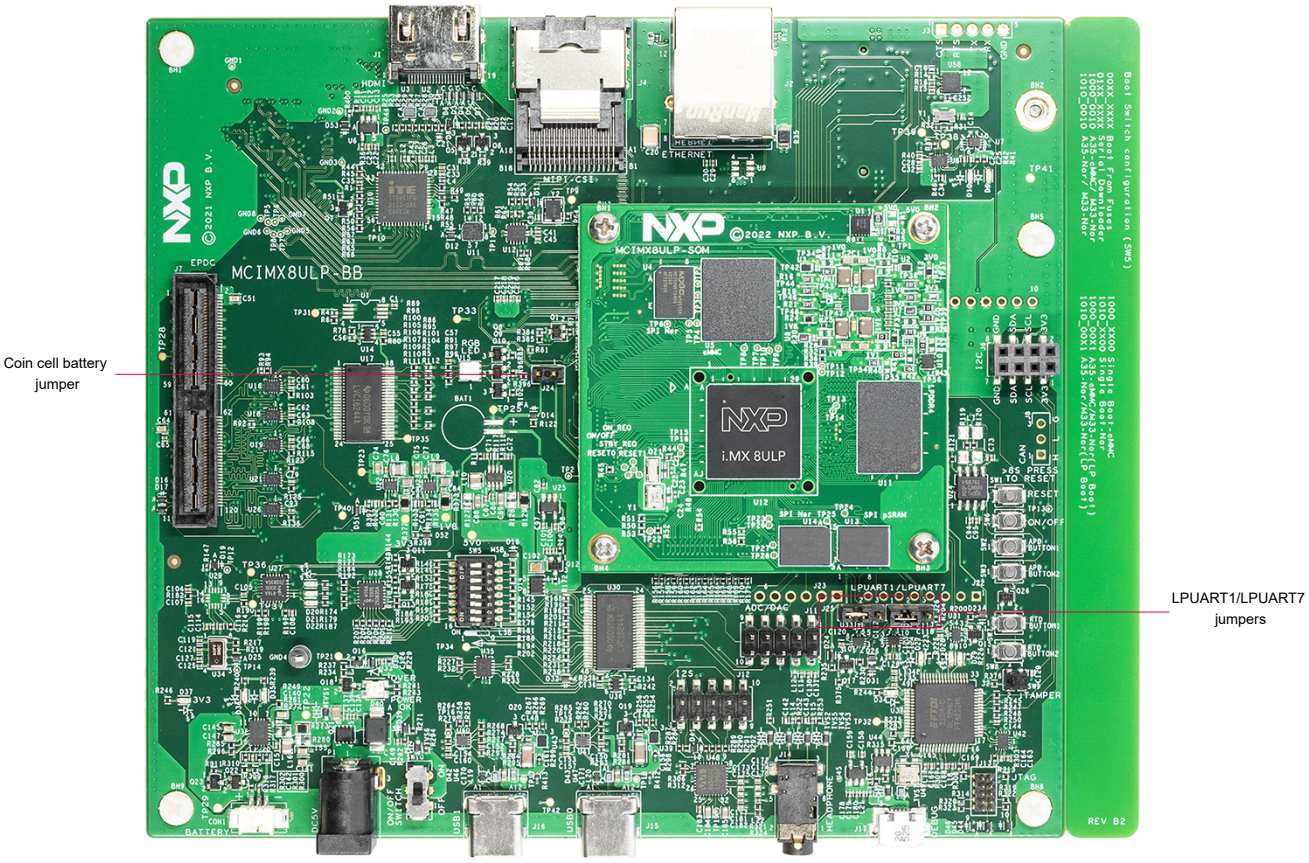


Figure 5. MCIMX8ULP-EVK jumpers

Figure 6 shows the push buttons, DIP switch, and LEDs.

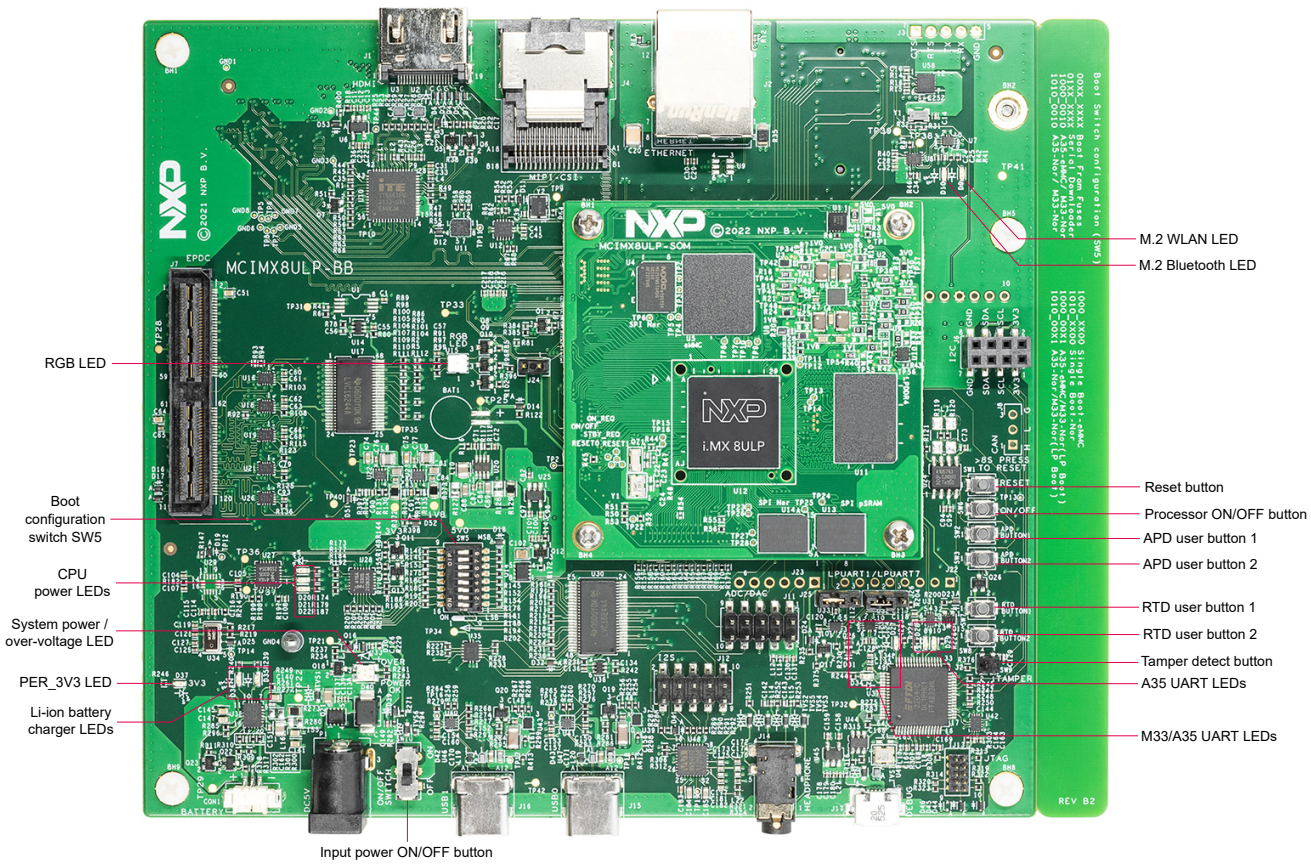


Figure 6. MCIMX8ULP-EVK push buttons, DIP switch, and LEDs

1.6 Board features

Table 4 lists the features of MCIMX8ULP-EVK.

Table 4. MCIMX8ULP-EVK features

Board feature	Target processor feature used	Description
Processor		NXP i.MX 8ULP processor (part number: PIMX8UD7DVP10SA, package size: 15 mm x 15 mm) based on up to two Arm Cortex-A35 cores, each running at 800 MHz frequency, and one Arm Cortex-M33F core running at 216 MHz nominal (RUN) frequency. ***Note:*** *For details on the i.MX 8ULP processor, see i.MX 8ULP Processor Reference Manual.*
LPDDR4/ LPDDR4x memory	LPDDR4 controller	2 GB LPDDR4 SDRAM
eMMC memory	uSDHC0 controller	32 GB eMMC NAND flash memory
FlexSPI interface	FlexSPI0 controller	32 MB octal SPI NOR flash memory
	FlexSPI1 controller	8 MB octal SPI pSRAM memory
	FlexSPI2 controller	64 MB octal SPI NOR flash memory

Table 4. MCIMX8ULP-EVK features*...continued*

Board feature	Target processor feature used	Description
Ethernet interface	ENET controller	10BASE-T / 100BASE-TX RMII Ethernet PHY accessible through an RJ45 jack
USB interface	USB0 controller (USB OTG)	USB 3.1 Type-C connector
	USB1 controller (USB OTG)	USB 3.1 Type-C connector
CAN interface	FlexCAN controller	HS CAN transceiver with option to connect (populate) a 3-pin CAN header
Display interface	MIPI-DSI host controller	One of the following two options can be used: • MIPI-to-HDMI transmitter with an HDMI Type-A connector • MIPI-DSI + touch connector
EPDC interface	EPDC, LPSPI0, and LPI2C1 controllers	120-pin EPDC connector for connecting an e-paper display
Camera interface	MIPI-CSI-2 host controller	Mini-SAS camera connector
I2C interface	LPI2C0, LPI2C1, LPI2C7, and PMIC0 controllers	• LPI2C0, LPI2C1, LPI2C7, and PMIC0 buses from the i.MX 8ULP processor • FTB bus from USB debug host (via USB-to-UART/MPSSE bridge) • 2x4-position I2C connector for remote I2C access
Audio codec	SAI0 controller	One of the following two options can be used: • Audio codec with an audio stereo headphone jack • External codec connector
Sensors	LPI2C0 controller	• 3-axis digital accelerometer / magnetometer (not populated by default) • 3-axis digital accelerometer (G-sensor) / gyroscope • I2C precision pressure sensor
ADC/DAC	ADC1 and DAC0 controllers	10-pin ADC/DAC header
M.2 connector	SAI5, uSDHC2, LPUART6, LPI2C7, and USB1 controllers	75-pin, M.2 Key-E mini card connector having EAR00385 Wi-Fi + Bluetooth card plugged in
Arduino connectors		Arduino socket with four connectors (not populated by default)
I/O expanders		Four I/O expanders to provide remote I/O expansion via the I2C bus interface
Debug interface		USB-to-UART/MPSSE bridge (with a USB debug connector) or a JTAG header for debugging the i.MX 8ULP processor
Boot configuration		8-pin DIP switch for controlling boot configuration
Power		The following power supply options are available: • DC power jack for connecting 5 V external power • Lithium-ion battery socket and battery charger • USB micro-B connector • Coin cell battery option (primary/secondary)
Power monitoring		Five quad-channel power monitors for power and energy monitoring
Clocks		Six crystals/oscillators
Orderable part number		MCIMX8ULP-EVK

1.7 Connectors

Table 5 describes the connectors available on the MCIMX8ULP-BB board. These connectors are shown in Figure 3 and Figure 4.

Table 5. Base board connectors

Part identifier	PCB label	Connector type	Description	Reference section
BT1	–	Coin cell battery holder	Holder for ML414 size coin cell battery. By default, no coin cell battery is present in BT1. With coin cell battery, BT1 can be used to produce LICELL_3V0 supply. ***Note:*** *As an alternative, a lithium coin cell battery BAT1 can be populated to produce LICELL_3V0 supply.*	Section 2.2
P1	DC5V	DC power jack	5 V power supply connector	
J2	ETHERNET	RJ45 jack	Ethernet connector	Section 2.7
J15	USB0	USB 3.1 Type-C connector	USB0 Type-C connector	Section 2.8
J16	USB1		USB1 Type-C connector	
J8 (DNP)	CAN	1x3-pin header	CAN connector	Section 2.9
J1	HDMI	1x19-pin connector	HDMI Type-A connector	Section 2.10
J18	MIPI-DSI	1x40-pin connector	MIPI-DSI + touch connector	
J7	EPDC	2x60-pin connector	EPDC board-to-board connector for connecting the MCIMX8ULP-EVK board to the IMXEBOOKDC5 board	Section 2.11
J4	MIPI-CSI	2x18-pin connector	Mini-SAS camera connector	Section 2.12
J6	I2C	2x4-position receptacle	I2C connector	Section 2.13
J12	I2S	2x5-pin header	External codec connector	Section 2.14
J14	HEADPHONE	3.5 mm audio jack	Audio headphone connector	
J11	ADC/DAC	2x5-pin header	12-bit ADC/DAC connector	Section 2.16
J19	M.2	75-pin connector	M.2 Key-E mini card connector	Section 2.17
J3 (DNP)	–	1x5-pin header	HiFi4 UART debug connector	
J20 (DNP)	Arduino Interface	1x10-pin header	Arduino connector (A35 domain)	Section 2.18
J21 (DNP)		1x8-pin header	Arduino connector (M33 domain)	
J22 (DNP)		1x8-pin header	Arduino connector (power and reset)	
J23 (DNP)		1x6-pin header	Arduino connector (M33 domain)	
J17	DEBUG	USB 2.0 micro-B connector	USB debug connector	Section 2.21.3
J13	JTAG	2x5-pin header	JTAG connector	Section 2.21.4
J5	–	2x40-position receptacle	Board-to-board connectors for base board – SOM board interconnection	For more information on these connectors,
J9	–			

Table 5. Base board connectors*...continued*

Part identifier	PCB label	Connector type	Description	Reference section
J10	–			see MCIMX8ULP-BB board schematics
CON1	BATTERY	Wire-to-board connector	Connector for external battery	

Table 6 describes the connectors available on the MCIMX8ULP-SOM board.

Table 6. SOM board connectors

Part identifier	Connector type	Description	Reference section
J1	2x40-pin header	Board-to-board connectors for base board – SOM board interconnection	For more information on these connectors, see MCIMX8ULP-SOM board schematics
J2			
J3			

1.8 Jumpers

Table 7 describes the MCIMX8ULP-EVK jumpers. The jumpers are shown in Figure 5. All the jumpers are placed on the MCIMX8ULP-BB board.

Table 7. MCIMX8ULP-EVK jumpers

Part identifier	PCB label	Jumper type	Description	Reference section
J24	–	1x2-pin header	Coin cell battery supply jumper: • Open (default setting): Coin cell battery supply LICELL_3V0 is unavailable. • Shorted: Coin cell battery supply LICELL_3V0 is available.	Section 2.2
J25	LPUART1/ LPUART7	1x3-pin header	FT4232H channel D connection jumpers: • Pins 1-2 shorted (default setting): FT4232H channel D is connected to LPUART1 (UART for Arm Cortex-M33F core, UARTM). • Pins 2-3 shorted: FT4232H channel D is connected to LPUART7 (UART for Arm Cortex-A35 core, UARTA).	Section 2.21
J26		1x3-pin header		

1.9 Push and slide buttons

Table 8 describes the MCIMX8ULP-EVK push and slide buttons. The push and slide buttons are shown in Figure 6. All these buttons are placed on the MCIMX8ULP-BB board.

Table 8. MCIMX8ULP-EVK push and slide buttons

Part identifier	PCB label	Button type	Name/function	Description
SW1	RESET	Push button	Reset button	Press and hold SW1 for more than 8 seconds to assert reset to PMIC power outputs except LDO_SNVS (PMIC PCA9460A is present on the SOM board). SW1 is directly connected to the PMIC. The i.MX 8ULP processor gets turned off immediately and reinitiates a boot cycle from the OFF state.

Table 8. MCIMX8ULP-EVK push and slide buttons*...continued*

Part identifier	PCB label	Button type	Name/function	Description
SW6	ON/OFF		Processor ON/OFF button	When pressed, SW6 generates input signal to change power state of the i.MX 8ULP processor (that is, ON or OFF) from the PMIC. SW6 is connected to the ONOFF pin of the i.MX 8ULP processor. It changes the power state of the processor as follows: • In the ON state, if SW6 is held longer than the debounce time, then the power-off interrupt is generated. If it is held longer than the defined max timeout, then the state changes from ON to OFF, and the PMIC_ON_REQ signal is sent to turn off the power outputs of the PMIC. • In the OFF state, if SW6 is held longer than the OFF-to-ON time, then the state changes from OFF to ON, and the PMIC_ON_REQ signal is sent to turn on the power outputs of the PMIC.
SW2	APD BUTTON1		User buttons	Software-defined, connected to application processor domain (APD). SW2 and SW3 are connected to the processor pins PTF7 and PTF30, respectively.
SW3	APD BUTTON2			
SW7	RTD BUTTON1			Software-defined, connected to real-time processor domain (RTD). SW7 and SW8 are connected to the processor pins PTB13 and PTB12, respectively.
SW8	RTD BUTTON2			
SW9	TAMPER		Tamper detect button	SW9 is connected to the TAMPER0 pin of the i.MX 8ULP processor. A tamper is detected when a change happens in the voltage level of this pin. When SW9 is pressed (the voltage level of the TAMPER0 pin changes from 1 to 0) or released (the voltage level of the pin changes from 0 to 1), a tamper signal is sent to the processor.
SW10	ON/OFF SWITCH	Slide button	Input power ON/OFF button	Button for controlling 5 V DC input supply

1.10 DIP switch

MCIMX8ULP-EVK has an 8-pin dual inline package (DIP) switch (SW5) for controlling the i.MX 8ULP boot mode. SW5 is placed on the MCIMX8ULP-BB board.

Each pin of the DIP switch has two positions:

- OFF position (pin has value 0)
- ON position (pin has value 1)

A DIP switch pin can be moved manually from OFF position to ON position and vice versa.

Figure 7 shows the MCIMX8ULP-EVK DIP switch.

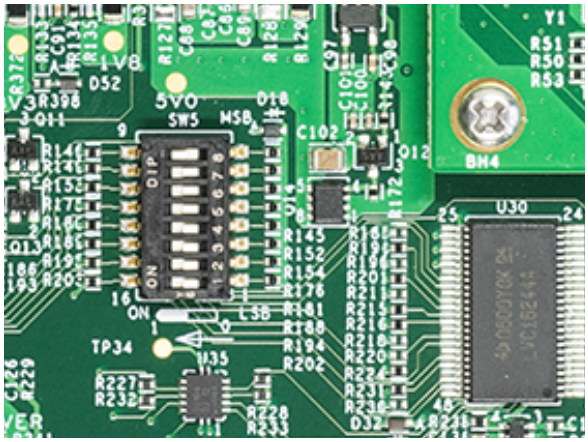


Figure 7. DIP switch

Table 9 describes the MCIMX8ULP-EVK DIP switch settings.

Table 9. Boot configuration settings

SW5[8] (MSB)	SW5[7]	SW5[6]	SW5[5]	SW5[4]	SW5[3]	SW5[2]	SW5[1] (LSB)	Boot mode
BOOT_ MODE1	BOOT_ MODE0	BT1_ CFG14	BT1_ CFG13	BT0_CFG4	BT0_CFG3	BT0_CFG1	BT0_CFG0	
0	0	x	x	x	x	x	x	Boot from Fuses
0	1	x	x	x	x	x	x[1]	Serial Download
1	0	0	0	0	0	1	0	A35 - eMMC / M33 - SPI NOR
1	0	1	0	0	0	1	0	A35 - SPI NOR / M33 - SPI NOR
1	0	0	0	x	x	0	0	Single Boot - eMMC (default setting)
1	0	1	0	x	x	0	0	Single Boot - SPI NOR
1	0	0	0	0	0	x	1	A35 - eMMC / M33 - SPI NOR (Low Power)
1	0	1	0	0	0	x	1	A35 - SPI NOR / M33 - SPI NOR (Low Power)

[1] Set to OFF when the fuse (BT_FUSE_SEL) is not blown.

The default setting for SW5[1:8] is 00000001. With this setting, both A35 and M33 cores boot from eMMC.

Note: *For more details on the i.MX 8ULP boot modes and boot mode configurations, see the "System Boot Flow" chapter in i.MX 8ULP Processor Reference Manual.*

1.11 LEDs

MCIMX8ULP-EVK provides numerous light-emitting diodes (LEDs) for monitoring system status. The information collected from the LEDs can be used for debugging purposes.

Table 10 describes the MCIMX8ULP-EVK LEDs. The LEDs are shown in Figure 6. All these LEDs are placed on the MCIMX8ULP-BB board.

Table 10. MCIMX8ULP-EVK LEDs

Part identifier	LED color	Name/function	Description (when LED is ON)
D9	Green	M.2 card WLAN status	M.2 card wireless LAN is operating correctly.
D10	Orange	M.2 card Bluetooth status	M.2 card Bluetooth is operating correctly.
D22	Orange	CPU power status	CPU power mode 0
D21	Orange		CPU power mode 1
D20	Orange		CPU power mode 2
D29	Orange	A35 UART	Arm Cortex-A35 core receives UART data from the host computer.
D28	Green		Arm Cortex-A35 core sends UART data to the host computer.
D27	Orange	M33/A35 UART	Arm Cortex-M33F / Arm Cortex-A35 core receives UART data from the host computer.
D34	Green		Arm Cortex-M33F / Arm Cortex-A35 core sends UART data to the host computer.
D33	Green	System power status	System power supply is available.
	Red	Over-voltage status	Over-voltage condition is detected.
D35	Green	Lithium-ion battery charger status	Battery charger is charging the lithium-ion battery. ***Note:*** *A blinking LED indicates bad lithium-ion battery. The OFF status indicates that either the battery is fully charged or the charger is not running.*
D36	Orange		Battery charger is getting valid AC input supply.
D37	Orange	PER_3V3 supply status	PER_3V3 supply is available.
U15	Blue	RGB	Connected to the processor pin `PTE6`
	Red		Connected to the processor pin `PTF29`
	Green		Connected to the processor pin `PTF20`

2 Functional description

This section contains the following subsections:

2.1 Processor

The NXP i.MX 8ULP family of processors features advanced implementation of the dual Arm Cortex-A35 cores, in addition to an Arm Cortex-M33F core. This combined architecture enables the device to run a rich operating system (such as Linux) on the Cortex-A35 core and an RTOS (such as FreeRTOS) on the Cortex-M33F core. It also includes a Fusion DSP for low-power audio and a HiFi4 DSP for advanced audio and machine learning applications.

The i.MX 8ULP processor provides a 32-bit LPDDR3/LPDDR4/LPDDR4X memory interface and several other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, and displays. Also, these two coprocessors are connected to the Cortex-M33F core: PowerQuad and Casper.

MCIMX8ULP-EVK includes an i.MX 8ULP processor (PIMX8UD7DVP10SA) with this package information: 485 BGA, 15 mm x 15 mm, 0.5 mm pitch.

For more information about the processor, see the following documents:

- *i.MX 8ULP Applications Processor—Consumer Products Data Sheet* or *i.MX 8ULP Applications Processor—Industrial Products Data Sheet*
- *i.MX 8ULP Processor Reference Manual*

2.2 Board power supply

MCIMX8ULP-EVK is powered up with an external 5 V DC power supply, through DC power jack P1 available on the base board. The 5 V power supply to the board can be turned on/off using a slide button SW10 connected to a P-channel MOSFET Q21.

The power supply devices on the board use the 5 V power to generate required power supplies for PMIC, board-to-board connectors, CAN transceiver, MIPI-to-HDMI transmitter, HDMI connector, USB connectors, pull-up resistors for power monitors, and other peripheral devices.

MCIMX8ULP-EVK also gets external power when it is connected to the host computer through the base board USB micro-B connector. This power is used for powering the FT4232H USB-to-UART/MPSSE bridge.

Figure 8 shows the MCIMX8ULP-EVK power supply diagram.

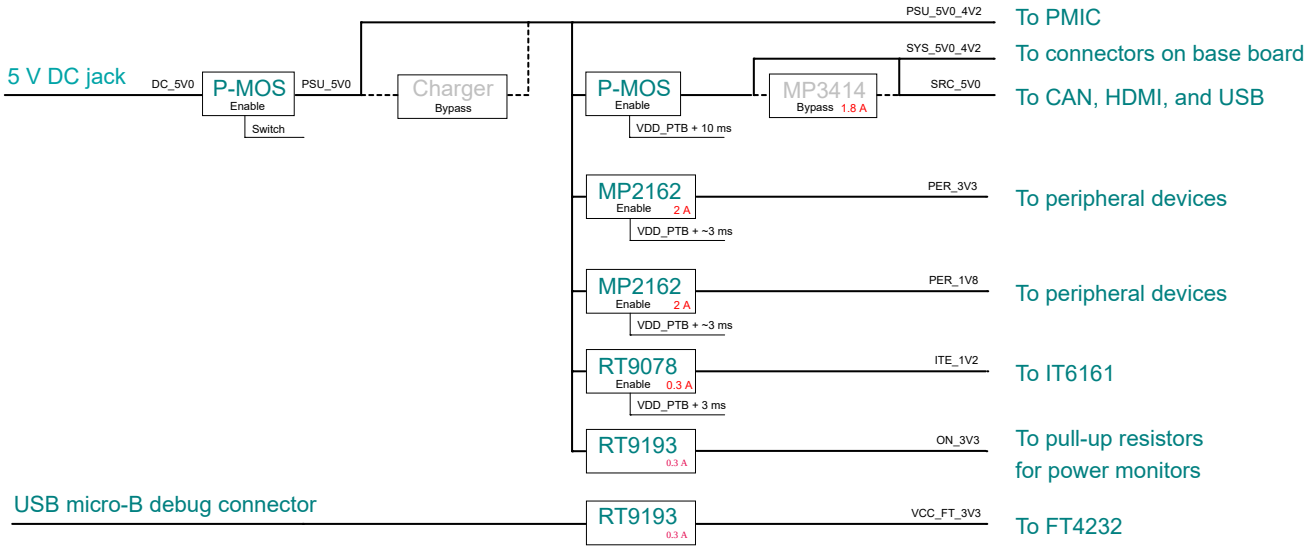


Figure 8. Power supply diagram

Table 11 describes the MCIMX8ULP-EVK power supplies.

Note: *Unless specified explicitly, the part identifiers mentioned in Table 11 correspond to the MCIMX8ULP-BB board.*

Table 11. MCIMX8ULP-EVK power supplies

Power source	Manufacturer and part number	Power supply	Description
External 5 V supply through DC power jack P1	–	DC_5V0 (5 V)	Supplies power to: • P-channel MOSFET Q21 • Red (over-voltage) LED of red-green (D33) LED
P-channel MOSFET Q21	Alpha & Omega Semiconductor AON3419	PSU_5V0 (5 V)	• Supplies power to: – Green (system power status) LED of red-green (D33) LED – Lithium-ion battery charger U38 if the R272 resistor is populated (not populated by default) • One of the two power source options (default option) for producing the PSU_5V0_4V2 supply
Lithium-ion battery charger U38	Monolithic Power Systems MP2617B	PSU_5V0_4V2 (5 V	Supplies power to:

Table 11. MCIMX8ULP-EVK power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
Note: *PSU_5V0_4V2 can be produced from either the PSU_5V0 supply or lithium-ion battery charger U38. By default, PSU_5V0 produces PSU_5V0_4V2 and U38 is bypassed.*		(default value) / 4.2 V) ***Note:*** *PSU_5V0_4V2 is 5 V when produced from PSU_5V0 and it is 4.2 V when produced from U38.*	• PMIC PCA9460A on the SOM board (through board-to-board connectors) • P-channel MOSFET Q14 • Voltage regulators U6, U22, U23, and U25
		BAT_4V2 (4.2 V)	Supplies power to lithium-ion battery socket
		CHG_VCC	Supplies power to D35 and D36 LEDs
P-channel MOSFET Q14	Alpha & Omega Semiconductor AON3419	SYS_5V0_4V2 (5 V / 4.2 V)	• Supplies power to voltage regulator U20 • One of the two power supplies for Arduino header J22 (not populated) • One of the three power supplies for: – MIPI-DSI + touch connector J18 – Mini-SAS camera connector J4 • One of the four power supplies for EPDC board-to-board connector J7
Voltage regulator U20	Monolithic Power Systems MP3414AGJ-Z	SRC_5V0 (5 V)	• Produces the HDMI_5V0 supply for powering HDMI connector J1 • Supplies power to USB host power control switches U39 and U43 • One of the two power supplies for CAN transceiver U24 • Second power supply for EPDC board-to-board connector J7
USB host power control switch U39	NXP NX5P3090UK	USB0_VBUS	Supplies power to: • USB0 Type-C connector J15 • Pull-up resistor on VBUS detection input signal to USB0 CC logic chip U41
USB host power control switch U43	NXP NX5P3090UK	USB1_VBUS	Supplies power to: • USB1 Type-C connector J16 • Pull-up resistor on VBUS detection input signal to USB1 CC logic chip U40
Voltage regulator U6	Richtek Technology RT9078-12GJ5_5P	ITE_1V2 (1.2 V at 0.3 A)	One of the three power supplies for MIPI-to-HDMI transmitter U10
Voltage regulator U22	Monolithic Power Systems MP2162 AGQHT-Z	PER_3V3 (3.3 V at 2 A)	• One of the two power source options for producing the ADC_VDD supply • Supplies power to: – DIP switch SW5 – CPU power status LEDs D20, D21, and D22 – RGB LED U15 and PER_3V3 supply status LED D37 – Audio codec U48 – Audio jack J14 – Accelerometer + magnetometer U29 (not populated)

Table 11. MCIMX8ULP-EVK power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
			– Pressure sensor U34 – USB0 CC logic chip U41 and USB1 CC logic chip U40 – I2C connector J6 – Arduino connector J20 (not populated) – MIPI-DSI I/O multiplexers U55, U56, and U57 – EPDC I/O multiplexers U16, U18, U19, U21, and U26 – JTAG remote control multiplexer U42 – I/O expander U27 – Boot mode remote control buffer/driver U30 – I/O isolation buffer U35 – Load switch U58 • Supplies VCCB power to voltage translators U12, U33, U52, U53, and U54 • Another power supply for: – CAN transceiver U24 – Arduino connector J22 (not populated) • Second power supply for: – MIPI-to-HDMI transmitter U10 – MIPI-DSI + touch connector J18 – Mini-SAS camera connector J4 • Third power supply for EPDC board-to-board connector J7 • One of the two power supplies for: – RMII Ethernet PHY U50 – RJ45 Ethernet connector J2 – External codec connector J12
Load switch U58	Diodes Incorporated AP22814AW5	M2_3V3 (3.3 V)	• Supplies power to: – Crystal oscillator Y1 – M.2 card LEDs D9 and D10 • Supplies VCCA power to voltage translator U7 • One of the two power supplies for M.2 connector J19
Voltage regulator U23	Monolithic Power Systems MP2162 AGQHT-Z	PER_1V8 (1.8 V at 2 A)	• Another power source option (disabled by default) for producing the ADC_VDD supply • Supplies power to: – Crystal oscillator Y2 – G-sensor + gyroscope sensor U11 – Boot mode remote control buffer/driver U17 – I/O expander U8 – Push buttons SW2, SW3, SW6, SW7, and SW8 • Supplies VCCA power to voltage translators U12, U52, U53, and U54 • Supplies VCCB power to voltage translators U7, U31, and U32 • Another power supply for: – RMII Ethernet PHY U50 – RJ45 Ethernet connector J2 – External codec connector J12

Table 11. MCIMX8ULP-EVK power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
			• Another power supply (disconnected by default) for M.2 connector J19 • Third power supply for: – MIPI-to-HDMI transmitter U10 – MIPI-DSI + touch connector J18 – Mini-SAS camera connector J4 • Fourth power supply for EPDC board-to-board connector J7
From PER_3V3 / PER_1V8 supply	–	ADC_VDD (3.3 V / 1.8 V)	Supplies power to ADC/ DAC connector J11
Voltage regulator U25	Richtek Technology RT9193	ON_3V3 (3.3 V at 0.3 A)	Provides always-ON power to pull-up resistors on input signals to power monitors
External supply through USB micro-B connector J17	–	VBUS_USB_DBG	Supplies power to LDO regulator U45
LDO regulator U45	Richtek Technology RT9193	VCC_FT_3V3 (3.3 V at 0.3 A)	• Supplies power to: – LEDs D27, D28, D29, and D34 – I/O expanders U13 and U28 – USB-to-UART/MPSSE bridge U37 – USB-to-UART/MPSSE bridge EEPROM U44 – System ID EEPROM U1 (not populated) – Power monitors on the SOM board (through board-to-board connectors) – Pull-up resistors on I2C signals to the SOM board • Supplies VCCA power to voltage translators U31, U32, and U33
From coin cell battery placed in BT1 holder through jumper J24 (no coin cell battery is present in BT1, by default)	–	LICELL_3V0 (3 V)	Can be used to produce LDO5_CPU_3V0 supply on SOM board
From coin cell battery BAT1 (not populated by default) through jumper J24	–		

The following base board supplies are used on the SOM board (passed through board-to-board connectors):

- PSU_5V0_4V2 (as SOM_5V0_4V2)
- VCC_FT_3V3
- LICELL_3V0

Figure 9 shows the i.MX 8ULP power sequence.

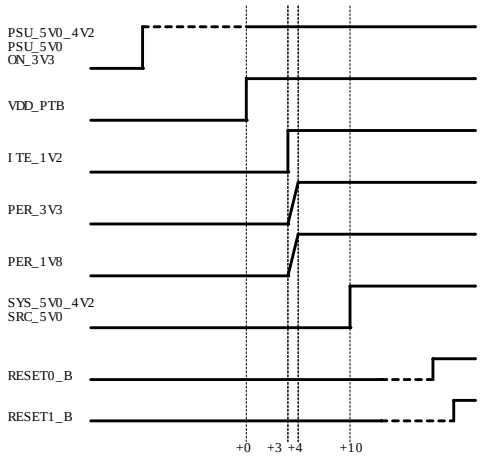


Figure 9. i.MX 8ULP power sequence

Note:

- *A delay of ~10 ms occurs after VDD_PTB ramp up.*
- *VDD_PTB is driven low (>250 ms) by PMIC during cold reset.*

For more details on the i.MX 8ULP power sequence, see the "Power sequencing—system" section in *i.MX 8ULP Applications Processor—Consumer Products Data Sheet* or *i.MX 8ULP Applications Processor—Industrial Products Data Sheet*.

2.2.1 PMIC supplies

MCIMX8ULP-EVK has a power management integrated circuit (PMIC) U6 (NXP PCA9460A), which is placed on the MCIMX8ULP-SOM board. PMIC allows to configure the power supply rails according to the needs of the current application.

Figure 10 shows the PMIC power supplies.

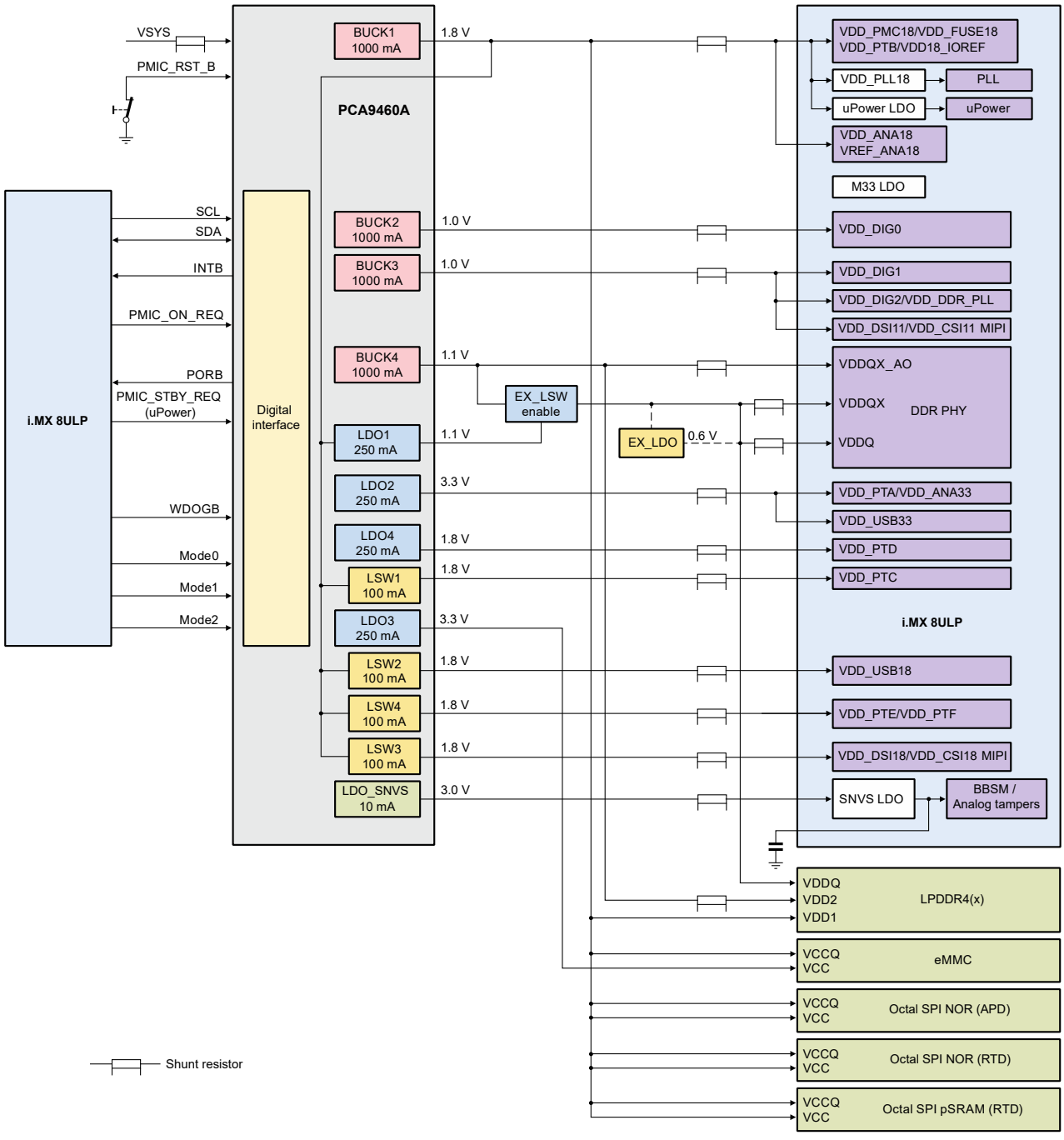


Figure 10. MCIMX8ULP-EVK PMIC diagram

PMIC U6 produces most of the power supplies required on the SOM board. Table 12 describes the power supplies that originate from the PMIC.

Note: *Unless specified explicitly, the part identifiers mentioned in Table 12 correspond to the MCIMX8ULP-SOM board.*

Table 12. PMIC power supplies

Power source	Manufacturer and part number	Power supply	Description
PMIC U6	NXP PCA9460A	LX1: BUCK1_1V8 (1.8 V)	• Produces the following supplies: – BUCK1_DRAM_1V8 – BUCK1_NOR_pSRAM_1V8 – BUCK1_LDOBIAS_1V8 – BUCK1_EMMC_NOR_1V8 • Provides enable input for producing SRC_5 V0, SYS_5V0_4V2, PER_3V3, PER_1V8, and ITE_1V2 supplies on the base board • Supplies power to load switch U8
		LX2: BUCK2_1V0 (1 V)	Supplies power to load switch U3
		LX3: BUCK3_1V0 (1 V)	Supplies power to load switch U2
		LX4: BUCK4_1V1 (1.1 V)	• Produces the following supplies: – BUCK4_CPU_1V1 – BUCK4_DRAM_1V1 • Supplies power to: – Load switch U7 – Load switch U9 (not populated by default)
		LSW1OUT: BUCK1_LSW1_1V8 (1.8 V)	Produces BUCK1_LSW1_CPU_1V8 supply
		LSW2OUT: BUCK1_LSW2_1V8 (1.8 V)	Produces BUCK1_LSW2_CPU_1V8 supply
		LSW3OUT: BUCK1_LSW3_1V8 (1.8 V)	Produces BUCK1_LSW3_CPU_1V8 supply
		LSW4OUT: BUCK1_LSW4_1V8 (1.8 V)	Produces BUCK1_LSW4_CPU_1V8 supply
		LDO1: LDO1_1V1 (1.1 V)[1]	• Produces LDO1_CPU_1V1 supply • One of the two power source options (default option) for producing LDO1_CPU_1V1_0V6 supply • One of the two power source options (default option) for producing LDO1_DRAM_1V1_0V6 supply • Supplies power to voltage regulator U10 if resistor R34 is populated (not populated by default)
		LDO2: LDO2_3V3 (3.3 V)	• Produces LDO2_CPU_3V3 supply • Supplies power (as VDD_PTA) to JTAG connector on the base board (through board-to-board connectors)
		LDO3: LDO3_3V3 (3.3 V)	Produces LDO3_EMMC_3V3 supply
		LDO4: LDO4_1V8 (1.8 V)	Produces the following supplies: • LDO4_CPU_1V8 • LDO4_EMMC_NOR_1V8
		LDO_SNVS: LDO5_3V0 (3 V)	One of the two power source options for producing LDO5_CPU_3V0 supply

Table 12. PMIC power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
From BUCK1_1V8 supply	–	BUCK1_DRAM_1V8 (1.8 V)	One of the three power supplies for LPDDR4/ LPDDR4x DRAM memory U11
		BUCK1_NOR_pSRAM_1V8 (1.8 V)	Supplies power to: • SPI pSRAM memory U13 • SPI NOR flash memory U14
		BUCK1_LDOBIAS_1V8 (1.8 V)	Provides BIAS input to voltage regulator U10 if resistor R43 is populated (not populated by default)
		BUCK1_EMMC_NOR_1V8 (1.8 V)	• Supplies power to SPI NOR flash memory U4 • One of the two power supplies for eMMC NAND flash memory U5
Load switch U8	Texas Instruments TPS22921	BUCK1_CPU_1V8 (1.8 V)	Provides the following powers to the i.MX 8ULP processor: • VDD_PTB • VDD18_IOREF • VDD_FUSE18 • VDD_PLL18 • VDD_PMC18 • VDD_ANA18 and VREFH_ANA18 (through BUCK1_CPU_1V8 filtered supply VDD_ANA_1 V8) • Alternative power supply (disconnected by default) for VDD_PTC and VDD_PTD
Load switch U3	Texas Instruments TPS22925 BNYPHT	BUCK2_CPU_1V0 (1 V)	Provides VDD_DIG0 power to the i.MX 8ULP processor
Load switch U2	Texas Instruments TPS22925 BNYPHT	BUCK3_CPU_1V0 (1 V / 1.1 V)[2]	Provides the following powers to the i.MX 8ULP processor: • VDD_DIG1 • VDD_DIG2 • VDD_DDR_PLL • VDD_DSI11 • VDD_CSI11
Load switch U7	Texas Instruments TPS22925 BNYPHT	LDO1_1V1 (1.1 V)[3]	• Produces LDO1_CPU_1V1 supply • One of the two power source options (default option) for producing LDO1_CPU_1V1_0V6 supply • One of the two power source options (default option) for producing LDO1_DRAM_1V1_0V6 supply • Supplies power to voltage regulator U10 if resistor R34 is populated (not populated by default)
From BUCK4_1V1 supply	–	BUCK4_CPU_1V1 (1.1 V)	Provides VDDQX_AO_DDR power to the i.MX 8ULP processor

Table 12. PMIC power supplies*...continued*

Power source	Manufacturer and part number	Power supply	Description
Load switch U9 (DNP)	Texas Instruments TPS22925 BNYPHT		
From BUCK4_1V1 supply	–	BUCK4_DRAM_1V1 (1.1 V)	Second power supply for LPDDR4/LPDDR4x DRAM memory U11
From BUCK1_ LSW1_1V8 supply	–	BUCK1_LSW1_CPU_1V8 (1.8 V)	Provides VDD_PTC power to the i.MX 8ULP processor
From BUCK1_ LSW2_1V8 supply	–	BUCK1_LSW2_CPU_1V8 (1.8 V)	Provides the following powers to the i.MX 8ULP processor: • VDD_USB0_18 • VDD_USB1_18
From BUCK1_ LSW3_1V8 supply	–	BUCK1_LSW3_CPU_1V8 (1.8 V)	Provides the following powers to the i.MX 8ULP processor: • VDD_DSI18 • VDD_CSI18
From BUCK1_ LSW4_1V8 supply	–	BUCK1_LSW4_CPU_1V8 (1.8 V)	Provides VDD_PTE and VDD_PTF powers to the i.MX 8ULP processor
Voltage regulator U10	Texas Instruments TPS7A1106 PDRVT	LDO1_0V6 (0.6 V)	Another option (alternative option) to produce the following supplies: • LDO1_CPU_1V1_0V6 • LDO1_DRAM_1V1_0V6
From LDO1_1V1 supply	–	LDO1_CPU_1V1 (1.1 V)	Provides VDDQX_DDR power to the i.MX 8ULP processor
From LDO1_1V1 / LDO1_0V6 supply	–	LDO1_CPU_1V1_0V6 (1.1 V (default value) / 0.6 V)	Provides VDDQ_DDR power to the i.MX 8ULP processor
From LDO1_1V1 / LDO1_0V6 supply	–	LDO1_DRAM_1V1_0V6 (1.1 V (default value) / 0.6 V)	Third power supply for LPDDR4/LPDDR4x DRAM memory U11
From LDO2_3V3 supply	–	LDO2_CPU_3V3 (3.3 V)	Provides the following powers to the i.MX 8ULP processor: • VDD_PTA • VDD_ANA33 (through LDO2_CPU_3V3 filtered supply VDD_ANA_3V3) • VDD_USB0_33 • VDD_USB1_33
From LDO3_3V3 supply	–	LDO3_EMMC_3V3 (3.3 V)	Another power supply for eMMC NAND flash memory U5
From LDO4_1V8 supply	–	LDO4_CPU_1V8 (1.8 V)	Provides VDD_PTD power to the i.MX 8ULP processor
		LDO4_EMMC_NOR_1V8 (1.8 V)	Supplies power to CMD signal pull-up resistor and CLK signal pull-up resistor (not populated) for the eMMC NAND flash memory U5
From LDO5_3V0 supply on SOM board or LICELL_3 V0 supply on base board	–	LDO5_CPU_3V0 (3 V)	Provides VDD_VBAT42 power to the i.MX 8ULP processor

[1] PMIC produces LDO1_1V1 supply if resistor R26 is populated (not populated by default). By default, load switch U7 produces LDO1_1V1 supply.
[2] For BUCK3_CPU_1V0, the default voltage is 1 V. In U-Boot, the voltage is updated to 1.1 V by the software.
[3] As an alternative option, LDO1_1V1 supply can be produced directly from PMIC by populating resistor R26.

The processor produces the following output voltages:

- VDD_PTC
- VDD_PTD
- VDD_VBAT18_CAP

PMIC is configured via I2C and external pins, as shown in Table 13.

Table 13. PMIC pins

PMIC pin	Processor pin
SCL	PTB11
SDA	PTB10
MODE0	PTB9
MODE1	PTB8
MODE2	PTB7
PMIC_RST_B	–
PMIC_ON_REQ	PMIC_ON_REQ
PMIC_STBY_REQ	STANDBY_REQ
WDOG_B	PTA14
POR_B	RESET0_B
IRQ_B	PTB15

The following SOM board supplies are used on the base board (passed through board-to-board connectors):

- LDO2_3V3 (as VDD_PTA)
- BUCK1_1V8 (as VDD_PTB)
- BUCK1_LSW4_1V8 (as VDD_PTF)
- Processor output voltages VDD_PTC and VDD_PTD

2.2.2 Power monitoring

MCIMX8ULP-EVK includes five quad-channel power monitors for power and energy monitoring. All the power monitors are placed on the MCIMX8ULP-SOM board.

Table 14 describes the MCIMX8ULP-EVK power monitors.

Table 14. Power monitors

Part identifier	Manufacturer and part number	7-bit I2C address[1]	Power rails
U15	Microchip Technology PAC1934T-I/J6CX	0x10	• BUCK1_CPU_1V8 • BUCK4_CPU_1V1
U16		0x13	• BUCK1_LSW2_CPU_1V8 • BUCK1_LSW3_CPU_1V8 • LDO4_CPU_1V8 • LDO2_CPU_3V3
U17		0x14	• VSYS_5V0_4V2

Table 14. Power monitors...*continued*

Part identifier	Manufacturer and part number	7-bit I2C address[1]	Power rails
			• LDO1_CPU_1V1_0V6 • BUCK4_DRAM_1V1
U18		0x11	• BUCK2_CPU_1V0 • BUCK3_CPU_1V0
U19		0x12	• LDO5_CPU_3V0 • LDO1_CPU_1V1 • BUCK1_LSW1_CPU_1V8 • BUCK1_LSW4_CPU_1V8

[1] A 7-bit address does not include the read/write (R/W) bit.

2.2.2.1 Power rails under measurement

Table 15 and Table 16 provide details about power measurements done by NXP on the MCIMX8ULP-SOM board.

Table 15 shows current and sense resistance values corresponding to the values populated on the MCIMX8ULP-SOM board revision A1, A2, or A3.

Table 16 shows current and sense resistance values corresponding to the values populated on the MCIMX8ULP-SOM board revision A4 or later.

For further details, see the latest MCIMX8ULP-SOM board schematics.

Table 15. Power rails tested on SOM board (revision A1, A2, or A3)

Sequence	Power rail	Typical voltage (V)	Range 1 measurement		Range 2 measurement	
			Current (mA)	Sense resistance (Ω)	Current (mA)	Sense resistance (Ω)
1	*VSYS_5V0_4V2*[1]	5.0	2000	0.02	10	10
2	LDO5_CPU_3V0	3.0	-	250.00	-	-
3	*BUCK1_CPU_1V8*[1]	1.8	900	0.10	9	10
4	LDO2_CPU_3V3	3.3	-	0.10	-	-
	BUCK1_LSW4_CPU_1V8	1.8	-	0.10	-	-
5	*BUCK2_CPU_1V0*[1]	1.0	500	0.05	5	10
	BUCK1_LSW2_CPU_1V8	1.8	-	0.10	-	-
6	*BUCK3_CPU_1V0*[1]	1.0	1000	0.02	5	10
	BUCK4_CPU_1V1	1.1	-	0.40	-	-
	BUCK4_DRAM_1V1	1.1	-	0.05	-	-
7	LDO4_CPU_1V8	1.8	-	0.10	-	-
8	BUCK1_LSW1_CPU_1V8	1.8	-	0.10	-	-
9	LDO1_CPU_1V1	1.1	-	0.10	-	-
	LDO1_CPU_1V1_0V6	1.1	-	0.05	-	-
10	BUCK1_LSW3_CPU_1V8	1.8	-	0.10	-	-

[1] Supports dual-range measurement

Table 16. Power rails tested on SOM board (revision A4 or later)

Sequence	Power rail	Typical voltage (V)	Range 1 measurement		Range 2 measurement	
			Current (mA)	Sense resistance (Ω)	Current (mA)	Sense resistance (Ω)
1	*VSYS_5V0_4V2*[1]	5.0	2000	0.02	10	10
2	LDO5_CPU_3V0	3.0	-	200.00	-	-
3	*BUCK1_CPU_1V8*[1]	1.8	900	0.10	9	10
4	LDO2_CPU_3V3	3.3	-	1.00	-	-
	BUCK1_LSW4_CPU_1V8	1.8	-	1.00	-	-
5	*BUCK2_CPU_1V0*[1]	1.0	500	0.05	5	10
	BUCK1_LSW2_CPU_1V8	1.8	-	1.00	-	-
6	*BUCK3_CPU_1V0*[1]	1.0	1000	0.02	5	10
	BUCK4_CPU_1V1	1.1	-	2.00	-	-
	BUCK4_DRAM_1V1	1.1	-	0.05	-	-
7	LDO4_CPU_1V8	1.8	-	1.00	-	-
8	BUCK1_LSW1_CPU_1V8	1.8	-	1.00	-	-
9	LDO1_CPU_1V1	1.1	-	0.50	-	-
	LDO1_CPU_1V1_0V6	1.1	-	0.05	-	-
10	BUCK1_LSW3_CPU_1V8	1.8	-	2.00	-	-

[1] Supports dual-range measurement

2.2.2.2 Power measurement applications

You can use following two applications to acquire real-time power data from the board. Both the applications are available for download at GitHub.

• BCU software: It is a command-line tool designed to control boards/platforms that support remote control and power measurement. It provides functions, such as on/off key operation, board reset, setting boot mode, JTAG debug, and power measurement through the USB debug port.

• PMT software: It is a GUI-based tool with features similar to BCU. It provides an additional GUI feature that allows real-time profiling of power rails, such as graphical monitoring of power, voltage, and current.

The sampling rate achieved on BCU is higher than the sampling rate achieved on PMT due to the GUI processing on PMT. Due to the higher sampling rate, BCU is used for power acquisition where fine live monitoring is not the primary purpose. For example, remote acquisition.

Due to enhanced GUI, PMT is used for live power monitoring activities during system design, debug phases, and also post-processing analysis.

Power acquisitions made using BCU can be imported into PMT for post-processing analysis; therefore, getting benefits of both the applications:

- Higher sampling resolution of BCU
- Enhanced visibility of power rail activities of PMT

This document only shows the power measurement functions for MCIMX8ULP-EVK. For more information about BCU and PMT, see *Board Control Utilities Release Notes* in GitHub and *i.MX Power Measurement Tool Application Note* (AN13119).

2.3 Clocks

MCIMX8ULP-EVK provides all the clocks required for the processor and peripheral interfaces. Table 17 provides details about the clocks available on MCIMX8ULP-EVK.

Table 17. MCIMX8ULP-EVK clocks

Clock generator	Clock	Frequency	Destination
Clocks on MCIMX8ULP-BB board			
Quartz crystal X1	FT_[OSCI, OSCO]	12 MHz	FT4232H USB-to-UART/MPSSE bridge U37
Crystal oscillator Y1	M2_RTC_CLK	32.768 kHz	M.2 connector J19
Crystal oscillator Y2	CSI_MCLK	24 MHz	Mini-SAS camera connector J4
Quartz crystal Y3	XI, XO	25 MHz	RMII Ethernet PHY U50
Clocks on MCIMX8ULP-SOM board			
Quartz crystal Y1	XTAL0, EXTAL0	24 MHz	i.MX 8ULP processor
Quartz crystal QZ1	XTAL32, EXTAL32	32.768 kHz	i.MX 8ULP processor

2.4 LPDDR4/LPDDR4x memory

The i.MX 8ULP processor provides one Low-Power Double Data Rate Controller (LPDDR4). On MCIMX8ULP-EVK, the LPDDR4 controller connects to a 16 Gbit (2 GB) LPDDR4 SDRAM chip (Micron Technology MT53E512M32D1ZW-046 WT:B). The DRAM chip supports 32-bit data bus width and it provides clock frequency up to 533 MHz.

The DRAM chip is placed on the MCIMX8ULP-SOM board and its part identifier is U11. It is placed on the top side of the board. The data traces to the DRAM chip are not necessarily in sequential order. However, the data traces are added as best determined by the layout and other critical traces for the ease of routing.

Each of the processor and the LPDDR4/LPDDR4x chip uses a 240 Ω 1% resistor for ZQ calibration.

By default, the board supports the LPDDR4 DRAM. Hardware rework is required to support the LPDDR4x DRAM.

Table 18 provides resistor configuration for LPDDR4 and LPDDR4x modes.

Table 18. LPDDR4 and LPDDR4x mode resistor configuration

Resistor	DDR mode	
	LPDDR4 (default mode)	LPDDR4x
R20	Populate	Do not populate
R22	Populate	Do not populate
R33	Populate	Do not populate
R37	Populate	Do not populate
R26	Do not populate	Populate
R34	Do not populate	Populate
R38	Do not populate	Populate
R41	Do not populate	Populate
R43	Do not populate	Populate

2.5 eMMC memory

The i.MX 8ULP processor has three Ultra Secured Digital Host Controllers (uSDHCs): uSDHC0, uSDHC1, and uSDHC2.

MCIMX8ULP-EVK supports communication with the following uSDHC controllers:

- uSDHC0: Connects to the eMMC memory on the SOM board that is discussed in the current section
- uSDHC2: Connects to the M.2 connector on the base board that is explained in Table 32

Table 19 describes the eMMC memory.

Table 19. eMMC memory

Part identifier	Manufacturer and part number	Description
U5 (on SOM board)	Western Digital SDINBDA6-32G-I	32 GB eMMC NAND flash memory

The eMMC memory is the default boot device for the i.MX 8ULP processor on MCIMX8ULP-EVK. For information on boot mode settings, see Table 9.

2.6 FlexSPI interface

The i.MX 8ULP processor has three Flexible Serial Peripheral Interface (FlexSPI) controllers: FlexSPI0, FlexSPI1, and FlexSPI2.

MCIMX8ULP-EVK supports SPI communication with all three FlexSPI controllers through three SPI memory devices, one for each controller. The three SPI memory devices are placed on the MCIMX8ULP-SOM board.

Table 20 describes the SPI memories available on MCIMX8ULP-EVK.

Table 20. SPI memories

FlexSPI controller	Processor domain	SPI memory		
		Part identifier	Manufacturer and part number	Description
FlexSPI0	Real-time processor domain (RTD)	U14	GigaDevice GD25LX256 EBIRY	256 Mbit (32 MB) octal SPI NOR flash memory, supporting clock frequency up to 166 MHz
FlexSPI1		U13	AP Memory APS6408L-OBM-BA	64 Mbit (8 MB) octal SPI pSRAM memory, supporting clock frequency up to 133 MHz
FlexSPI2	Application processor domain (APD)	U4	Macronix MX25UW51345 GXDI00	512 Mbit (64 MB) octal SPI NOR flash memory, supporting clock frequency up to 166 MHz

2.7 Ethernet interface

The i.MX 8ULP processor has an Ethernet controller (ENET) with a 10/100 Mbit/s Ethernet MAC.

MCIMX8ULP-EVK communicates with the Ethernet controller through to a 10BASE-T / 100BASE-TX reduced media-independent interface (RMII) Ethernet PHY U50 (Microchip Technology KSZ8081RNB).

The RMII PHY is connected to an RJ45 Ethernet jack J2 (Hanrun HR911105A), which has integrated magnetics.

2.8 USB interface

The i.MX 8ULP processor has two independent USB 2.0 On-The-Go (OTG) controllers: USB0 and USB1. Both the controllers provide host and device functionality with support for OTG.

On MCIMX8ULP-EVK, each USB OTG controller connects to a USB Type-C connector, as explained in Table 21.

Table 21. USB connectors

USB OTG controller	USB connector		
	Part identifier	Manufacturer and part number	Description
USB0	J15	ANYTRONIC 23 K20101#LCP-582RF	Two USB 3.1 Type-C connectors. Each connector allows an external USB connection using a USB Type-C cable.
USB1	J16		

As an alternative option, the USB1 controller can be connected to the M.2 connector J19. For more information, see Table 32.

For controlling USB host power, each USB OTG port (USB0/USB1) connects to a USB host power control switch U39/U43 (NXP NX5P3090UK). Each USB power switch gets powered by 5 V power supply and it:

- Enables 5 V VBUS power from the associated USB port when the port operates in Host mode
- Produces 5 V VBUS power to be used by the associated USB port when the port operates in Device mode

Each USB power switch sends a power fault indication (through PTF4_USB0_OC/PTF6_USB1_OC signal) to the processor if current consumption for the connected USB device exceeds the maximum allowed limit of 3.3 A.

For controlling USB mode of operation, each USB OTG port (USB0/USB1) connects to a configuration channel (CC) logic chip U41/U40 (NXP PTN5150A). A CC logic chip is used for USB configuration in USB Type-C applications that include CC control logic detection and indication functions.

The following three pins of U41/U40 are used for USB configuration:

- EXT_SEL: Selects configuration channel (CC1/CC2) for communication with USB Type-C connector
- PORT: Sets one of the following modes as USB mode:
  - Upstream-Facing Port (UFP) mode (Device mode)
  - Downstream-Facing Port (DFP) mode (Host mode)
  - Dual-Role Power (DRP) mode (Host or Device mode)
- ADD/CON_DET: In I2C mode, this pin acts as an input pin (ADD) and sets I2C address of the CC logic chip. In Non-I2C mode, this pin acts as an output pin (CON_DET) and notifies the processor if a USB device is detected in the USB connector.

Table 22 describes the settings of EXT_SEL, PORT, and ADD/CON_DET pins of CC logic chips U41 and U40.

Table 22. CC logic chip configuration pin settings

Pin	Value/setting	Description
EXT_SEL	0	Configuration channel 2 (CC2) is selected.
	1 (default value for both U41 and U40)	Configuration channel 1 (CC1) is selected.
PORT	0	USB port is set to UFP mode.
	1	USB port is set to DFP mode.
	Not connected / floating (default setting for both U41 and U40)	USB port is set to DRP mode.

Table 22. CC logic chip configuration pin settings...*continued*

Pin	Value/setting	Description
ADD/CON_DET	0 (default value for U41)	CC logic chip is placed at I2C address 0x3A (7-bit I2C address 0x1D).
	1 (default value for U40)	CC logic chip is placed at I2C address 0x7A (7-bit I2C address 0x3D).
	Not connected / floating	• If no USB connection is detected, then pin has value 0. • If a USB connection is detected, then pin has value 1.

Note: *For more details on the PTN5150A pin assignments, see PTN5150A Product Data Sheet at NXP website.*

2.9 CAN interface

The i.MX 8ULP processor has a Flexible Controller Area Network (FlexCAN) controller, which supports CAN with flexible data-rate (FD).

MCIMX8ULP-EVK supports communication with the FlexCAN controller through a high-speed (HS) CAN transceiver U24 (NXP TJA1057GT/3), which provides differential transmit and receive capabilities to the FlexCAN controller.

Note: *For more details about TJA1057GT/3, see TJA1057 Data Sheet.*

The CAN transceiver drives CAN signals between the FlexCAN controller and a physical two-wire CAN bus:

- It receives analog data from CAN bus lines, converts it into digital data, and sends it to the processor
- It receives digital data from the processor, converts it into analog data, and sends it to the CAN bus lines

The CAN bus terminates at a 3-pin header J8 (not populated by default). Table 23 explains J8 header pinout.

Table 23. CAN header pinout

Pin number	Signal name	Description
1	CAN0_H	CAN transceiver high signal
2	CAN0_L	CAN transceiver low signal
3	GND	Ground

2.10 Display interface

The i.MX 8ULP processor has a MIPI display serial interface (MIPI-DSI) host controller, which operates on the transmit side of a DSI link. The data transmitted by the MIPI-DSI controller can be displayed in one of the following two ways on MCIMX8ULP-EVK:

- As HDMI output (default option): The i.MX 8ULP processor does not support HDMI output. However, MCIMX8ULP-EVK has a MIPI-to-HDMI transmitter U10 (ITE IT6161) that supports HDMI 1.4b display, with SPDIF audio input.
  The data is transmitted to the MIPI-to-HDMI transmitter, which converts MIPI-DSI signals to HDMI signals and transmits them to an HDMI Type-A connector J1. An HDMI cable can be connected from the HDMI connector for displaying the data on a display device.
- Through a MIPI display: The data is transmitted to a MIPI-DSI + touch connector J18. For displaying data using this option, a touch screen display can be attached to the J18 connector.
  The connector supports an LCD panel from Rocktech Displays (RK055HDMIPI4MA0). The LCD panel is a 5.5-inch, 720 x 1280 pixel TFT panel with LED back light and full viewing angle. For more details on the RK055HDMIPI4MA0 LCD panel, see nxp.com.

The selection of one of these options can be made using a set of three multiplexers described in Section 2.19.1.

2.11 EPDC interface

The i.MX 8ULP processor has an Electrophoretic Display Controller (EPDC), which is specifically designed to drive E Ink EPD panels, supporting a wide variety of TFT back planes. The EPDC controller provides SoC integration of the EPD functionality for e-paper applications.

MCIMX8ULP-EVK provides a 120-pin, 0.5 mm pitch high-speed board-to-board connector J7 (Samtec QSH-060-01-L-D-A) for communicating with the EPDC controller. The EPDC connector can be connected to an NXP IMXEBOOKDC5 accessory card, which has an e-paper display.

Note: *For more information on the IMXEBOOKDC5 board, see IMXEBOOKDC5 Board User Manual.*

Table 24 describes the MCIMX8ULP-EVK EPDC connector pinout.

Table 24. EPDC connector pinout

Pin numbers	Signal name	Description	Connection details
43	PTF23_EPDC0_D0	EPDC data 0	Connects to the EPDC controller of the i.MX 8ULP processor.
116	PTF22_EPDC0_D1	EPDC data 1	
110	PTF21_EPDC0_D2	EPDC data 2	
114	PTF20_EPDC0_D3	EPDC data 3	
44	PTF19_EPDC0_D4	EPDC data 4	
46	PTF18_EPDC0_D5	EPDC data 5	
118	PTF17_EPDC0_D6	EPDC data 6	
120	PTF16_EPDC0_D7	EPDC data 7	
68	PTF30_EPDC0_SDCE2	EPDC source driver pulse start data 2	
72	PTF27_EPDC0_SDCE0	EPDC source driver pulse start data 0	
78	PTF26_EPDC0_SDLE	EPDC source driver latch enable	
102	PTF24_EPDC0_SDCLK	EPDC source driver clock	
108	PTF0_EPDC0_SDOE	EPDC source driver output enable	
94	PTE19_EPDC0_GDCLK	EPDC gate driver clock	
96	PTF25_EPDC0_GDSP	EPDC gate driver pulse start	
98	PTE20_EPDC0_GDOE	EPDC gate driver output enable	
100	PTE21_EPDC0_GDRL	EPDC gate driver right/left select	
85	PTE15_EPDC0_ PWRCOM	EPDC VCOM enable	
74	PTE9_EPDC0_VCOM1	EPDC VCOM selection bit 1	
76	PTE10_EPDC0_VCOM0	EPDC VCOM selection bit 0	
37	PTE16_EPDC0_PWRIRQ	EPDC power interrupt	
33	PTE18_EPDC0_ PWRWAKE	EPDC power-ON request	
86	PTE17_EPDC0_ PWRSTAT	EPDC power status	

Table 24. EPDC connector pinout...*continued*

Pin numbers	Signal name	Description	Connection details
50	PTA23_LPSPI0_PCS0	SPI chip select 0	Connects to the LPSPI0 controller of the i.MX 8ULP processor.
52	PTA22_LPSPI0_SCK	SPI clock	
56	PTA20_LPSPI0_SIN	SPI data input	
58	PTA21_LPSPI0_SOUT	SPI data output	
29	PTA13_LPI2C1_SDA	I2C data	Connects to the LPI2C1 controller of the i.MX 8ULP processor.
31	PTA12_LPI2C1_SCL	I2C clock	
64	PTH5_TOUCH_RESET_B	Touch panel reset	-
112	PTA3_TPM0_CH2	-	-
117, 119	PTB5_PTB5	-	-
1, 17, 19, 25	PER_1V8	1.8 V power input	Gets 1.8 V supply.
2, 4, 7, 8	SYS_5V0_4V2	5 V power input	Gets 5 V supply.
5, 45, 47, 49	PER_3V3	3.3 V power input	Gets 3.3 V supply.
11, 13, 39, 41	SRC_5V0	5 V power input	Gets 5 V supply.
65, 67, 69, 71, 73, 75, 77	SYS_5V0_4V2	5 V / 4.2 V power input	Gets 5 V / 4.2 V supply.
6, 12, 18, 23, 24, 30, 36, 42, 48, 54, 60, 80, 83, 84, 87, 92, 93, 103, 104, 106, 111, 113, 115	–	–	Connects to ground.
3, 9, 10, 14, 15, 16, 20, 21, 22, 26, 27, 28, 32, 34, 35, 38, 40, 51, 53, 55, 57, 59, 61, 62, 63, 66, 70, 79, 81, 82, 88, 89, 90, 91, 95, 97, 99, 100, 101, 105, 107, 109	–	–	Unused

2.12 Camera interface

The i.MX 8ULP processor has a MIPI camera serial interface - 2 (MIPI-CSI-2) host controller, which handles image sensor data from camera modules.

On MCIMX8ULP-EVK, the MIPI-CSI-2 controller is connected to a mini-SAS camera connector J4. The connector supports a MIPI-CSI camera module from NXP (MINISASTOCSI). The camera module is based on a 5-megapixel image sensor from OmniVision (OV5640). For more details on the MINISASTOCSI module, see nxp.com.

2.13 I2C interface

The Inter-Integrated Circuit (I2C) protocol is a serial bus protocol that allows multiple peripheral devices to communicate to one or more master devices with a pair of control and data signals.

In MCIMX8ULP-EVK, I2C interface is implemented through I2C buses from two I2C masters, described in Table 25. MCIMX8ULP-EVK also provides a 2x4-position I2C connector for remote I2C access.

Table 25. I2C buses and masters

I2C bus	Processor domain	I2C master	Description
LPI2C0	Real-time processor domain (RTD)	NXP PIMX8UD7DVP10SA (U12 on SOM board)	i.MX 8ULP processor
LPI2C1			
LPI2C7	Application processor domain (APD)		
PMIC0	–		
FTB	–	USB debug host	Host computer connected to MCIMX8ULP-EVK through USB micro-B connector J17. The I2C bus is supported through FTDI FT4232H USB-to-UART/MPSSE bridge (U37).

Table 26 shows the MCIMX8ULP-EVK I2C bus device map.

Note: *Unless specified explicitly, the part identifiers mentioned in Table 26 correspond to the MCIMX8ULP-BB board.*

Table 26. I2C bus device map

I2C bus	7-bit I2C address[1]	Device	Description
I2C master: i.MX 8ULP processor			
LPI2C0 (domain: RTD)	0x1A	Cirrus Logic WM8960 (U48)	Onboard audio codec
	0x1E	NXP FXOS8700CQ (U29)	Accelerometer + magnetometer (not populated by default)
	0x20	NXP PCA6416AHF,128 (U27)	I/O expander
	0x4C	ITE IT6161 (U10)	MIPI-to-HDMI transmitter
	0x60	NXP MPL3115A2 (U34)	I2C precision pressure sensor
	0x6A	STMicroelectronics LSM6DSO (U11)[2]	G-sensor + gyroscope
	[3]	MIPI-CSI camera module	Camera module attached to the mini-SAS camera connector J4
	[4]	Arduino board[5]	Board/module attached to the Arduino socket (J20, J21, J22, and J23 connectors). The Arduino connectors are not populated by default. I2C signals are connected through pins 9 and 10 of the J20 connector.
LPI2C1 (domain: RTD)	[4]	LCD panel	Module attached to the MIPI-DSI + touch connector J18
	[4]	e-paper display module	Module attached to the EPDC connector J7
LPI2C7 (domain: APD)	0x1D	NXP PTN5150A (U41)	USB0 CC logic chip
	0x21	NXP PCAL6408AHK (U8)	I/O expander
	0x3D	NXP PTN5150A (U40)	USB1 CC logic chip
	[4]	External I2C device	Module attached to the I2C connector J6
	[4]	M.2 card	Module attached to the M.2 connector J19

Table 26. I2C bus device map...*continued*

I2C bus	7-bit I2C address[1]	Device	Description
	[4]	Arduino board[5]	Board/module attached to the Arduino socket (J20, J21, J22, and J23 connectors). The Arduino connectors are not populated by default. I2C signals are connected through pins 9 and 10 of the J20 connector.
PMIC0	–	NXP PCA9460A (U6 on SOM board)	PMIC
I2C master: Host computer			
FTB	0x10	Microchip Technology PAC1934T-I/J6CX (U15 on SOM board)	Power monitors
	0x11	Microchip Technology PAC1934T-I/J6CX (U18 on SOM board)	
	0x12	Microchip Technology PAC1934T-I/J6CX (U19 on SOM board)	
	0x13	Microchip Technology PAC1934T-I/J6CX (U16 on SOM board)	
	0x14	Microchip Technology PAC1934T-I/J6CX (U17 on SOM board)	
	0x20	NXP PCA6416AHF,128 (U28)	I/O expanders
	0x21	NXP PCA6416AHF,128 (U13)	
	0x53 (when resistor R6 is populated and resistor R4 is not populated.)	Microchip Technology AT24C02C-XHM-B (U1)	System ID EEPROM (not populated by default)
	0x57 (when resistor R4 is populated and resistor R6 is not populated.)		

[1] A 7-bit address does not include the read/write (R/W) bit.
[2] By default, U11 is placed on the LPI2C0 bus. Alternatively, U11 can be placed on the I3C2 bus, which is in the APD domain.
[3] I2C address depends on the plugged-in camera module. For OV5640 camera module, I2C address is 0x78.
[4] I2C address depends on the plugged-in board/module.
[5] By default, LPI2C0 provides I2C bus to the Arduino board. Alternatively, LPI2C7 can provide I2C bus to the Arduino board.

Table 27 explains the I2C connector J6 (Samtec SSM-104-L-DV) pinout.

Table 27. I2C connector pinout

Pin numbers	Signal name	Description
3, 4	PTE12_LPI2C7_SCL_3V3	I2C clock

Table 27. I2C connector pinout...*continued*

Pin numbers	Signal name	Description
5, 6	PTE13_LPI2C7_SDA_3V3	I2C data
1, 2	PER_3V3	Power supply
7, 8	GND	Ground

2.14 Audio codec

The i.MX 8ULP processor has the following eight Synchronous Audio Interface (SAI) controllers:

- SAI0 and SAI1 for Cortex-M33 domain
- SAI2 and SAI3 for DSP Fusion domain
- SAI4 and SAI5 for Cortex-A35 domain
- SAI6 and SAI7 for LPAV domain

MCIMX8ULP-EVK supports communication with the following SAI controllers:

- SAI0: Connects to an onboard/external audio codec. This connection is discussed in the current section.
- SAI5: Connects to the M.2 connector J19. For more information, see Table 32.

For communication with the SAI0 controller, MCIMX8ULP-EVK provides the following two options:

- Onboard audio codec option: MCIMX8ULP-EVK has an audio codec U48 (Cirrus Logic WM8960), which encodes analog audio into digital audio and decodes digital audio into analog audio. The audio codec supports 24-bit I2S data and 48 kHz sampling rate.
  The onboard audio codec is connected to a 3.5 mm audio stereo headphone jack J14 (Fodot Electronics KJ366EYS) for audio input/output.
- External audio codec option: MCIMX8ULP-EVK has a 2x5-pin header J12 for connecting an external codec.

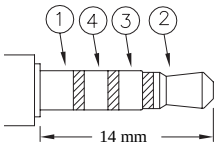
Communication between the onboard/external audio codec and the processor is enabled using I2C bus (for control signals) and I2S bus (for data signals). Table 28 shows control and data signal mapping between the audio codec and the processor.

Table 28. Audio codec control and data signals

I2C/I2S signal	Description	Processor pin
PTA8_LPI2C0_SCL	I2C clock	PTA8
PTA9_LPI2C0_SDA	I2C data	PTA9
PTA7_I2S0_TXD0	I2S transmit	PTA7
PTA2_I2S0_RXD0	I2S receive	PTA2
PTA4_I2S0_MCLK	I2S master clock	PTA4
PTA0_I2S0_RX_BCLK	I2S bit clock	PTA0
PTA1_I2S0_RX_FS	I2S frame sync	PTA1

The audio jack J14 accepts a CTIA standard, 4-pole, 3.5 mm audio plug having pinout as shown in Table 29.

Table 29. Audio plug pinout

Audio plug diagram	Pin number	Description
	1	Microphone
	2	Left-side earpiece
	3	Right-side earpiece
	4	Connected to ground

2.15 Sensors

MCIMX8ULP-EVK has three sensors supported through the LPI2C0 controller of the i.MX 8ULP processor. Table 30 describes the MCIMX8ULP-EVK sensors.

Table 30. MCIMX8ULP-EVK sensors

Part identifier	Manufacturer and part number	Description	7-bit I2C address
U29 (not populated by default)	NXP FXOS8700CQ	14-bit, 3-axis, digital accelerometer + 16-bit, 3-axis, digital magnetometer, supporting an acceleration range of ±2/4/8 g and a magnetic measurement range of ±1200 µT. It operates at 3.3 V. For more information, see nxp.com.	0x1E
U11	STMicroelectronics LSM6DSO	3-axis digital accelerometer (G-sensor) + 3-axis digital gyroscope, supporting an acceleration range of ±2/4/8/16 g and an angular rate range of ±125/250/500/1000/2000 dps. It operates at 1.8 V.	0x6A
U34	NXP MPL3115A2	I2C precision pressure sensor with altimetry, supporting a wide operating range of 20 kPa to 110 kPa. It operates at 3.3 V. Its current consumption is as follows: • Active mode: 2 mA • Standby mode: 2µA For more information, see nxp.com.	0x60

2.16 ADC/DAC

The i.MX 8ULP processor has two Analog-to-Digital Converter (ADC) controllers: ADC0 and ADC1. Each ADC controller supports 22 input channels:

- 11 channels (0A – 10A) with plus (+) polarity
- 11 channels (0B – 10B) with minus (-) polarity

The i.MX 8ULP processor has two Digital-to-Analog Converter (DAC) controllers: DAC0 and DAC1.

MCIMX8ULP-EVK provides a 10-pin header J11 for connecting an external 12-bit ADC/DAC.

Table 31 explains the ADC/DAC connector pinout.

Table 31. ADC/DAC connector pinout

Pin number	Signal name	Description
1	PTA16_PTA16	Connects to i.MX 8ULP ADC1 channel 4A (disconnected by default).
3	PTA15_PTA15	Connects to i.MX 8ULP ADC1 channel 3B.
7	PTA18_PTA18	Connects to i.MX 8ULP ADC1 channel 5A.

Table 31. ADC/DAC connector pinout*...continued*

Pin number	Signal name	Description
9	PTA24_PTA24	Connects to i.MX 8ULP ADC1 channel 5B.
8	DAC0_OUT	Connects to i.MX 8ULP DAC0 output.
10	DAC1_OUT	Connects to i.MX 8ULP DAC1 output.
2, 4	–	Connects to the ADC_VDD supply (3.3 V by default).
5, 6	–	Connects to ground.

2.17 M.2 connector and Wi-Fi/Bluetooth module

MCIMX8ULP-EVK has a 75-pin, M.2 Key-E mini card connector J19 for plugging a Wi-Fi/Bluetooth card. The M.2 mini card connector supports communication with the LPUART6, LPI2C7, uSDHC2, SAI5, and USB1 controller of the i.MX 8ULP processor.

Table 32 explains the M.2 connector pinout.

Table 32. M.2 connector pinout

Pin numbers	Signal name	Connection details
6	M2_LED1_B	Connects to the M.2 card WLAN status LED (D9).
16	M2_LED2_B	Connects to the M.2 card Bluetooth status LED (D10).
20	M2_BT_WAKE	Connects to the `PTF11` pin of the i.MX 8ULP processor via a 30 V Schottky barrier diode, which is pulled up by the software.
50	M2_RTC_CLK	32.768 kHz RTC clock from base board crystal oscillator Y1
23	PTG0_WLAN_RESET	Connects to the `P0` port of I/O expander U8.
54	PTG1_BT_RESET_3V3	Connects to the `P1` port of I/O expander U8 through voltage translator U7.
56	PTG2_WAKEUP_WLAN_3V3	Connects to the `P2` port of I/O expander U8 through voltage translator U7.
8	PTF26_I2S5_TX_BCLK	Connects to the SAI5 controller of the i.MX 8ULP processor.
10	PTF27_I2S5_TX_FS	
12	PTF24_I2S5_RXD3	
14	PTF28_I2S5_TXD0	
9	PTE2_SDHC2_CLK	Connects to the uSDHC2 controller of the i.MX 8ULP processor.
11	PTE3_SDHC2_CMD	
13	PTE1_SDHC2_D0	
15	PTE0_SDHC2_D1	
17	PTE5_SDHC2_D2	
19	PTE4_SDHC2_D3	
22	PTE11_LPUART6_RX	Connects to the LPUART6 controller of the i.MX 8ULP processor.
32	PTE10_LPUART6_TX	
34	PTE8_LPUART6_CTS_b	
36	PTE9_LPUART6_RTS_b	

Table 32. M.2 connector pinout...*continued*

Pin numbers	Signal name	Connection details
58	PTE13_LPI2C7_SDA	Connects to the LPI2C7 controller of the i.MX 8ULP processor.
60	PTE12_LPI2C7_SCL	
3	USB1_DP	Connects to the USB1 controller of the i.MX 8ULP processor (disconnected by default). By default, USB Type-C connector J16 is connected to the USB1 controller.
5	USB1_DM	
21	PTE7_PTE7	Connects to the `PTE7` pin of the i.MX 8ULP processor.
2, 4, 72, 74		Connects to the M2_3V3 supply.
38, 40		Connects to the PER_1V8 supply (disconnected by default).
1, 7, 18, 33, 39, 45, 51, 57, 63, 69, 75		Connects to ground.
24, 25, 26, 27, 28, 29, 30, 31, 35, 37, 41, 42, 43, 44, 46, 47, 48, 49, 52, 53, 55, 59, 61, 62, 64, 65, 66, 67, 68, 70, 71, 73		Unused

Note: *For more details about i.MX 8ULP interfaces, see i.MX 8ULP Processor Reference Manual.*

The MCIMX8ULP-EVK kit comes with a Wi-Fi + Bluetooth card to be used on the M.2 connector. Table 33 describes the Wi-Fi + Bluetooth card.

Table 33. Wi-Fi + Bluetooth card

Feature	Description
Manufacturer	Embedded Artists AB
Part number	EAR00385
Module	Murata LBEE5CJ1XK (also known as 1XK)
Chipset	NXP IW416
WLAN standards	Wi-Fi 4, 802.11 a/b/g/n
Bluetooth standards	5.2 BR/EDR/LE

Note: *For more information on the 1XK M.2 card, see https://www.embeddedartists.com/products/1xk-m-2-module/.*

2.18 Arduino connectors

MCIMX8ULP-EVK has an Arduino socket with the following four connectors:

- J20: 1x10-position receptacle
- J21: 1x8-position receptacle
- J22: 1x8-position receptacle
- J23: 1x6-position receptacle

The two 1x8-position receptacles are placed diagonally opposite to each other. The Arduino socket is pin-compatible with an Arduino Uno revision 3 (R3) board. The Arduino connectors are not populated by default.

Table 34, Table 35, Table 36, and Table 37 show the pinouts of the Arduino connectors.

Table 34. J20 pinout

Pin number	Function	Processor pin	Processor domain
1	LPI2C6_SCL	PTF0	A35
2	FC4_TXD	PTF9	
3	LPSPI5_PCS0 / TPM5_CH0	PTF19	
4	LPSPI5_SOUT / I2C6_SDA / TPM4_CH5	PTF17	
5	LPSPI5_SIN / LPI2C6_SCL / TPM4_CH4	PTF16	
6	LPSPI5_SCK / TPM5_CLKIN	PTF18	
7	GND	–	–
8	PER_3V3 supply	–	–
9	LPI2C0_SDA (default function)	PTA9	M33
	LPI2C7_SDA (alternative function)	PTE13	A35
10	LPI2C0_SCL (default function)	PTA8	M33
	LPI2C7_SCL (alternative function)	PTE12	A35

Table 35. J21 pinout

Pin number	Function	Processor pin	Processor domain
1	LPSPI0_SIN / TPM1_CH0	PTA20	M33
2	LPSPI0_SOUT / TPM1_CH1 / MQS0_RIGHT	PTA21	
3	LPSPI0_SCK / I3C_SCL / MQS0_LEFT	PTA22	
4	LPSPI0_PCS0 / I3C_SDA / MQS0_RIGHT	PTA23	
5	LPUART2_CTS_b / MICFIL0_CLK / WUU0_P17	PTB0	
6	LPUART2_RTS_b / MICFIL0_DATA0 / WUU0_P18	PTB1	
7	LPUART2_TX / MICFIL0_CLK / WUU0_P19	PTB2	
8	LPUART2_RX / MICFIL0_DATA1 / WUU0_P20	PTB3	

Table 36. J22 pinout

Pin number	Function	Description
1	Unused	Supports power/reset connections
2, 4	PER_3V3 supply	
3	RESET_b	
5, 8	SYS_5V0_4V2 supply (5 V by default)	
6, 7	GND	

Table 37. J23 pinout

Pin number	Function	Processor pin	Processor domain
1	ADC1_CH3B / LPSPI1_PCS0 / LPUART0_RX / I3C0_SDA / TPM0_CH0 / SEC0_RX / WUU0_P12	PTA15	M33

Table 37. J23 pinout...*continued*

Pin number	Function	Processor pin	Processor domain
2	ADC1_CH4A / LPSPI1_SIN / LPUART0_CTS_b / TPM0_CH1 / CAN0_TX / WUU0_P13	PTA16	
3	ADC1_CH4B / LPSPI1_SOUT / LPUART0_RTS_b / TPM0_CH2 / CAN0_RX / WUU0_P14	PTA17	
4	ADC1_CH5A / LPSPI1_SCK / LPUART0_TX / TPM0_CH3 / WUU0_P15	PTA18	
5	ADC1_CH5B / I3C0_PUR / WUU0_P16	PTA24	
6	CMP0_IN4 / I3C0_SCL / TPM0_CH5 / SEC0_TX / RTC_CLKOUT	PTA6	

2.19 I/O multiplexers

MCIMX8ULP-EVK I/O multiplexers can be categorized into the following categories:

- Multiplexers for MIPI-DSI signal muxing (see Section 2.19.1)
- Multiplexers for EPDC signal muxing (see Section 2.19.2)
- Multiplexer for JTAG signal muxing (Section 2.19.3)

2.19.1 MIPI-DSI signal muxing

MCIMX8ULP-EVK provides a set of three multiplexers for muxing processor MIPI-DSI signals between MIPI-to-HDMI transmitter U10 and MIPI-DSI + touch connector J18.

Table 38 describes the MIPI-DSI signal multiplexers.

Table 38. MIPI-DSI signal multiplexers

Part identifier	Manufacturer and part number	Description
U55	NXP CBTU02043	2-differential-channel, 1:2 multiplexers
U56		
U57		

At each multiplexer, the routing of MIPI-DSI signals to/from the processor is decided based on the value of the PTH9_MIPI_SWITCH signal from I/O expander U27, as follows:

- 0 (default value): MIPI-DSI signals are routed to the MIPI-to-HDMI transmitter U10.
- 1: MIPI-DSI signals are routed to the MIPI-DSI + touch connector J18.

2.19.2 EPDC signal muxing

The processor signals used for EPDC purposes on MCIMX8ULP-EVK are multiplexed signals and they are also used for other purposes on the board.

For routing the signals to either the EPDC connector J7 (as EPDC signals) or other board devices (such as MIPI-to-HDMI transmitter U10, M.2 connector J19, Ethernet PHY U50, USB-to-UART/MPSSE bridge U37, and RGB LED U15), MCIMX8ULP-EVK provides a set of five multiplexers. These multiplexers are described in Table 39.

Table 39. EPDC signal multiplexers

Part identifier	Manufacturer and part number	Description
U16	Texas Instruments TMUX1574RSVR	4-channel, 1:2 multiplexers with power-off protection
U18		
U19		
U21		
U26		

At each multiplexer, the routing of signals to/from the processor is decided based on the value of the PTH10_EPDC_SWITCH signal from I/O expander U27, as follows:

- 0 (default value): The signals to/from the processor are used for EPDC purposes and are routed to the EPDC connector J7.
- 1: The signals to/from the processor are used for other purposes.

2.19.3 JTAG signal muxing

MCIMX8ULP-EVK provides the following two remote JTAG debugging options for i.MX 8ULP processor:

- Using a JTAG debugger connected through JTAG header J13
- Using USB debug host through channel A of USB-to-UART/MPSSE bridge U37

The selection of one of the above options is made at a 4-channel 1:2 multiplexer U42 (Texas Instruments TMUX1574RSVR), based on the value of the FT_REMOTE_EN signal from I/O expander U28, as follows:

- 0 (default value): JTAG signals from the JTAG connector are routed to the i.MX 8ULP processor.
- 1: JTAG signals from the USB-to-UART/MPSSE bridge channel A are routed to the i.MX 8ULP processor.

2.20 I/O expanders

MCIMX8ULP-EVK has four general-purpose input/output (GPIO) expanders that provide remote I/O expansion via the I2C bus interface.

Table 40 describes the MCIMX8ULP-EVK I/O expanders.

Table 40. I/O expanders

Part identifier	Manufacturer and part number	Description
U27	NXP PCA6416AHF,128	8-bit GPIO expander, which provides remote I/O expansion for the LPI2C0 bus of the i.MX 8ULP processor.
U8	NXP PCAL6408AHK	16-bit GPIO expander, which provides remote I/O expansion for the LPI2C7 bus of the i.MX 8ULP processor.
U28	NXP PCA6416AHF,128	Two 16-bit GPIO expanders, which are controlled by a USB debug host over I2C bus (FTB) of the USB-to-UART/MPSSE bridge (U37).
U13		

2.21 Board control and debug interface

MCIMX8ULP-EVK uses a USB-to-UART/multiprotocol synchronous serial engine (MPSSE) device U37 (FTDI FT4232H) for board control and debug.

The USB-to-UART/MPSSE device acts as a bridge to enable communication between the host computer and the i.MX 8ULP processor. The USB-to-UART/MPSSE bridge is connected to a USB micro-B connector J17 on

the base board that serves as the USB debug connector on the board. A USB cable can be used to connect the board to the host computer.

The USB-to-UART/MPSSE bridge has four UART channels (A, B, C, and D), which allow USB-to-UART connections or USB-to-MPSSE connections (through protocols, such as JTAG, I2C, or SPI). One or both of channels A and B can be configured as MPSSE ports.

Table 41 describes the supported connections for each USB-to-UART/MPSSE bridge channel.

Table 41. USB-to-UART/MPSSE bridge channel connections

Channel	Description
A	Provides a remote JTAG debugging option for the i.MX 8ULP processor system. Another remote JTAG debugging option for the i.MX 8ULP processor system is provided by the JTAG header J13. For more details, see Section 2.21.4. The selection between the two remote JTAG debugging options is made at multiplexer U42. For more details, see Section 2.19.3.
B	Provides I2C control to base board peripheral devices (I/O expanders U13 and U28 and system ID memory U1, not populated) and SOM board peripherals (power monitors). This port also provides reset input to I/O expanders U13 and U28, and accepts interrupt output from I/O expander U28.
C	Can be used as a UART debug port for debugging the Arm Cortex-A35 core of the i.MX 8ULP processor.
D	Can be used as a UART debug port for debugging the Arm Cortex-M33F core or the Arm Cortex-A35 core of the i.MX 8DXL processor. The selection between the two cores is made based on the settings of the jumpers J25 and J26. For more details, see Table 7.

The Board Control Utilities (BCU) software supports board control features, debugging via open-OCD, and also power monitoring. For more details, see https://github.com/NXPmicro/bcu.

The Power Measurement Tool (PMT) also provides board control features and power monitoring with graphical interface. For more details, see AN13119, i.MX Power Measurement Tool.

2.21.1 System ID EEPROM

MCIMX8ULP-EVK provides a memory placeholder U1 for adding a 2 kbit system ID EEPROM (Microchip Technology AT24C02C-XHM-B). U1 is controlled through the I2C bus of channel B of USB-to-UART/MPSSE bridge U37.

This EEPROM can be used to store the following board information:

- Board ID and revision
- SoC ID and revision
- PMIC ID and revision
- Number of measurable power rails on the board
- Board serial number (user-defined)

PMT and BCU Section 2.2.2.2 can detect the type of board connected by reading the EEPROM.

If the connected board is used for the first time, ensure that the EEPROM is programmed correctly. EEPROMs are programmed initially during the board-manufacturing process. However, they can be reconfigured later, if required.

2.21.1.1 EEPROM configuration

Table 42 describes the board-related configuration settings stored in the EEPROM. The "Data" column indicates the configuration values set at the time of board manufacturing. Some of the configuration settings, such as BOARD_ID and BOARD_REV can be modified later using the BCU or PMT tool.

Table 42. Board configuration settings

Setting	Data	Description
BOARD_ID	NXP i.MX8ULP EVK Board	Ensure that BOARD_ID and BOARD_REV are set properly in the PMT yaml configuration file.
BOARD_REV	A0	In BCU, provide the correct [-brev=] value in the command if you are not using the default revision value. ***Note:*** *BOARD_REV value depends on the current revision of the board.*
SOC_ID	i.MX8ULP	This setting is related to the [-board=] option and cannot be changed manually in BCU.
SOC_REV	A0	In BCU, provide the correct [-srev=] value in the command if you are not using the default revision value. ***Note:*** *SOC_REV value depends on the revision of the SoC used on the board.*
PMIC_ID	PCA9460AUK	These settings are related to the [-board=] option and cannot be changed manually in BCU.
PMIC_REV	N/A	
NBR_PWR_RAILS	15	
BOARD_SN	24 (example)	Board-specific serial number, user-defined (range: 1–65535).

For details on how to configure EEPROM, see *Board Control Utilities Release Notes* in GitHub and *i.MX Power Measurement Tool Application Note* (AN13119).

2.21.2 Boot configuration

The i.MX 8ULP processor supports separate boot ROMs for application (A35) and real-time (M33) domains. With separate boot ROMs, the processor supports three boot types, as described in Table 43.

Table 43. Boot types

Boot type	Boot ROM
Single boot (default boot type)	A35 ROM
Dual boot	A35 ROM and M33 ROM
Low-power boot	M33 ROM

The processor supports several boot configurations based on the above boot types. The BT0_CFGn and BT1_CFGn pins are used to select different boot configurations.

Note: *For details about i.MX 8ULP boot modes and boot configurations, see the "System Boot Flow" chapter in i.MX 8ULP Processor Reference Manual.*

On MCIMX8ULP-EVK, the boot configurations can be selected using DIP switch SW5 available on the base board or from the boot configuration stored on the internal fuse of the processor. In addition, the i.MX 8ULP processor can download a program image from a USB connection when configured in serial download configuration.

Table 9 describes how to select boot configuration using SW5.

Note: *For information on how to set up and boot MCIMX8ULP-EVK, see i.MX 8ULP Evaluation Kit Quick Start Guide provided with the MCIMX8ULP-EVK hardware kit.*

2.21.3 USB debug connector

MCIMX8ULP-EVK has a USB 2.0 micro-B connector that allows to connect the i.MX 8ULP processor to the host computer for debugging purposes. Table 44 describes the USB debug connector.

Table 44. USB debug connector

Part identifier	Description
J17	Allows you to create a high-speed USB connection between the i.MX 8ULP processor and the host computer. It also supplies 5 V power (VBUS_USB_DBG) to the board. The USB debug connector is connected to the `USBDP` and `USBDM` pins of the USB-to-UART/ MPSSE bridge U37 (FTDI FT4232H).

2.21.4 JTAG header

MCIMX8ULP-EVK provides a 2x5-pin header J13 that allows JTAG debugging of the i.MX 8ULP processor using a remote debugger. Table 45 shows the JTAG header pinout.

Table 45. JTAG header pinout

Pin number	JTAG signal	Description
2	CON_JTAG_TMS	TAP machine state
4	CON_JTAG_TCK	TAP clock
6	CON_JTAG_TDO	TAP data out
8	CON_JTAG_TDI	TAP data in
10	SYS_Global_RST_b	Cold reset, available by default
	RESET0_B	Warm reset (processor only), not available by default
1	VDD_PTA	Power supply
3, 5, 7, 9	GND	Ground

2.22 PCB information

MCIMX8ULP-EVK consists of two boards:

- MCIMX8ULP-SOM: It is made from FR4 substrate material with standard 6-layer PCB technology
- MCIMX8ULP-BB: It is made from FR4 substrate material with standard 8-layer PCB technology

Table 46 shows the MCIMX8ULP-SOM PCB stack-up information.

Table 46. MCIMX8ULP-SOM PCB stack-up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	Signal	0.33+plating			1.15
	Dielectric		106 RC77%	3.90	2.16
2	GND	0.33+plating			
	Dielectric		1080 RC69%	4.10	2.74
3	Signal	1			

Table 46. MCIMX8ULP-SOM PCB stack-up information*...continued*

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
	Dielectric		7628 RC50% 1506 RC45% 1506 RC45% 7628 RC50%	4.70 4.80 4.80 4.70	27.56
4	Power	1			
	Dielectric		1080 RC69%	4.10	3.12
5	GND	0.33+plating			
	Dielectric		106 RC77%	3.90	2.10
6	Signal	0.33+plating			1.15
Finished:	47.24 (± 4.72) mil				1.20 (± 0.12) mm

Table 47 shows the MCIMX8ULP-BB PCB stack-up information.

Table 47. MCIMX8ULP-BB PCB stack-up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	Signal	0.5+plating			1.31
	Dielectric		1080 RC64%	3.75	2.90
2	GND	1			
	Dielectric		Core 0.1MM 1/1	4.13	3.94
3	Signal	1			
	Dielectric		7628 RC47% 2116 RC58%	4.20 3.91	12.72
4	Power	1			
	Dielectric		Core 0.3MM 1/1	4.47	11.81
5	Power	1			
	Dielectric		2116 RC58% 7628 RC47%	3.91 4.20	12.61
6	Signal	1			
	Dielectric		Core 0.1MM 1/1	4.13	3.94
7	GND	1			
	Dielectric		1080 RC64%	3.75	2.90
8	Signal	0.5+plating			1.31
Finished:	62.992 (± 6.299) mil				1.60 (± 0.16) mm

2.23 Board errata

None

3 Revision history

Table 48 summarizes the revisions to this document.

Table 48. Revision history

Revision number	Release date	Description
1	14 August 2023	Initial public release

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