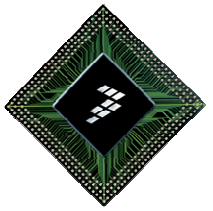
Torpedo ATMC (0M89C)
Ambient Test Elimination Summary



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22July2008

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Room Test Elimination Process (RTE)

- Final Test Room failures were collected from >100K of units with at least 12 different wafer lots in KLM/KTM with mixed packages (80lds and 112lds) per Freescale specification (12MRE10539D).
- Each lot must be processed in a different time frame/day than others over a nine-week period of time to make certain that all lots are non-consecutive.
- Units are representative of production package and temperature mixes.
- Quantities of rejects were verified in KLM as being present and correct prior to a verification that accepted for RTE exercise.
- Zero failure at room flow for the acceptance criteria.

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Reject collection summary

Total sample collected = 136,818 units

Collected from 28 different wafer lots.

All the wafer lots are processed between Q1 and Q2 2008 with over a nine-week period of wafer fab window.

Result :

Achieved zero room test failures when all units were processed to the existing flow at Room Test.

There are proper guardband in place at the Probe, Final Test Cold and Final Test Hot to achieve zero room test failures.

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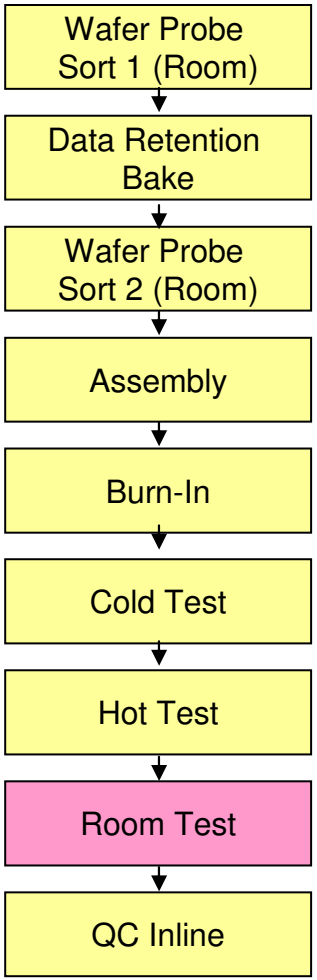
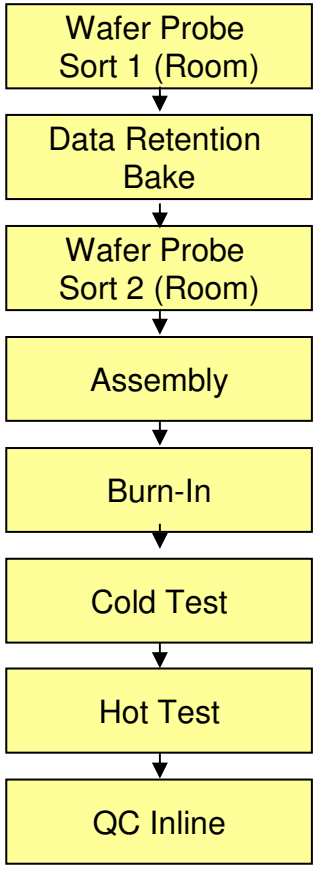
Proposed RTE flow

Current Test Flow



Proposed Test Flow



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Wafer Lots Used

No.	Wafer Lots
1	DD405701
2	DD452431
3	DD457941
4	DD457971
5	DD460821
6	DD466731
7	DD466741
8	DD469541
9	DD469551
10	DD469571
11	DD472431
12	DD475141
13	DD475151
14	DD475161

No.	Wafer Lots
15	DD477231
16	DD480391
17	DD480401
18	DD480451
19	DD480461
20	DD483071
21	DD483081
22	DD485871
23	DD485901
24	DD489041
25	DD492331
26	DD492361
27	DD492363
28	DD509891

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