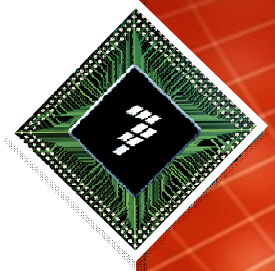
MPC5603/4P, MPC5603/4/5/6/7B & MPC5602/4/6S (Pictus 512K, Bolero 512K/1M5 & Spectrum) Burn-In Improvement (Voltage Acceleration Burn-In) Qual Report

Gordon Campbell
21 November 2011



CAB 11161323M

1. Introduction & Reason for Burn-in Time Optimization

- This report describes an increase in burn-in voltage to allow a burn-in time reduction on Bolero, Pictus and Spectrum products, while maintaining an equivalent stress*
- The reason for this reduction is cycle time optimization.
- Affected Products;
  - MPC5605/6/7B / Bolero 1M5
  - MPC5603/4B / Bolero 512K
  - MPC5603/4P / Pictus 512K
  - MPC5602/4/6S / Spectrum

* To maintain an equivalent burn-in stress compared to the existing production burn-in program, the voltage acceleration factor (Afv) will be increased from 264 to 877 (130C use – see slide 4). This is equivalent to 12 hours burn in reduction based on acceleration factor calculation, as per Freescale Spec 68MWS00084. Qualification units from Bolero 1M5, covering 3 different wafer lots, were used to evaluate the product from the new burn-in conditions.

2. Objective & Considerations

1.1 Objective

- This report details the evaluation results of the outlined Freescale products to demonstrate the qualification of optimized burn-in conditions.

1.2 Considerations

- The evaluation units were first stressed using the proposed equivalent condition and then were submitted for subsequent reliability stress tests.
- Test measurements were performed per AEC-Q100 specification.

3. Burn-In Information

3.1 Comparison of Burn-In Conditions

	Bolero 512K			Bolero 1M5	
	Existing Burn In	New Burn In		Existing Burn In	New Burn In
Temperature (Ta)	125C	125C		125C	125C
Non-NVM Voltage	1.8V	1.92V		1.8V	1.92V
Total Duration	24hrs	12hrs		24hrs	12hrs
Burn-In System	IBE/CC3	IBE/CC3		IBE/CC3	IBE/CC3
Burn-In Board - 64ld	01EKB00201	01EKB00201		-	-
100ld	01EKB00139	01EKB00139		01EKB00139	01EKB00139
144ld	01EKB00140	01EKB00140		01EKB00140	01EKB00140
176ld	-	-		01EKB00138	01EKB00138
Software	Voltage / Duration Change Only*			Voltage / Duration Change Only*	

	Pictus 512K			Spectrum	
	Existing Burn In	New Burn In		Existing Burn In	New Burn In
Temperature (Ta)	125C	125C		125C	125C
Non-NVM Voltage	1.8V	1.92V		1.8V	1.92V
Total Duration	24hrs	12hrs		24hrs	12hrs
Burn-In System	IBE/CC3	IBE/CC3		IBE/CC3	IBE/CC3
Burn-In Board - 64ld	-	-		-	-
100ld	01EKB00113	01EKB00113		-	-
144ld	01EKB00105	01EKB00105		01EKB00141	01EKB00141
176ld				01EKB00142	01EKB00142
Software	Voltage / Duration Change Only*			Voltage / Duration Change Only*	

Note; * Only voltage and duration changes implemented for BI reduction

3. Burn-In Information

3.2 Comparison of Burn-In Voltages

- Non-NVM portion of BI currently 17.5hrs @ 1.8V
- Plan to reduce non-NVM section to 5.5hrs @ 1.92V
  - Non-NVM section includes Module Exercise, Scan & BIST Stresses
- ***Stresses equivalent using voltage acceleration model,*** *from Freescale Specification 68MWS00084B.*

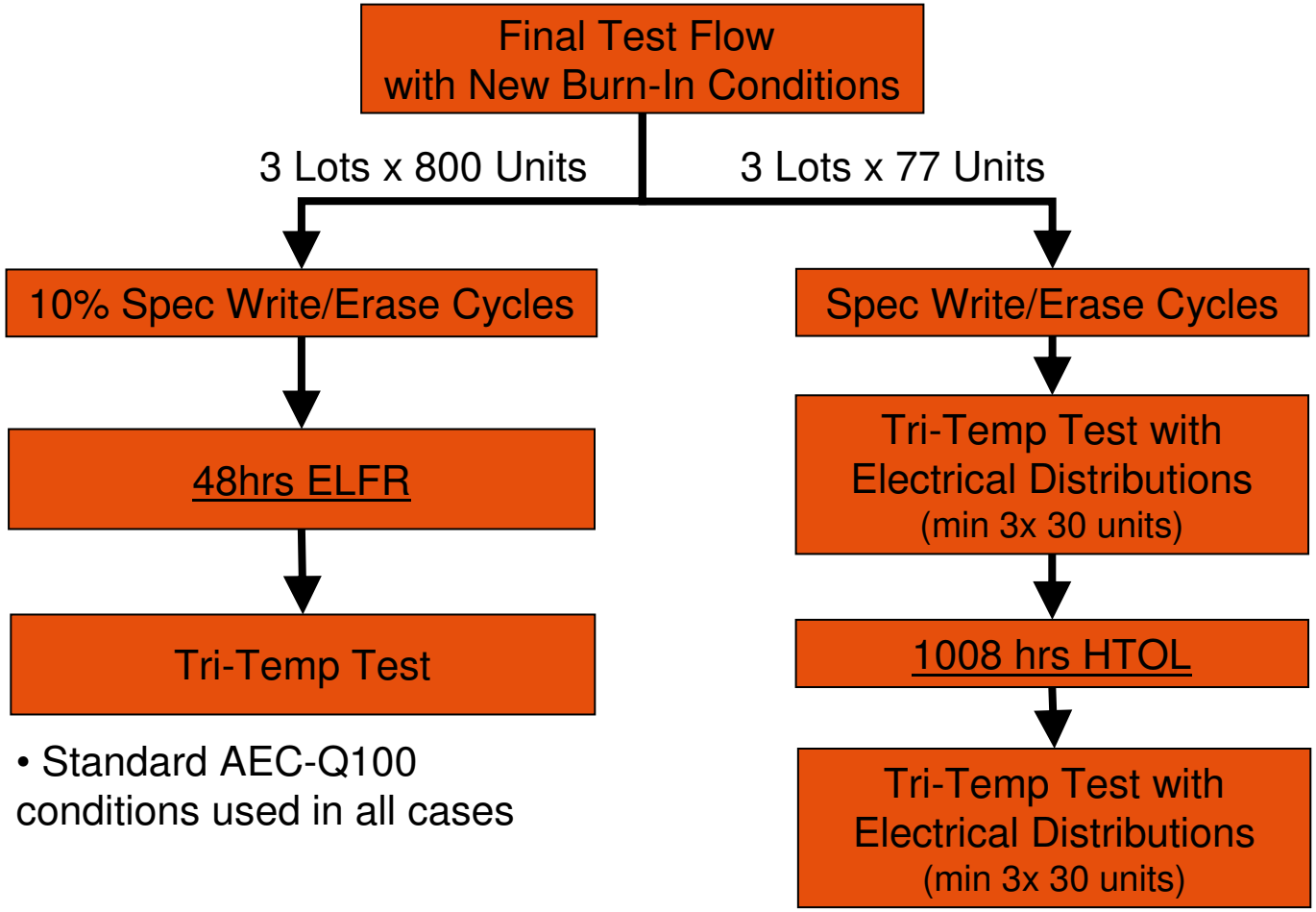
See Appendix A for explanation of terms used below.

		Voltage Acceleration				Temp. Acceleration				Voltage + Temp. Acceleration			
Use Model	Burn In Stress	Stress Vdd	Use Vdd	VAP	AFv	Stress Temp (Tj)	Use Temp (Tj)	EA	AFt	AFtot	Stress Time	On Time	Equiv Years
130C	24hr / 1.8V	1.8	1.28	10	181.3	140	130	0.54	1.46	264.1	17.5	10%	5.277
10% On	12hr / 1.92V	1.92	1.28	10	601.8	140	130	0.54	1.46	877	5.5	10%	5.506
70C	24hr/ 1.8V	1.8	1.28	10	181.3	140	70	0.54	22.12	4010	17.5	100%	8.012
100% On	12hr / 1.92V	1.92	1.28	10	601.8	140	70	0.54	22.12	13315	5.5	100%	8.360

Current BI Conditions
Proposed Conditions

4. Qualification Plan

- Bolero 1M5 identified as driver product for reliability study



- Standard AEC-Q100 conditions used in all cases

5. Qualification Results

5.1 Reliability Stress Results

1008hrs HTOL

Device Type	Wafer Lot	Package	# Fails / Samples
Bolero1M5	DD75959	144 QFP	0/77
Bolero1M5	DD76512	144 QFP	0/77
Bolero1M5	DD76242	144 QFP	0/77

48hrs ELFR

Device Type	Wafer Lot	Package	# Fails / Samples
Bolero1M5	DD76512	144 QFP	1/800*
Bolero1M5	DD75959	144 QFP	0/286
Bolero1M5	DD75959	176 QFP	0/512
Bolero1M5	DD76242	144 QFP	0/527
Bolero1M5	DD76242	176 QFP	0/273

* See 8D report in Appendix B

5. Qualification Results

5.2 Additional Reliability Stress Results

- Pictus & Bolero 256K device qualifications run with 1.92V BI conditions;

1008hrs HTOL

Device Type	Wafer Lot	Package	# Fails / Samples
Pictus 256K	DD82200	100 QFP	0/77
Pictus 256K	DD82482	100 QFP	0/77
Pictus 256K	DD82756	100 QFP	0/77
Bolero 256K	DD88507	100 QFP	0/77

48hrs ELFR

Device Type	Wafer Lot	Package	# Fails / Samples
Pictus 256K	DD82200	100 QFP	0/800
	DD82482		
Bolero 256K	DD88507	100 QFP	0/800

5. Qualification Results

5.3 Electrical Distribution Results

- Parametric data analysed pre and post 1008hrs HTOL on material with 12hr burn-in.
- Drift and Cpk calculated for each parameter, see Appendix C for full results.
- *Results in line with device qualification data.*
- *No issues found.*

5. Qualification Results

5.4 Yield Comparison

Yield Comparison on Pictus Lots
% deivation from mean shown

	Final Test Lot	Burn-In	Cold Test	Hot Test	Room Test
12hr Burn-In	KLMHA1H9NX01	0.35%	-0.81%	0.49%	1.42%
12hr Burn-In	KLMHA1H9NV01	0.24%	0.35%	0.63%	0.39%
12hr Burn-In	KLMHA1H8FW01	0.15%	-0.35%	-0.78%	1.05%
12hr Burn-In	KLMHA1HK9C01	0.45%	-0.80%	-1.65%	-0.19%
24hr Burn-In	KLMHA1H9NX00	-1.41%	-0.17%	1.10%	1.03%
24hr Burn-In	KLMHA1H9NV00	-0.60%	-0.09%	0.33%	0.22%
24hr Burn-In	KLMHA1H8FW00	0.45%	1.54%	0.49%	-2.86%
24hr Burn-In	KLMHA1HK9200	0.36%	0.36%	-0.62%	-1.03%

- *No change from 24hrs to 12hrs*

5.5 Burn-In Voltage Current Study

- Characterisation was carried out to measure the burn-in board current, on the non-NVM stresses, as the voltage is ramped from 1.8V through 1.92V and beyond.
- *Linear VI relationship observed as voltage was increased.*
- *No over-current issues found.*

6. Conclusions

- Recommend increase of burn-in voltage and reduction of burn-in time on Bolero 512K, Bolero 1M5, Pictus 512K & Spectrum devices.

Appendix A

Burn-in Acceleration Factors for Temperature and Voltage

Equivalent Hours in Application = Stress Hours x AF_{Temp} x $AF_{Voltage}$

$AF_{Temp} = \exp((Ea/k)(1/T_{Use} - 1/T_{Stress}))$, where

Ea = activation energy (0.2 – 1.0, generally 0.54)
k = Boltzmann Constant (8.617E-05)
T = Temperature in degrees Kelvin

$AF_{Voltage} = \exp(\beta(V_{Stress}-V_{Use}))$, where

V = Voltage
β = Voltage Acceleration Parameter (specific to technology)
β for CMOS90FG = 10

Note: Industry-standard model. Freescale presented at *International Reliability Physics Symposium 2010* showing data alignment to model

Appendix B; ELFR Fail 8D Report

8D Header

8D Title	CMOS90 LC 12hr Burn-in optimisation
8D Abstract	One unit failed 48hrs ELFR as part of the reliability stressing to qualify a new 12hr optimised burn-in flow for CMOS90 LC products. Failure analysis showed the unit to have a latent defect in the form of a topside scratch.

Corrective action #	76662A	**C.A. Status**	CLOSED
Creation Date	15-SEP-2011	**Incident #**	450954A
ICAP	FIUO	**Point of Failure**	Lifetime Simulation
Freescale Part#	SPC5606BF0MLQ6	**Part Common Name**	BOLERO_1.5M

D1 Team Description

Name	Location	Function	Role
Douglas Blackwood	East Kilbride	NPI Quality	Team Leader
Simon Young	East Kilbride	Product Engineering Manager	Team Member
Gordon Campbell	East Kilbride	Product Engineering	Team Member
Phil Walker	Austin	Device Engineering Manager	Team Member
Doug Garret	Austin	Probe	Team Member
Buddy Torres	Austin	Wafer Fab Quality	Team Member
Tod Yin	Austin	Device Engineering	Team Member
Wei-Keng Wong	KLM	Assembly	Team Member
Huzaimi Mohd Rupingat	KLM	Assembly	Team Member
Ravindra Sanmugam	KLM	Quality	Team Member

Appendix B; ELFR Fail 8D Report

D2 Problem Description

Customer Problem Description	One Bolero1.5M part failed Stop IDD on the VDDLV power supply following 48hrs ELFR as part of a 12Hr Burn-in optimisation.
Reception Centre Findings	The failure was verified using the Credence D10 tester with the J750 test pattern, bolero2_ews21_iddq_exttck_complexon_edt_nbb. The fail unit measured 440uA of Stop IDD current compared to 80uA in a correlation unit.

D3 Containment

Line Item#	1
Trace Code	QAT1041D
Date Code	1041

Lot History	Lot History reviewed through Fab, probe, and Assembly. No abnormalities seen.
Previous Returns	CQI history related to surface damage was checked for similar returns. Pictus (MPC5604P) was checked specifically with the results that 0 returns for this failure mode were seen from 430K in the field. Total shipments for all Microcontrollers (for the last 2 years) were also checked for top surface scratches. Two returns were found (1 in 2010 and 1 in 2011) out of a total of 2.4 billion units shipped giving a 0.8ppb

Appendix B; ELFR Fail 8D Report

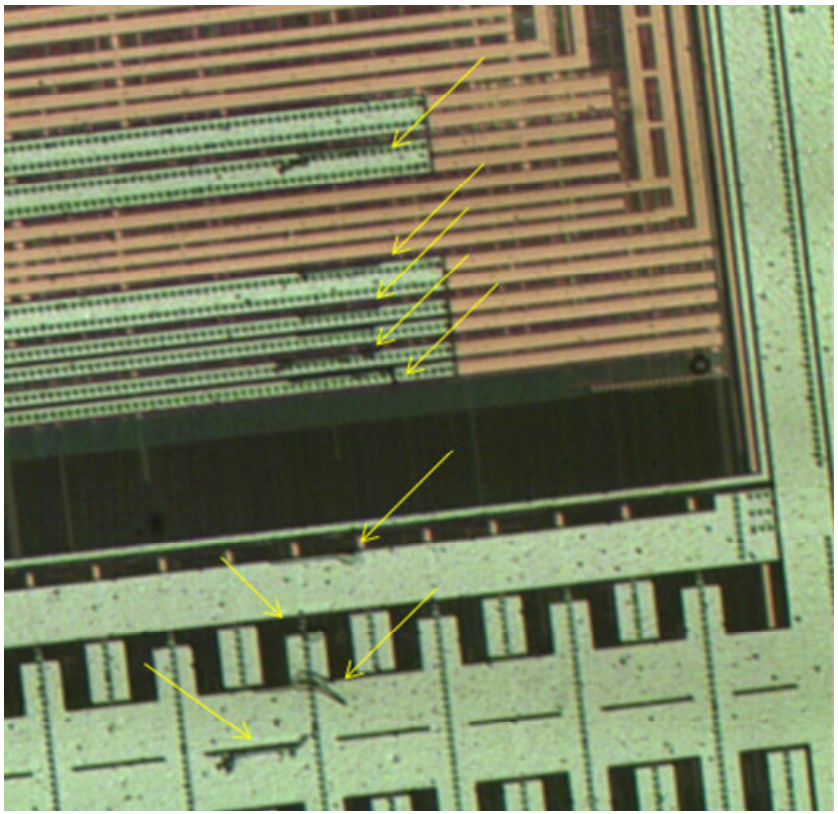
5Y OCCUR

D4 Root Cause
Why1: Device failed ATPG pattern, elevated Stop Idd and IDDQ after ELFR
Why2: SEM images show metal migration through a crack causing leakage
Why3: Passivation cracking led to metal migration through the crack
Why4: Mechanical damage to the surface of the die

5Y ESCAPE

D4 Root Cause
Why1: Failure mechanism did not fail during Probe, Burn-in, Final Test
Why2: Device failed due to latent failure mechanism
Why3: Failure mode accelerated by time and temperature
Why4: Latent defect pulled out by reliability stressing

Appendix B; ELFR Fail 8D Report

Line item #	PA Summary
1	Yield Assist diagnosis of three failing scan patterns placed callouts in the general area of surface damage with a single callout directly underneath a crack A passivation integrity etch was performed, evidence of mechanical damage was found on the surface of the die (Image1). A SEM image of the surface shows the cracking in more detail (Image2).  ***Image1:*** *Low magnification optical image shows top surface damage to metal highlighted by passivation integrity etch over several metal lines*

Appendix B; ELFR Fail 8D Report

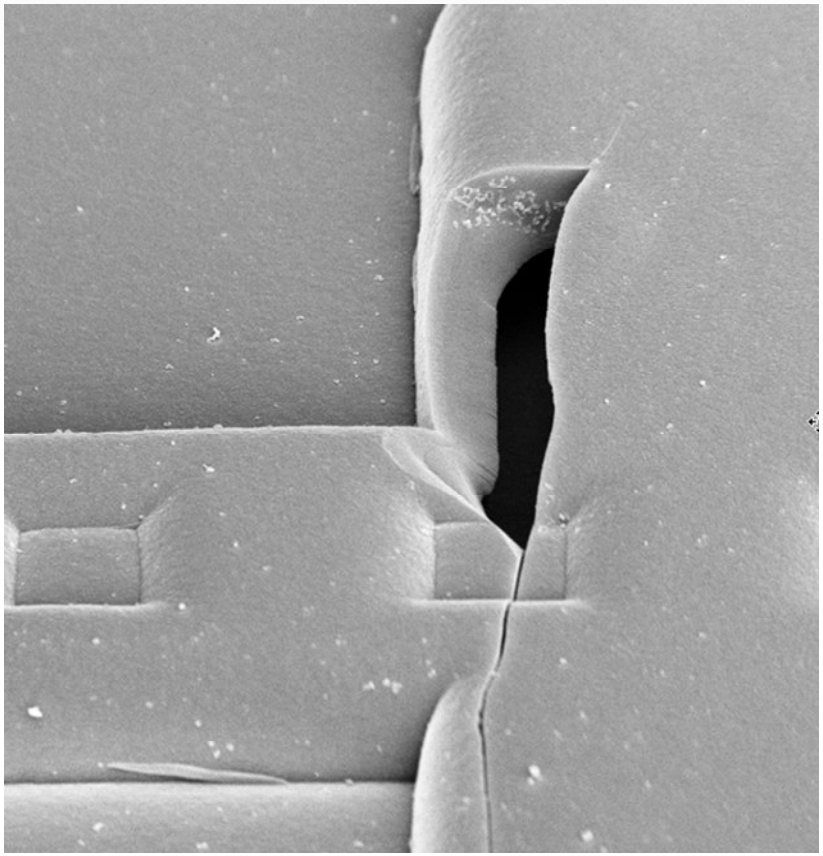


Image2: *SEM image show top surface mechanical damage to passivation*

Appendix B; ELFR Fail 8D Report

Sequential cross sections through the area highlighted by the yield tool (Image3) showed metal migration through a stress crack (Image4). EDS analysis revealed the defect to consist of copper.

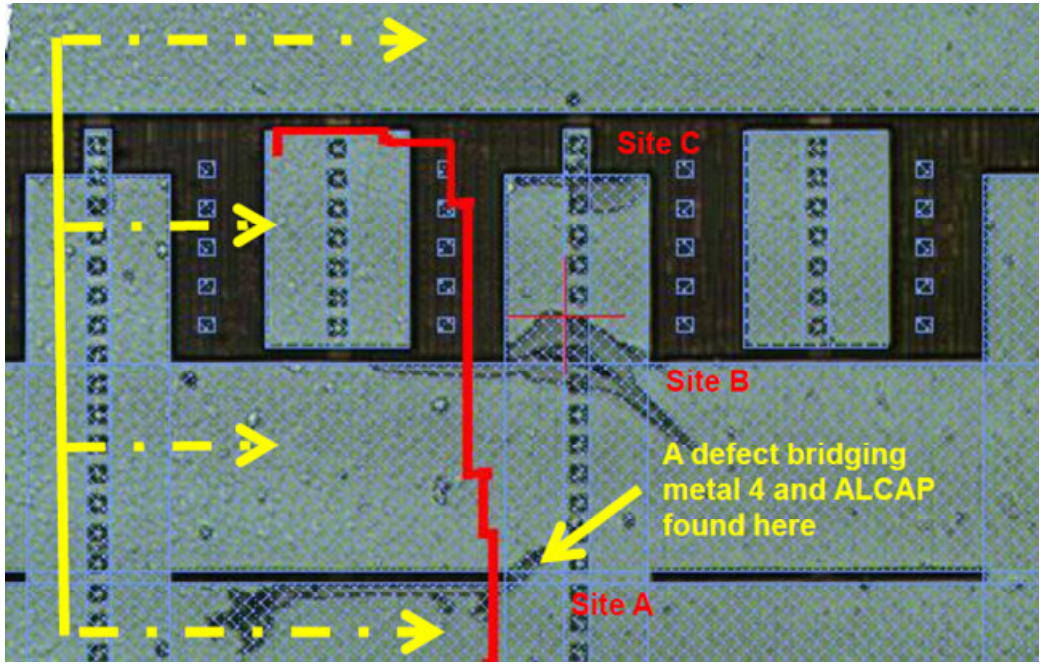


Image3: *Composite image show top surface mechanical damage to passivation synchronised with the yield analysis tool and the failing signal (red line). Cross sections performed as per yellow hatched lines*

Appendix B; ELFR Fail 8D Report

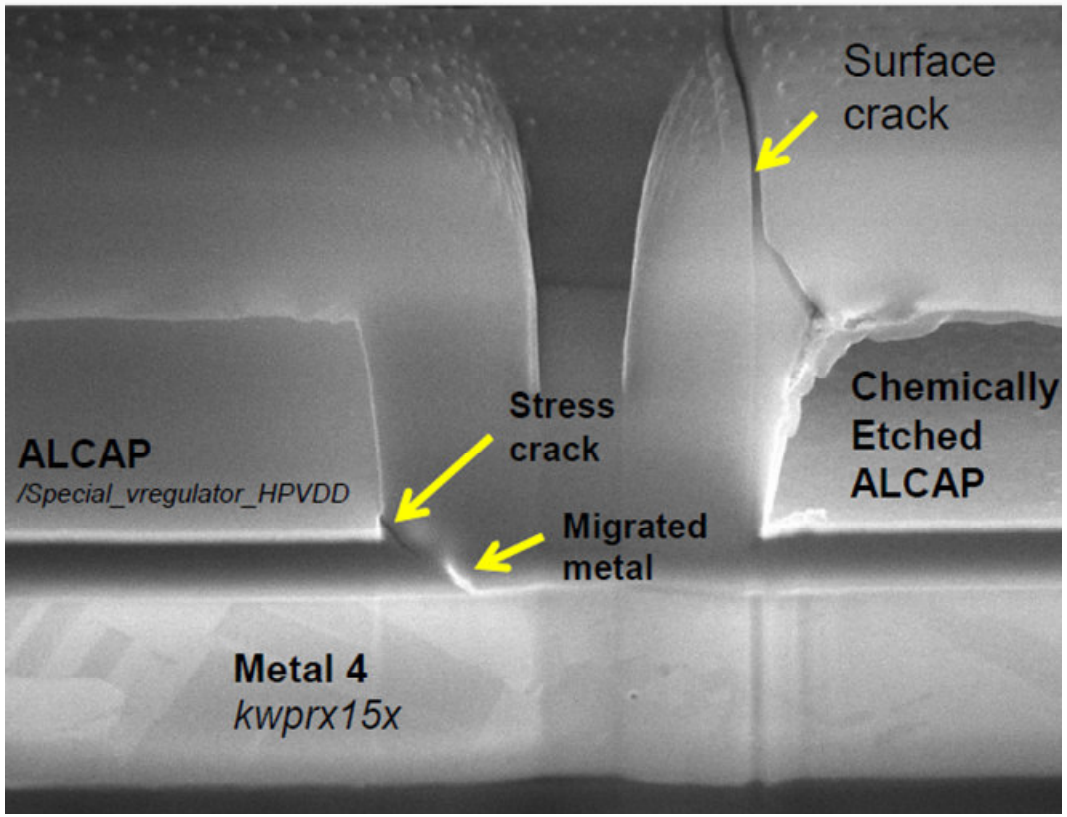


Image4: *Cross section through the failure site.*

Metal migration through the crack is visible in cross section (Image4), subsequent cross sections through this area showed the crack between Metal4 and ALCAP extending parallel with the surface crack.

Appendix B; ELFR Fail 8D Report

Failure Mech Summary	SEM images show metal migration through a crack directly underneath mechanically damaged passivation. Copper migrated up the crack bridging the suspected signal at metal 4 to ALCAP

D4 Summary	**Occurrence:** Mechanical surface damage can occur in the process steps following passivation in Wafer Fab through to mould encapsulation at Assembly. Each area was contacted to review the failure and provide potential causes for the failure mode seen. Fab: Passivation module checked for qualification lot including lots prior to after manufacture, no issues with the qualification lot or lots built in the timeframe were evident. SGPC location well away from area of die and not typical damage seen in this area. FTA reviewed several areas but conclusion is that does not appear to be system issue and damage is not typical of wafer Fab/ SGPC type damage. Probe: No issues were seen on reviewing lot history, damage not consistent with probe needle or other handling in the area Assy: A simulation run by assembly on the pickup tool, with debris deliberately placed on the pickup tool, showed a different kind of damage and in a different area to that of the failing device. An FTA did not highlight any other areas of concern in Assembly. In addition, to rule out any systemic issues Die from the same location of the wafer as the failure were examined and passivation etch used to highlight any damage; no issues were identified. **Occurrence:** The escape root cause of the failure is a random defect that was not screened out by the probe, burn-in and final test programs when this lot was tested and subsequently submitted for qualification.

D5 Summary	No permanent corrective action is possible due to the inconclusive cause of the defect.

Appendix B; ELFR Fail 8D Report

D6 Summary	Although no Permanent Corrective action was identified several follow-up actions were noted; 1. 1/2400 units failed ELFR during the qualification, 2 further lots of ELFR have been performed on Pictus 256k (0/800) and Bolero 256k (0/800) without issue. **Complete** **2.** Although the failing unit sat within the population's parametric distribution, prior to stress, and could not have been identified via limits an opportunity existed to tighten the limits for Iddq and has been rolled out for Pictus 512k with others being reviewed. **Complete** 3. For each product being released to 12hr BI the Iddq test limits will be reviewed and tightened where appropriate. **As Appropriate** 4. We will perform an additional sample ELFR on Pictus (800 units total covering a minimum of 3 wafer lots). Units will come from supply plan (end of line units) and will not be shipped. **Due WW50** 5. We will perform passivation integrity etch on 30 units (covering a minimum of 3 wafer lots) **Complete:** Analysis did not show systemic issue as seen above. 6. Supplement the C90 Reliability Monitor, which already has HTOL and extended stress data, to include ELFR (45 units per month ongoing). **Complete:** Added to Rap and will be collected over the next 12 months

Appendix B; ELFR Fail 8D Report

D7 Summary

Current data suggest that this type of failure mode has a very low ppb (0.8) rate however this failure mode will be monitored through field data and current qualifications.

Stress	Read Point	Qty of Devices	Qty of Rejects	% Rejects
ELFR @ 125℃	48hrs	4036	0	0.00
HTOL @ 125℃	168hrs	1481	0	0.00
HTOL @ 125℃	504hrs	1327	0	0.00
HTOL @ 125℃	1008hrs	1324	0	0.00
HTOL @ 125℃	2016hrs	395	0	0.00
HTOL @ 125℃	3024hrs	238	0	0.00
HTOL @ 125℃	4032hrs	238	0	0.00
HTOL @ 125℃	5040hrs	78	0	0.00

***Table1**; Existing 24hrs BI data*

Stress	Read Point	Qty of Devices	Qty of Rejects	% Rejects
ELFR @ 125℃	48hrs	4000	1	0.025
HTOL @ 125℃	168hrs	521	0	0.00
HTOL @ 125℃	504hrs	521	0	0.00
HTOL @ 125℃	1008hrs	521	0	0.00
HTOL @ 125℃	2016hrs	77	0	0.00
HTOL @ 125℃	3024hrs	77	0	0.00
HTOL @ 125℃	4032hrs	0	0	0.00
HTOL @ 125℃	5040hrs	0	0	0.00

***Table2**; Existing 12hrs BI data*

Appendix C; Electrical Distributions Detail

Electrical Distribution Results Summary

Module Level Summary	
Consumption	All Tests show Cpk > 1.67 and Mean drift < 10% with exception of IDDSTDBY2 at 150C, which shows Mean drifts of -11.12% (i.e. Idd appears to increase with stress) across all 3 lots. Optimised settling time which has subsequently been introduced would have nullified apparent site issues.
Oscillator	All Tests showing Cpk > 1.67 and MEAN DRIFT < 10%
PLL	All Tests showing Cpk > 1.67 and MEAN DRIFT < 10%
I/O	All Tests showing Cpk > 1.67 and MEAN DRIFT < 10% or SPEC DRIFT < 5% where applicable.
LVD	**VLVDLVCORL**: Cpk showing < 1.67 at 150C on one lot and MEAN DRIFT < 10% on all tests.
Voltage Regulator	All Tests showing Cpk > 1.67 and MEAN DRIFT < 10%

Conclusions	
Drift Performance:	Drift performance generally robust across all parameters. Exceptions with Mean drift > 10% are:- **(1) IDDSTDBY2 at 150C**, driven by test instability at 150C, related to settling time site issues.
Cpk Performance:	Cpk's performance generally robust across all parameters. Exceptions with Cpk < 1.67 are: **(1) VLVDLVCORL**: At T1008 Hrs, 150C one lot is showing a Cpk of 1.57; test is drifting ~4mV upward through 1008Hrs of HTOL. Further optimisation of LVD programming/measurement algorithm has been implemented in subsequent test programs.

Appendix C; Electrical Distributions Detail

Current Consumption Data (Page 1 of 2)

Unit	Temp	Symbol	Test Name	Domain	Lot	Spec LSL	Spec USL	Mean (T0)	Min (T0)	Max (T0)	Std Dev (T0)	Cpk (T0)	Mean (T1008)	Min (T1008)	Max (T1008)	Std Dev (T1008)	Cpk (T1008)	MEAN DRIFT
mA	-40	IDDHALT	Halt_16MHz_HV	HV	DD75959		15	1.486	1.443	1.526	0.015	34.38	1.48	1.443	1.507	0.013	39.82	0.4
mA	25	IDDHALT	Halt_16MHz_HV	HV	DD75959		15	1.441	1.403	1.475	0.013	39.75	1.435	1.405	1.461	0.011	47.84	0.41
mA	150	IDDHALT	Halt_16MHz_HV	HV	DD75959		25	1.482	1.449	1.51	0.012	42.56	1.491	1.455	1.527	0.014	36.34	-0.61
mA	-40	IDDHALT	Halt_16MHz_HV	HV	DD76242		3	1.496	1.453	1.546	0.016	31.14	1.492	1.451	1.535	0.015	32.97	0.24
mA	25	IDDHALT	Halt_16MHz_HV	HV	DD76242		3	1.447	1.403	1.482	0.014	36.8	1.443	1.406	1.492	0.014	36.54	0.27
mA	150	IDDHALT	Halt_16MHz_HV	HV	DD76242		3	1.487	1.442	1.547	0.017	29.67	1.494	1.443	1.548	0.018	27.89	-0.43
mA	-40	IDDHALT	Halt_16MHz_HV	HV	DD76512		15	1.516	1.472	1.56	0.02	24.17	1.512	1.477	1.554	0.02	24.9	0.28
mA	25	IDDHALT	Halt_16MHz_HV	HV	DD76512		15	1.465	1.423	1.508	0.019	27.21	1.459	1.42	1.5	0.019	26.9	0.4
mA	150	IDDHALT	Halt_16MHz_HV	HV	DD76512		25	1.517	1.476	1.56	0.024	20.98	1.523	1.479	1.57	0.025	20	-0.43
mA	-40	IDDHALT	Halt_16MHz_BV	LV	DD75959		3	12.71	12.363	12.905	0.106	7.17	12.722	12.387	12.906	0.107	7.08	-0.09
mA	25	IDDHALT	Halt_16MHz_BV	LV	DD75959		3	12.896	12.551	13.083	0.104	6.71	12.888	12.522	13.066	0.105	6.71	0.06
mA	150	IDDHALT	Halt_16MHz_BV	LV	DD75959		3	16.446	15.609	17.161	0.332	8.6	16.637	15.777	17.51	0.365	7.65	-1.16
mA	-40	IDDHALT	Halt_16MHz_BV	LV	DD76242		15	12.554	12.232	12.809	0.121	6.72	12.567	12.26	12.828	0.124	6.52	-0.1
mA	25	IDDHALT	Halt_16MHz_BV	LV	DD76242		15	12.748	12.459	13.043	0.125	6.02	12.733	12.456	13.027	0.125	6.05	0.12
mA	150	IDDHALT	Halt_16MHz_BV	LV	DD76242		25	16.06	15.201	17.219	0.408	7.3	16.185	15.018	17.277	0.432	6.81	-0.78
mA	-40	IDDHALT	Halt_16MHz_BV	LV	DD76512		3	12.742	12.261	12.999	0.136	5.52	12.751	12.271	13.001	0.132	5.67	-0.07
mA	25	IDDHALT	Halt_16MHz_BV	LV	DD76512		3	12.928	12.444	13.203	0.131	5.26	12.918	12.438	13.177	0.13	5.33	0.07
mA	150	IDDHALT	Halt_16MHz_BV	LV	DD76512		3	16.725	15.72	17.906	0.4	6.9	16.807	15.782	17.701	0.415	6.59	-0.49
mA	-40	IDDRUN	Run_64MHz_5V5_max	HV	DD75959		90	10.133	9.808	10.368	0.109	121.77	10.092	9.63	10.31	0.117	113.88	0.41
mA	25	IDDRUN	Run_64MHz_5V5_max	HV	DD75959		90	9.846	9.496	10.313	0.26	51.46	9.913	9.395	10.305	0.282	47.45	-0.69
mA	150	IDDRUN	Run_64MHz_5V5_max	HV	DD75959		90	8.985	8.868	9.188	0.066	208.14	8.995	8.859	9.118	0.062	221.75	-0.11
mA	-40	IDDRUN	Run_64MHz_5V5_max	HV	DD76242		90	10.161	9.648	10.382	0.138	95.95	10.141	9.649	10.404	0.142	93.61	0.19
mA	25	IDDRUN	Run_64MHz_5V5_max	HV	DD76242		90	9.78	9.387	10.838	0.286	46.86	9.816	9.347	10.246	0.272	49.24	-0.38
mA	150	IDDRUN	Run_64MHz_5V5_max	HV	DD76242		90	9.02	8.843	9.15	0.074	184.63	9.016	8.785	9.237	0.082	167.2	0.04
mA	-40	IDDRUN	Run_64MHz_5V5_max	HV	DD76512		90	10.265	9.765	10.633	0.162	81.85	10.227	9.69	10.612	0.179	74.09	0.37
mA	25	IDDRUN	Run_64MHz_5V5_max	HV	DD76512		90	9.662	9.369	10.321	0.243	55.33	9.637	9.211	10.148	0.257	52.38	0.25
mA	150	IDDRUN	Run_64MHz_5V5_max	HV	DD76512		90	9.092	8.913	9.283	0.081	167.54	9.087	8.916	9.256	0.07	194.26	0.05
mA	-40	IDDRUN	Run_64MHz_5V5_max	LV	DD75959		50	63.453	61.445	64.546	0.678	13.05	63.509	61.559	64.648	0.678	13.02	-0.09
mA	25	IDDRUN	Run_64MHz_5V5_max	LV	DD75959		50	63.989	61.993	65.021	0.632	13.72	63.993	61.992	64.996	0.63	13.77	-0.01
mA	150	IDDRUN	Run_64MHz_5V5_max	LV	DD75959		50	68.028	66.158	69.365	0.724	10.12	68.192	66.248	69.678	0.774	9.39	-0.24
mA	-40	IDDRUN	Run_64MHz_5V5_max	LV	DD76242		50	62.745	60.704	64.296	0.773	11.75	62.825	60.778	64.429	0.775	11.7	-0.13
mA	25	IDDRUN	Run_64MHz_5V5_max	LV	DD76242		50	63.34	61.258	64.893	0.74	12	63.325	61.242	64.837	0.738	12.05	0.02
mA	150	IDDRUN	Run_64MHz_5V5_max	LV	DD76242		50	67.151	64.38	68.838	0.87	8.75	67.247	64.145	68.983	0.912	8.32	-0.14
mA	-40	IDDRUN	Run_64MHz_5V5_max	LV	DD76512		50	63.654	61.217	64.975	0.719	12.21	63.7	61.337	65.103	0.703	12.47	-0.07
mA	25	IDDRUN	Run_64MHz_5V5_max	LV	DD76512		50	64.215	61.887	65.483	0.677	12.7	64.209	61.89	65.499	0.681	12.62	0.01
mA	150	IDDRUN	Run_64MHz_5V5_max	LV	DD76512		50	68.595	65.765	70.195	0.803	8.89	68.633	65.864	70.161	0.847	8.41	-0.06

Appendix C; Electrical Distributions Detail

Current Consumption Data (Page 2 or 2)

Test Name	Domain	Lot	Spec LSL	Spec USL	Mean (T0)	Min (T0)	Max (T0)	Std Dev (T0)	Cpk (T0)	Mean (T1008)	Min (T1008)	Max (T1008)	Std Dev (T1008)	Cpk (T1008)	MEAN DRIFT
Standby2_VDD_BV	LV	DD75959		80	17.934	10.918	20.893	1.847	11.2	16.659	11.853	20.017	1.556	13.57	7.11
Standby2_VDD_BV	LV	DD75959		80	9.774	8.71	11.192	0.525	44.62	10.435	8.744	11.338	0.481	48.18	-6.76
Standby2_VDD_HV	LV	DD75959		20	270.21	229.022	304.504	16.835	22.37	285.017	238.01	324.686	20.497	18.13	-5.48
Standby2_VDD_BV	HV	DD75959		80	7.607	5.643	9.329	1.222	3.38	7.269	6.229	8.456	0.516	8.23	4.44
Standby2_VDD_HV	HV	DD75959		20	8.382	6.739	9.727	1.035	3.74	8.232	6.544	10.396	0.902	4.35	1.79
Standby2_VDD_HV	HV	DD75959		20	57.176	50.835	65.144	3.767	21.48	63.533	51.345	71.812	5.432	14.51	-11.12
Standby2_VDD_BV	LV	DD76242		80	14.232	10.411	18.872	1.52	14.42	13.922	10.564	18.933	1.386	15.89	2.18
Standby2_VDD_BV	LV	DD76242		80	11.203	9.86	12.721	0.67	34.22	11.497	10.292	13.371	0.67	34.06	-2.62
Standby2_VDD_HV	LV	DD76242		20	261.666	214.527	328.407	22.213	17.08	270.97	199.375	335.662	24.343	15.46	-3.56
Standby2_VDD_BV	HV	DD76242		80	7.642	5.791	9.643	1.173	3.51	7.363	5.787	8.398	0.578	7.29	3.65
Standby2_VDD_HV	HV	DD76242		20	8.035	6.44	9.638	0.845	4.72	8.135	6.529	10.119	0.909	4.35	-1.25
Standby2_VDD_HV	HV	DD76242		20	59.643	49.557	72.507	4.312	18.58	65.103	46.712	74.156	5.398	14.51	-9.15
Standby2_VDD_BV	LV	DD76512		1400	17.181	9.37	20.374	1.858	11.27	15.699	9.731	19.504	1.693	12.66	8.62
Standby2_VDD_BV	LV	DD76512		1400	9.778	8.615	11.475	0.564	41.53	10	8.911	11.501	0.51	45.76	-2.28
Standby2_VDD_HV	LV	DD76512		300	251.429	204.122	293.327	17.579	21.78	256.016	206.318	304.996	22.179	17.19	-1.82
Standby2_VDD_BV	HV	DD76512		1400	7.692	5.901	9.58	1.169	3.51	7.292	6.256	8.532	0.578	7.33	5.2
Standby2_VDD_HV	HV	DD76512		300	8.574	6.598	10.783	1.08	3.53	8.513	6.621	10.579	0.941	4.07	0.71
Standby2_VDD_HV	HV	DD76512		300	68.843	55.956	84.535	6.424	12	73.243	49.571	92.561	8.294	9.11	-6.39
Stop_BV_5V5_max	HV	DD75959		200	10.724	8.877	12.4	0.921	68.52	10.654	9.536	11.598	0.548	115.19	0.65
Stop_HV_5V5_max	HV	DD75959		200	11.487	10.352	12.595	0.692	90.76	11.148	9.331	12.648	0.88	71.55	2.96
Stop_HV_5V5_max	HV	DD75959		2000	45.444	40.309	51.553	2.709	240.52	49.344	41.1	54.4	3.795	171.36	-8.58
Stop_BV_5V5_max	LV	DD75959		700	65.309	56.041	75.685	3.542	59.73	67.656	48.191	75.618	3.995	52.76	-3.59
Stop_BV_5V5_max	LV	DD75959		700	93.371	84.04	104.678	3.896	51.9	97.928	87.347	108.756	4.097	48.98	-4.88
Stop_HV_5V5_max	LV	DD75959		12000	3264.625	2613.22	3880.07	283.519	10.27	3466.862	2757.81	4280.1	322.754	8.81	-6.19
Stop_BV_5V5_max	HV	DD76242		200	10.688	9.398	12.147	0.895	70.47	10.774	9.631	11.743	0.552	114.34	-0.81
Stop_HV_5V5_max	HV	DD76242		200	10.986	9.887	11.976	0.641	98.32	10.995	9.069	12.438	0.801	78.7	-0.09
Stop_HV_5V5_max	HV	DD76242		2000	46.521	38.661	57.363	3.572	182.28	50.911	36.965	59.541	4.395	147.83	-9.44
Stop_BV_5V5_max	LV	DD76242		700	81.322	69.089	113.606	7.741	26.64	84.734	73.547	116.203	7.921	25.89	-4.2
Stop_BV_5V5_max	LV	DD76242		700	110.07	97.195	150.923	9.782	20.1	113.832	100.244	155.605	10.187	19.18	-3.42
Stop_HV_5V5_max	LV	DD76242		12000	3043.008	2401.53	4227.2	344.316	8.67	3176.242	2316.66	4251.42	361.524	8.14	-4.38
Stop_BV_5V5_max	HV	DD76512		200	10.703	9.363	12.241	0.879	71.76	10.495	9.145	11.999	0.697	90.6	1.95
Stop_HV_5V5_max	HV	DD76512		200	11.349	9.445	12.606	0.788	79.82	11.171	9.297	12.903	0.927	67.92	1.57
Stop_HV_5V5_max	HV	DD76512		2000	54.122	44.063	67.23	5.25	123.55	57.838	40.041	72.211	6.616	97.85	-6.87
Stop_BV_5V5_max	LV	DD76512		700	64.093	39.581	100.829	6.686	31.71	67.049	60.283	103.273	6.258	33.71	-4.61
Stop_BV_5V5_max	LV	DD76512		700	93.992	79.632	125.872	6.983	28.93	97.821	83.672	129.15	7.074	28.38	-4.07
Stop_HV_5V5_max	LV	DD76512		12000	3484.032	2912.88	4582.84	350.806	8.09	3581.133	2850.6	4457.72	357.929	7.84	-2.79

Appendix C; Electrical Distributions Detail

Voltage Data

Unit	Temp	Symbol	Test Name	Lot	Spec LSL	Spec USL	Mean (T0)	Min (T0)	Max (T0)	Std Dev (T0)	Cpk (T0)	Mean (T1008)	Min (T1008)	Max (T1008)	Std Dev (T1008)	Cpk (T1008)	MEAN DRIFT
V	-40	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD75959	1.15	1.32	1.212	1.202	1.224	0.006	3.47	1.216	1.207	1.226	0.005	4.36	-0.32
V	25	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD75959	1.15	1.32	1.209	1.204	1.215	0.003	6.34	1.219	1.21	1.232	0.006	3.78	-0.78
V	150	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD75959	1.15	1.32	1.193	1.182	1.199	0.003	4.3	1.207	1.196	1.219	0.008	2.52	-1.23
V	-40	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD76242	1.15	1.32	1.212	1.202	1.224	0.005	3.91	1.217	1.206	1.227	0.005	4.09	-0.38
V	25	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD76242	1.15	1.32	1.214	1.202	1.225	0.006	3.54	1.219	1.207	1.234	0.006	3.62	-0.48
V	150	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD76242	1.15	1.32	1.193	1.185	1.201	0.003	4.12	1.208	1.192	1.219	0.008	2.31	-1.27
V	-40	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD76512	1.15	1.32	1.212	1.2	1.223	0.006	3.7	1.218	1.208	1.229	0.005	4.47	-0.51
V	25	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD76512	1.15	1.32	1.213	1.202	1.225	0.006	3.74	1.22	1.209	1.232	0.005	4.27	-0.55
V	150	VLPREG	LP_Reg_T0_PostTrim_15mA_5V	DD76512	1.15	1.32	1.193	1.182	1.203	0.004	3.93	1.207	1.191	1.222	0.008	2.41	-1.25
V	-40	VMREG	Main_Reg_160mA_Load_5V	DD75959	1.15	1.32	1.213	1.199	1.235	0.01	2.12	1.213	1.199	1.233	0.01	2.05	0.01
V	25	VMREG	Main_Reg_160mA_Load_5V	DD75959	1.15	1.32	1.204	1.2	1.208	0.003	6.88	1.204	1.199	1.208	0.003	6.9	0.03
V	150	VMREG	Main_Reg_160mA_Load_5V	DD75959	1.15	1.32	1.185	1.177	1.192	0.004	3.19	1.183	1.175	1.191	0.004	2.8	0.15
V	-40	VMREG	Main_Reg_160mA_Load_5V	DD76242	1.15	1.32	1.213	1.198	1.232	0.011	1.98	1.214	1.199	1.231	0.011	1.9	-0.1
V	25	VMREG	Main_Reg_160mA_Load_5V	DD76242	1.15	1.32	1.215	1.2	1.235	0.013	1.69	1.208	1.199	1.237	0.009	2.08	0.55
V	150	VMREG	Main_Reg_160mA_Load_5V	DD76242	1.15	1.32	1.186	1.177	1.194	0.004	3.39	1.186	1.178	1.193	0.004	3.42	-0.02
V	-40	VMREG	Main_Reg_160mA_Load_5V	DD76512	1.15	1.32	1.212	1.201	1.234	0.01	2.09	1.217	1.201	1.234	0.011	2.02	-0.34
V	25	VMREG	Main_Reg_160mA_Load_5V	DD76512	1.15	1.32	1.213	1.2	1.233	0.012	1.81	1.204	1.2	1.209	0.003	6.96	0.67
V	150	VMREG	Main_Reg_160mA_Load_5V	DD76512	1.15	1.32	1.187	1.181	1.193	0.003	3.74	1.186	1.181	1.192	0.003	3.88	0.1
V	-40	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD75959	1.15	1.32	1.222	1.215	1.231	0.004	6.07	1.225	1.217	1.232	0.004	7.03	-0.22
V	25	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD75959	1.15	1.32	1.225	1.22	1.23	0.003	8.46	1.231	1.224	1.239	0.004	7.46	-0.5
V	150	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD75959	1.15	1.32	1.213	1.204	1.22	0.003	6.86	1.222	1.216	1.229	0.004	6.53	-0.74
V	-40	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD76242	1.15	1.32	1.223	1.215	1.231	0.003	6.99	1.226	1.218	1.234	0.004	6.47	-0.26
V	25	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD76242	1.15	1.32	1.227	1.218	1.234	0.004	7.3	1.231	1.223	1.24	0.004	7.23	-0.37
V	150	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD76242	1.15	1.32	1.214	1.206	1.221	0.003	6.46	1.223	1.213	1.23	0.004	5.64	-0.75
V	-40	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD76512	1.15	1.32	1.222	1.213	1.229	0.004	6.59	1.226	1.219	1.234	0.003	7.66	-0.32
V	25	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD76512	1.15	1.32	1.226	1.219	1.233	0.003	7.76	1.231	1.225	1.238	0.003	8.72	-0.43
V	150	VULPREG	ULP_Reg_T0_PostTrim_5mA_5V	DD76512	1.15	1.32	1.213	1.204	1.222	0.003	6.13	1.222	1.212	1.232	0.004	5.92	-0.77

Appendix C; Electrical Distributions Detail

LVD Data

Unit	Temp	Symbol	Test Name	Lot	Spec LSL	Spec USL	Mean (T0)	Min (T0)	Max (T0)	Std Dev (T0)	Cpk (T0)	Mean (T1008)	Min (T1008)	Max (T1008)	Std Dev (T1008)	Cpk (T1008)	MEAN DRIFT
V	-40	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD75959	1.08	1.14	1.102	1.096	1.109	0.003	2.16	1.098	1.091	1.108	0.004	1.66	0.38
V	25	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD75959	1.08	1.14	1.111	1.104	1.117	0.003	3.08	1.109	1.1	1.116	0.003	2.9	0.19
V	150	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD75959	1.08	1.14	1.117	1.109	1.126	0.004	2	1.121	1.113	1.13	0.004	1.57	-0.42
V	-40	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD76242	1.08	1.14	1.103	1.095	1.112	0.003	2.22	1.099	1.091	1.107	0.004	1.79	0.33
V	25	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD76242	1.08	1.14	1.11	1.106	1.116	0.003	3.36	1.109	1.103	1.114	0.003	3.41	0.11
V	150	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD76242	1.08	1.14	1.115	1.107	1.125	0.004	2.2	1.12	1.111	1.13	0.004	1.72	-0.41
V	-40	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD76512	1.08	1.14	1.102	1.093	1.108	0.003	2.18	1.097	1.089	1.105	0.003	1.71	0.41
V	25	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD76512	1.08	1.14	1.11	1.102	1.117	0.003	3.11	1.108	1.101	1.116	0.003	3	0.12
V	150	VLVDLVCORL	LV_LVD_D_FLASH_3V3	DD76512	1.08	1.14	1.116	1.107	1.125	0.004	2.27	1.121	1.112	1.13	0.004	1.7	-0.46

IO Data

- All Tests showing Cpk > 1.67 and MEAN DRIFT < 10% or SPEC DRIFT < 5% where applicable.
- Data available on request (runs to >200 pages)

Appendix C; Electrical Distributions Detail

Oscillator Data (Page 1 of 2)

Unit	Temp	Symbol	Test Name	Lot	Spec LSL	Spec USL	Mean (T0)	Min (T0)	Max (T0)	Std Dev (T0)	Cpk (T0)	Mean (T1008)	Min (T1008)	Max (T1008)	Std Dev (T1008)	Cpk (T1008)	MEAN DRIFT
mA/V	-40	gmFXOSC	lxtl_12_3V3_SM0	DD75959	2.2	8.2	4.79	4.279	6.671	0.265	3.26	4.785	4.346	6.606	0.255	3.38	0.1
mA/V	25	gmFXOSC	lxtl_12_3V3_SM0	DD75959	2.2	8.2	5.033	4.658	6.417	0.201	4.69	5.03	4.651	6.32	0.192	4.91	0.07
mA/V	150	gmFXOSC	lxtl_12_3V3_SM0	DD75959	2.2	8.2	5.07	4.839	5.882	0.119	8.02	5.057	4.862	5.779	0.109	8.77	0.27
mA/V	-40	gmFXOSC	lxtl_12_3V3_SM0	DD76242	2.2	8.2	5.069	4.524	6.792	0.549	1.74	5.062	4.499	6.723	0.531	1.8	0.14
mA/V	25	gmFXOSC	lxtl_12_3V3_SM0	DD76242	2.2	8.2	5.243	4.846	6.49	0.403	2.45	5.24	4.836	6.477	0.399	2.47	0.05
mA/V	150	gmFXOSC	lxtl_12_3V3_SM0	DD76242	2.2	8.2	5.193	4.924	5.923	0.235	4.24	5.175	4.878	5.915	0.229	4.32	0.35
mA/V	-40	gmFXOSC	lxtl_12_3V3_SM0	DD76512	2.2	8.2	4.943	4.553	5.885	0.245	3.72	4.939	4.513	5.868	0.246	3.72	0.08
mA/V	25	gmFXOSC	lxtl_12_3V3_SM0	DD76512	2.2	8.2	5.172	4.832	5.853	0.185	5.35	5.168	4.804	5.853	0.188	5.27	0.08
mA/V	150	gmFXOSC	lxtl_12_3V3_SM0	DD76512	2.2	8.2	5.18	4.917	5.558	0.119	8.32	5.17	4.9	5.528	0.12	8.25	0.19
mA/V	-40	gmFXOSC	lxtl_12_3V3_SM1	DD75959	2.7	9.7	5.722	5.122	7.937	0.313	3.22	5.711	5.172	7.856	0.303	3.32	0.19
mA/V	25	gmFXOSC	lxtl_12_3V3_SM1	DD75959	2.7	9.7	6.003	5.562	7.627	0.236	4.66	5.996	5.57	7.51	0.225	4.88	0.12
mA/V	150	gmFXOSC	lxtl_12_3V3_SM1	DD75959	2.7	9.7	6.038	5.791	7.001	0.141	7.91	6.019	5.78	6.86	0.128	8.64	0.32
mA/V	-40	gmFXOSC	lxtl_12_3V3_SM1	DD76242	2.7	9.7	6.053	5.409	8.091	0.651	1.72	6.04	5.37	8.017	0.633	1.76	0.21
mA/V	25	gmFXOSC	lxtl_12_3V3_SM1	DD76242	2.7	9.7	6.251	5.794	7.726	0.478	2.4	6.241	5.761	7.693	0.472	2.44	0.17
mA/V	150	gmFXOSC	lxtl_12_3V3_SM1	DD76242	2.7	9.7	6.182	5.837	7.051	0.28	4.15	6.161	5.81	7.017	0.272	4.24	0.34
mA/V	-40	gmFXOSC	lxtl_12_3V3_SM1	DD76512	2.7	9.7	5.902	5.433	7.024	0.289	3.69	5.895	5.374	6.988	0.29	3.67	0.12
mA/V	25	gmFXOSC	lxtl_12_3V3_SM1	DD76512	2.7	9.7	6.164	5.749	6.967	0.221	5.22	6.159	5.727	6.99	0.226	5.11	0.07
mA/V	150	gmFXOSC	lxtl_12_3V3_SM1	DD76512	2.7	9.7	6.169	5.845	6.606	0.141	8.2	6.154	5.836	6.568	0.141	8.18	0.24
mA/V	-40	gmFXOSC	lxtl_12_5V_SM0	DD75959	2	7.4	4.622	4.189	6.255	0.229	3.81	4.606	4.208	6.215	0.226	3.85	0.35
mA/V	25	gmFXOSC	lxtl_12_5V_SM0	DD75959	2	7.4	4.784	4.458	5.977	0.174	5.02	4.774	4.454	5.902	0.168	5.2	0.22
mA/V	150	gmFXOSC	lxtl_12_5V_SM0	DD75959	2	7.4	4.766	4.573	5.464	0.103	8.51	4.743	4.556	5.389	0.097	9.09	0.48
mA/V	-40	gmFXOSC	lxtl_12_5V_SM0	DD76242	2	7.4	4.865	4.383	6.381	0.482	1.75	4.843	4.349	6.298	0.469	1.82	0.45
mA/V	25	gmFXOSC	lxtl_12_5V_SM0	DD76242	2	7.4	4.967	4.627	6.038	0.353	2.3	4.953	4.583	6.023	0.35	2.33	0.29
mA/V	150	gmFXOSC	lxtl_12_5V_SM0	DD76242	2	7.4	4.872	4.618	5.526	0.206	4.09	4.848	4.591	5.504	0.204	4.16	0.49
mA/V	-40	gmFXOSC	lxtl_12_5V_SM0	DD76512	2	7.4	4.749	4.4	5.616	0.22	4.01	4.733	4.377	5.579	0.218	4.08	0.34
mA/V	25	gmFXOSC	lxtl_12_5V_SM0	DD76512	2	7.4	4.901	4.599	5.529	0.169	4.94	4.891	4.583	5.535	0.17	4.91	0.2
mA/V	150	gmFXOSC	lxtl_12_5V_SM0	DD76512	2	7.4	4.859	4.625	5.218	0.11	7.7	4.841	4.602	5.187	0.111	7.69	0.37
mA/V	-40	gmFXOSC	lxtl_12_5V_SM1	DD75959	2.5	9.2	5.677	5.148	7.676	0.282	3.76	5.654	5.152	7.618	0.276	3.81	0.41
mA/V	25	gmFXOSC	lxtl_12_5V_SM1	DD75959	2.5	9.2	5.872	5.484	7.329	0.212	5.24	5.854	5.467	7.227	0.205	5.44	0.32
mA/V	150	gmFXOSC	lxtl_12_5V_SM1	DD75959	2.5	9.2	5.841	5.612	6.695	0.128	8.72	5.814	5.599	6.571	0.116	9.53	0.46
mA/V	-40	gmFXOSC	lxtl_12_5V_SM1	DD76242	2.5	9.2	5.973	5.395	7.822	0.587	1.83	5.945	5.35	7.717	0.572	1.9	0.47
mA/V	25	gmFXOSC	lxtl_12_5V_SM1	DD76242	2.5	9.2	6.093	5.678	7.422	0.43	2.41	6.073	5.634	7.384	0.427	2.44	0.32
mA/V	150	gmFXOSC	lxtl_12_5V_SM1	DD76242	2.5	9.2	5.971	5.67	6.754	0.25	4.3	5.94	5.625	6.747	0.248	4.38	0.53
mA/V	-40	gmFXOSC	lxtl_12_5V_SM1	DD76512	2.5	9.2	5.833	5.415	6.879	0.268	4.14	5.814	5.381	6.853	0.266	4.16	0.33
mA/V	25	gmFXOSC	lxtl_12_5V_SM1	DD76512	2.5	9.2	6.014	5.64	6.783	0.205	5.18	5.995	5.615	6.787	0.207	5.17	0.32
mA/V	150	gmFXOSC	lxtl_12_5V_SM1	DD76512	2.5	9.2	5.954	5.678	6.38	0.133	8.12	5.928	5.637	6.333	0.134	8.12	0.44

Appendix C; Electrical Distributions Detail

Oscillator Data (Page 2 of 2)

Unit	Temp	Symbol	Test Name	Lot	Spec LSL	Spec USL	Mean (T0)	Min (T0)	Max (T0)	Std Dev (T0)	Cpk (T0)	Mean (T1008)	Min (T1008)	Max (T1008)	Std Dev (T1008)	Cpk (T1008)	MEAN DRIFT
kHz	-40	fSIRCVAR	LS_Osc_Flash	DD75959	115.2	140.8	127.634	124.762	130.238	1.215	3.41	127.426	124.762	130	1.207	3.38	0.16
kHz	25	fSIRCVAR	LS_Osc_Flash	DD75959	115.2	140.8	127.426	125.714	129.286	1.059	3.85	127.127	125.238	128.81	1.045	3.8	0.23
kHz	150	fSIRCVAR	LS_Osc_Flash	DD75959	115.2	140.8	125.576	123.095	128.571	1.367	2.53	125.523	123.095	128.571	1.371	2.51	0.04
kHz	-40	fSIRCVAR	LS_Osc_Flash	DD76242	115.2	140.8	127.594	124.048	130.238	1.507	2.74	127.304	123.81	130.238	1.475	2.74	0.23
kHz	25	fSIRCVAR	LS_Osc_Flash	DD76242	115.2	140.8	127.44	125.714	129.048	1.042	3.92	127.066	125.238	129.048	1.042	3.8	0.29
kHz	150	fSIRCVAR	LS_Osc_Flash	DD76242	115.2	140.8	125.513	122.857	129.762	1.399	2.46	125.442	122.619	129.762	1.418	2.41	0.06
kHz	-40	fSIRCVAR	LS_Osc_Flash	DD76512	115.2	140.8	127.544	125	131.428	1.395	2.95	127.197	124.762	130.952	1.352	2.96	0.27
kHz	25	fSIRCVAR	LS_Osc_Flash	DD76512	115.2	140.8	127.291	125.714	129.286	1.1	3.66	126.899	125.238	128.81	1.059	3.68	0.31
kHz	150	fSIRCVAR	LS_Osc_Flash	DD76512	115.2	140.8	125.372	122.143	128.095	1.385	2.45	125.31	122.143	128.095	1.391	2.42	0.05
MHz	-40	fSIRCVAR	Main_Osc_Flash	DD75959	15.2	16.8	15.911	15.76	16.09	0.088	2.7	15.892	15.745	16.06	0.088	2.64	0.12
MHz	25	fSIRCVAR	Main_Osc_Flash	DD75959	15.2	16.8	15.995	15.86	16.155	0.084	3.14	15.975	15.845	16.13	0.085	3.05	0.12
MHz	150	fSIRCVAR	Main_Osc_Flash	DD75959	15.2	16.8	15.983	15.835	16.18	0.086	3.05	15.962	15.81	16.165	0.086	2.96	0.13
MHz	-40	fSIRCVAR	Main_Osc_Flash	DD76242	15.2	16.8	15.896	15.725	16.04	0.072	3.21	15.876	15.72	16.03	0.074	3.03	0.12
MHz	25	fSIRCVAR	Main_Osc_Flash	DD76242	15.2	16.8	16.004	15.865	16.145	0.072	3.67	15.978	15.83	16.12	0.074	3.53	0.16
MHz	150	fSIRCVAR	Main_Osc_Flash	DD76242	15.2	16.8	16.016	15.805	16.19	0.08	3.25	15.999	15.785	16.17	0.08	3.32	0.11
MHz	-40	fSIRCVAR	Main_Osc_Flash	DD76512	15.2	16.8	15.909	15.745	16.09	0.089	2.64	15.892	15.725	16.075	0.089	2.59	0.11
MHz	25	fSIRCVAR	Main_Osc_Flash	DD76512	15.2	16.8	15.999	15.86	16.155	0.085	3.12	15.983	15.84	16.145	0.086	3.02	0.1
MHz	150	fSIRCVAR	Main_Osc_Flash	DD76512	15.2	16.8	16.011	15.835	16.19	0.09	2.91	15.993	15.815	16.175	0.091	2.92	0.11
V	-40	VFOSSCOP	OscOP_Voltage_3V3	DD75959	0.75	1.15	0.981	0.96	1.055	0.014	4.01	0.978	0.955	1.05	0.014	4.08	0.3
V	25	VFOSSCOP	OscOP_Voltage_3V3	DD75959	0.75	1.15	0.927	0.909	0.993	0.013	4.53	0.926	0.907	0.993	0.013	4.51	0.14
V	150	VFOSSCOP	OscOP_Voltage_3V3	DD75959	0.7	1.15	0.838	0.821	0.894	0.012	2.52	0.838	0.821	0.895	0.012	2.53	0.02
V	-40	VFOSSCOP	OscOP_Voltage_3V3	DD76242	0.75	1.15	0.986	0.953	1.074	0.027	2.02	0.984	0.952	1.07	0.027	2.06	0.23
V	25	VFOSSCOP	OscOP_Voltage_3V3	DD76242	0.75	1.15	0.931	0.9	1.011	0.025	2.43	0.931	0.9	1.01	0.025	2.43	0.01
V	150	VFOSSCOP	OscOP_Voltage_3V3	DD76242	0.7	1.15	0.842	0.814	0.91	0.021	2.21	0.843	0.816	0.912	0.022	2.2	-0.1
V	-40	VFOSSCOP	OscOP_Voltage_3V3	DD76512	0.75	1.15	0.957	0.932	1.02	0.017	3.88	0.955	0.929	1.015	0.016	4.05	0.24
V	25	VFOSSCOP	OscOP_Voltage_3V3	DD76512	0.75	1.15	0.904	0.881	0.961	0.015	3.35	0.902	0.879	0.96	0.015	3.29	0.14
V	150	VFOSSCOP	OscOP_Voltage_3V3	DD76512	0.7	1.15	0.816	0.795	0.866	0.014	2.82	0.817	0.795	0.867	0.014	2.77	-0.05
V	-40	VFOSSCOP	OscOP_Voltage_5V	DD75959	0.75	1.15	1.003	0.982	1.076	0.014	3.5	0.999	0.975	1.07	0.014	3.58	0.32
V	25	VFOSSCOP	OscOP_Voltage_5V	DD75959	0.75	1.15	0.95	0.931	1.016	0.013	5.05	0.949	0.929	1.015	0.013	5.02	0.17
V	150	VFOSSCOP	OscOP_Voltage_5V	DD75959	0.75	1.15	0.868	0.851	0.923	0.012	3.32	0.868	0.85	0.924	0.012	3.32	0.03
V	-40	VFOSSCOP	OscOP_Voltage_5V	DD76242	0.75	1.15	1.007	0.974	1.094	0.027	1.78	1.005	0.972	1.09	0.027	1.82	0.26
V	25	VFOSSCOP	OscOP_Voltage_5V	DD76242	0.75	1.15	0.954	0.923	1.034	0.025	2.64	0.954	0.922	1.032	0.025	2.64	0.05
V	150	VFOSSCOP	OscOP_Voltage_5V	DD76242	0.75	1.15	0.872	0.844	0.941	0.021	1.89	0.872	0.845	0.942	0.022	1.88	-0.08
V	-40	VFOSSCOP	OscOP_Voltage_5V	DD76512	0.75	1.15	0.977	0.952	1.041	0.017	3.46	0.975	0.95	1.037	0.016	3.61	0.26
V	25	VFOSSCOP	OscOP_Voltage_5V	DD76512	0.75	1.15	0.926	0.903	0.985	0.015	3.81	0.924	0.901	0.983	0.016	3.73	0.18
V	150	VFOSSCOP	OscOP_Voltage_5V	DD76512	0.75	1.15	0.846	0.824	0.896	0.014	2.31	0.846	0.824	0.898	0.014	2.25	-0.01

Appendix C; Electrical Distributions Detail

PLL Data

Unit	Temp	Symbol	Test Name	Lot	Spec LSL	Spec USL	Mean (T0)	Min (T0)	Max (T0)	Std Dev (T0)	Cpk (T0)	Mean (T1008)	Min (T1008)	Max (T1008)	Std Dev (T1008)	Cpk (T1008)	MEAN DRIFT
MHz	-40	fPLLOUT	PLL_2x10MHz_Meas	DD75959	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	25	fPLLOUT	PLL_2x10MHz_Meas	DD75959	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	150	fPLLOUT	PLL_2x10MHz_Meas	DD75959	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	-40	fPLLOUT	PLL_2x10MHz_Meas	DD76242	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	25	fPLLOUT	PLL_2x10MHz_Meas	DD76242	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	150	fPLLOUT	PLL_2x10MHz_Meas	DD76242	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	-40	fPLLOUT	PLL_2x10MHz_Meas	DD76512	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	25	fPLLOUT	PLL_2x10MHz_Meas	DD76512	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	150	fPLLOUT	PLL_2x10MHz_Meas	DD76512	19.802	20.2	20	20	20	0		20	20	20	0		0
MHz	-40	fPLLOUT	PLL_4x10MHz_Meas	DD75959	39.526	40.32	40	40	40	0		40	40	40	0		0
MHz	25	fPLLOUT	PLL_4x10MHz_Meas	DD75959	39.526	40.32	40	40	40	0		40	40	40	0		0
MHz	150	fPLLOUT	PLL_4x10MHz_Meas	DD75959	39.526	40.32	40	40	40	0		40	40	40	0		0
MHz	-40	fPLLOUT	PLL_4x10MHz_Meas	DD76242	39.526	40.32	40	40	40	0		40	40	40	0		0
MHz	25	fPLLOUT	PLL_4x10MHz_Meas	DD76242	39.526	40.32	40	40	40	0		40	40	40	0		0
MHz	150	fPLLOUT	PLL_4x10MHz_Meas	DD76242	39.526	40.32	40	40	40	0		40	40	40.01	0.001	94.29	0
MHz	-40	fPLLOUT	PLL_4x10MHz_Meas	DD76512	39.526	40.32	40	40	40	0		40	40	40	0		0
MHz	25	fPLLOUT	PLL_4x10MHz_Meas	DD76512	39.526	40.32	40	40	40	0		40	40	40	0		0
MHz	150	fPLLOUT	PLL_4x10MHz_Meas	DD76512	39.526	40.32	40	40	40	0		40	40	40.01	0.001	96.11	0
MHz	-40	fFREE	PLL_ODF16xFree_Meas	DD75959	1.563	7.813	3.153	2.62	3.69	0.23	2.3	3.186	2.68	3.75	0.231	2.34	-1.06
MHz	25	fFREE	PLL_ODF16xFree_Meas	DD75959	1.563	7.813	3.938	3.46	4.46	0.212	3.74	3.948	3.48	4.46	0.211	3.77	-0.24
MHz	150	fFREE	PLL_ODF16xFree_Meas	DD75959	1.563	7.813	5.855	5.41	6.41	0.218	3	5.91	5.44	6.45	0.224	2.83	-0.95
MHz	-40	fFREE	PLL_ODF16xFree_Meas	DD76242	1.563	7.813	3.191	2.68	3.79	0.21	2.58	3.205	2.69	3.8	0.211	2.59	-0.42
MHz	25	fFREE	PLL_ODF16xFree_Meas	DD76242	1.563	7.813	3.996	3.53	4.52	0.196	4.14	3.977	3.51	4.51	0.196	4.1	0.49
MHz	150	fFREE	PLL_ODF16xFree_Meas	DD76242	1.563	7.813	5.909	5.49	6.37	0.187	3.4	5.953	5.55	6.41	0.187	3.32	-0.75
MHz	-40	fFREE	PLL_ODF16xFree_Meas	DD76512	1.563	7.813	3.09	2.55	3.73	0.21	2.42	3.097	2.51	3.72	0.216	2.37	-0.21
MHz	25	fFREE	PLL_ODF16xFree_Meas	DD76512	1.563	7.813	3.882	3.38	4.46	0.209	3.7	3.874	3.38	4.45	0.208	3.69	0.2
MHz	150	fFREE	PLL_ODF16xFree_Meas	DD76512	1.563	7.813	5.814	5.33	6.38	0.231	2.88	5.848	5.36	6.41	0.23	2.85	-0.59
MHz	-40	fFREE	PLL_ODF8xFree_Meas	DD75959	3.125	15.625	6.308	5.25	7.36	0.46	2.3	6.373	5.37	7.49	0.461	2.35	-1.04
MHz	25	fFREE	PLL_ODF8xFree_Meas	DD75959	3.125	15.625	7.88	6.93	8.93	0.423	3.74	7.895	6.96	8.92	0.421	3.78	-0.19
MHz	150	fFREE	PLL_ODF8xFree_Meas	DD75959	3.125	15.625	11.708	10.81	12.82	0.436	2.99	11.82	10.87	12.9	0.447	2.84	-0.96
MHz	-40	fFREE	PLL_ODF8xFree_Meas	DD76242	3.125	15.625	6.382	5.36	7.57	0.42	2.58	6.407	5.38	7.6	0.421	2.6	-0.39
MHz	25	fFREE	PLL_ODF8xFree_Meas	DD76242	3.125	15.625	7.993	7.05	9.04	0.393	4.13	7.952	7.01	9.02	0.392	4.11	0.51
MHz	150	fFREE	PLL_ODF8xFree_Meas	DD76242	3.125	15.625	11.817	10.97	12.74	0.375	3.38	11.905	11.1	12.83	0.374	3.32	-0.75
MHz	-40	fFREE	PLL_ODF8xFree_Meas	DD76512	3.125	15.625	6.181	5.12	7.46	0.42	2.43	6.194	5.03	7.44	0.43	2.38	-0.2
MHz	25	fFREE	PLL_ODF8xFree_Meas	DD76512	3.125	15.625	7.763	6.78	8.92	0.419	3.69	7.748	6.76	8.91	0.417	3.69	0.2
MHz	150	fFREE	PLL_ODF8xFree_Meas	DD76512	3.125	15.625	11.626	10.66	12.75	0.464	2.87	11.693	10.72	12.83	0.459	2.85	-0.58