freescale semiconductor

AEC-Q100G/Comm/Ind Tier Qual Results

Objective: Cu wire qualification in FSL-TJN-FM for AW60&AC16 on 7x7LQFP&10x10LQFP Package

Freescale PN:	Varies	Customer Name(s):	"Varies"	Plan or Results:	Rev 1.0 - Result
Part Name:	Varies	PN(s):	"Varies"	Revision # & Date:	See revision history
Technology:	0.25um SGF				
Package:	10x10LQFP64&44, 7x7LQFP32 / 8426, 8256&6300	Design Engr:	Not applicable	QUARTZ Tracking #:	NA
Fab / Assembly / Final Test Sites:	FSL-CHD-FAB / FSL-TJN-FM / Final FSL-TJN-FM	Product Engr:	Guo Donna-B06244		(Signature/Date shown below may be electronic)
Maskset#:	in report	GAO(Global Assembly Aperation) Engr:	Guo Rachel-R64564	GAO Approval (for DIM/BOM results)	Rachel Guo
Rev#:				Signature & Date:	Jun-17-2013
Die Size (in mm) W x L x T	in report	NPI PRQE:	Long Nancy - B07252	NPI PRQE Approval Signature & Date:	Nancy Long Jun-13-2013
Part Operating Temp. Grade:	Grade 1 / - 40℃ to +125 ℃	Trace/DateCode:	LOT A / LOT B / LOT C	CAB Approval	13100528M
				Signature & Date:	Jun-17-2013
				Customer Approval Signature & Date:	May be N/A

TESTS HIGHLIGHTED IN YELLOW WILL BE PERFORMED FOR THIS STUDY

This testing is performed by Freescale Reliability Lab (TJN) unless otherwise noted in the Comments.

GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
PC	JESD22-A113 J-STD-020	**Preconditioning (PC) :** PC required for SMDs only. MSL 3 @ 260℃, +5/-0℃ (or document otherwise with justification)	TEST @ RH	All surface mount devices prior to THB, HAST, AC, UHST, TC, PC+PTC and as required per test conditions.			passed	Generic data: Q202057, JM60 (CHD, M36H), 64LQFP: 0/693 Q203037, DRACO4 (CHD, L11Y), 64LQFP:0/77 Q215084, Celis(CHD, N03F), 44LQFP:0/77 Q197820, DRACO4 (TSMC3, N22A), 64LQFP: 0/693 Q206678, QE32(CHD, M49M), 32LQFP: 0/693
HAST	JESD22-A101 A110	**Highly Accelerated Stress Test (HAST):** PC before HAST (for SMDs only): Required HAST = 130℃/85%RH for 96 hrs Bias = Max Vdd (or justify othrwise) *Timed RO of 48hrs. MAX*	TEST @ RH	77	0	0	passed	Generic data: Q202057, JM60 (CHD, M36H), 64LQFP: 0/231 Q197820, DRACO4 (TSMC3, N22A), 64LQFP: 0/231 Q206678, QE32(CHD, M49M), 32LQFP: 0/231 202629, AC16(TSMC3, N50A), 32LQFP: 0/77
AC	JESD22-A102 A118	**Autoclave (AC):** PC before AC (for SMDs only): Required AC = 121℃/100%RH/15 psig for 96 hrs *Timed RO of 2-48hrs. MAX*	TEST @ R	77	0	0	passed	Generic data: Q202057, JM60 (CHD, M36H), 64LQFP: 0/231 Q197820, DRACO4 (TSMC3, N22A), 64LQFP: 0/231 Q206678, QE32(CHD, M49M), 32LQFP: 0/231
TC	JESD22-A104 AEC Q100-Appendix 3	**Temperature Cycle (TC):** PC before TC (for SMDs only): Required TC = -65℃ to 150℃ for 500 cycles. For AEC only: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.	TEST @ H For AEC: WBP =/> 3 grams	77	0	0	passed	Generic data: Q202057, JM60 (CHD, M36H), 64LQFP: 0/231, WP: 0/5, min>3g Q203037, DRACO4 (CHD, L11Y), 64LQFP:0/77, WP: 0/5, min>3g Q215084, Celis(CHD, N03F), 44LQFP:0/77, WP: 0/5, min>3g Q206678, QE32(CHD, M49M), 32LQFP: 0/231, WP: 0/5, min>3g
HTSL	JESD22-A103	**High Temperature Storage Life (HTSL):** 175℃ for 504hrs *Timed RO = 96hrs. MAX*	TEST @ RH	77	0	0	passed	Generic data: Q202057, JM60 (CHD, M36H), 64LQFP: 0/231 Q203037, DRACO4 (CHD, L11Y), 64LQFP:0/77 Q215084, Celis(CHD, N03F), 44LQFP:0/77 Q206678, QE32(CHD, M49M), 32LQFP: 0/231

TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
HTOL	JESD22-A108	**High Temperature Operating Life (HTOL):** AEC Ta = 125℃ for 1008 hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0	Passed	Generic data for Cu wire: Q197820, DRACO4 (TSMC3, N22A), 64LQFP: 0/77 Q203037, DRACO4 (CHD, L11Y), 64LQFP: 0/77 Q202062, LL16(TSMC3, N21A):, 64LQFP: 0/77 Q202059, LL16(CHD, M60K), 64LQFP: 0/77 Q206758, DZ60(ATMC, M74K), 64LQFP: 0/77 Q216026, DZ60(TSMC11, N88E), 64LQFP: 0/77
ELFR	AEC Q100-008	**Early Life Failure Rate (ELFR):** AEC Ta = 125℃ for 48 hrs *Timed RO of 48 hrs MAX*	TEST @ RH	800	0	0	Passed	Generic data for Cu wire: Q197820, DRACO4 (TSMC3, N22A), 64LQFP: 0/611 Q203037, DRACO4 (CHD, L11Y), 64LQFP: 0/611 Q202062, LL16(TSMC3, N21A):, 64LQFP: 0/611 Q202059, LL16(CHD, M60K), 64LQFP: 0/611 Q206758, DZ60(ATMC, M74K), 64LQFP: 0/611 Q216026, DZ60(TSMC11, N88E), 64LQFP: 0/611
EDR	AEC Q100-005	**NVM Endurance, Data Retention, and Operational Life (EDR):** 150℃ for 1008 hrs or 175℃ for 504hrs Devices incorporating NVM shall receive 1X 'NVM endurance preconditioning'(W/E cycling). Test R, H, C after W/E cycling. *Timed RO of 96hrs. MAX*	TEST @ RHC	77	0	0		Not required for Cu wire qual

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
WBS	AEC Q100-001	**Wire Bond shear (WBS)**	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	passed	Generic data: Q203037, DRACO4 (CHD, L11Y), 64LQFP: 0/5, Cpk>1.67 Q202057, JM60 (CHD, M36H), 64LQFP: 0/5, Cpk>1.67 Q215084, Celis(CHD, N03F), 44LQFP: 0/5, Cpk>1.67 AW60(CHD, M75B) 44LQFP Cu wire qual assembly CZ: 0/5, Cpk>1.67 AC16(CHD, M62J) 32LQFP Cu wire qual assembly CZ: 0/5, Cpk>1.67
WBP	MilStd883-2011	**Wire Bond Pull (WBP):** Cond. C or D	Cpk = or > 1.67	30 bonds from minimum 5 units	0	0	passed	Generic data: Q203037, DRACO4 (CHD, L11Y), 64LQFP: 0/5, Cpk>1.67 Q202057, JM60 (CHD, M36H), 64LQFP: 0/5, Cpk>1.67 Q215084, Celis(CHD, N03F), 44LQFP: 0/5, Cpk>1.67 AW60(CHD, M75B) 44LQFP Cu wire qual assembly CZ: 0/5, Cpk>1.67 AC16(CHD, M62J) 32LQFP Cu wire qual assembly CZ: 0/5, Cpk>1.67
SD	JESD22-B102	**Solderability (SD):** 8hr.(1 hr. for Au-plated leads) Steam age prior to test. If production burn-in is done, samples must also undergo burn-in prior to SD.	>95% lead coverage of critical areas	15	0	0		not required for Cu wire change
PD	JESD22-B100	**Physical Dimensions(PD):** PD per FSL 98A drawing	Cpk = or > 1.67	10	0	0		not required for Cu wire change
DIM & BOM		**Dimensional (DIM):** GAO to verify PD results against valid 98A drawing. **BOM Verification (BOM):** GAO to verify qual lot ERF BOM is accurate.					DIM: not required BOM: passed	
SBS	AEC-Q100-010	**Solder Ball Shear (SBS):** Performed on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Lead Frame (but NOT Flip Chip). Two reflow cycles at MSL reflow temperature before shear.	Cpk = or >1.67	10 (5 balls from a min. of 10 devices)	0	0		For solder ball mounted packages only; NOT for Flip Chips.
LI	JESD22-B105	**Lead Integrity (LI):** Not required for surface mount devices; Only required for through-hole devices.	No lead breakage or cracks	5 (10 leads from each of 5 parts)	0	0		

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Freescale PN: Varies Part Name: Varies	Customer Name(s): "Varies" PN(s): "Varies"	Plan or Results: Rev 1.0 - Result Revision # & Date: See revision history

TEST GROUP E - ELECTRICAL VERIFICATION TESTS

Stress Test	Reference	Test Conditions	End Point Requirements	Minimum Sample Size	# of Lots	Total Units including spares	Results Lot ID-(#Rej/SS) NA=Not Applicable	Comments or Generic Data
TEST	Freescale 48A	**Pre- and Post Functional / Parametrics (TEST):** For AEC, test software shall meet requirements of AEC-Q100-007. Testing performed to the limits of device specification in temperature and limit value.	0 Fails	All	All	All	See Results Summary	This action refers to Final Testing of all qualification units.
CCU	Freescale 12MYS-62419B	**Control/Correlation Units (CCU):** CCU required Units shall be marked to distinguish them from the qual units and must be marked in such a way as to retain marking over the test temperature.	NA	60 30 units as primary units, 30 units as back-up units	0	0		not required
HBM	AEC-Q100-002 / JESD22-A114E Jan 2007	**ElectroStatic Discharge/** **Human Body Model Classification (HBM):** Test @ 500/1000/1500/2000 Volts For AEC, see AEC-Q100-002 for classification levels.	TEST @ RH 2KV min.	3 units per Voltage level	0	0		not required
MM	AEC-Q100-003 or JESD22	**ElectroStatic Discharge/** **Machine Model Classification m(MM):** Test @ 200 Volts For AEC, see AEC-Q100-003 for classification levels.	TEST @ RH 200V only	3 units per Voltage level	0	0		not required
CDM	AEC-Q100-011	**ElectroStatic Discharge/** **Charged Device Model Classification (CDM):** Test @ 250/500/750Volts For AEC, see AEC-Q100-011 for classification levels. ***Timed RO of 96hrs MAX.***	TEST @ RH All pins =/> 500V For AEC, Corner pins =/> 750V;	3 units per Voltage level	0	0		not required
LU	JESD78 plus AEC-Q100- 004 for AEC	**Latch-up (LU):** Test per JEDEC JESD78 with the AEC-Q100-004 requirements for AEC. Ta= Maximum operating temperature Vsupply = Maximum operating voltage	TEST @ RH	6	0	0		not required
ED	AEC-Q100-009, Freescale 48A spec	**Electrical Distribution (ED)**	TEST @ RHC For AEC, Cpk target > 1.67	30	0	0	ED comparison Cu vs Au: done on DZ60 detail refer to DZ60 ED report	
FG	For AEC, AEC-Q100-007	**Fault Grading (FG)**	FG shall be = or > 90% for qual units				FG%= no change	
CHAR	For AEC, AEC-Q003	**Characterization (CHAR):** Ony performed on new technologies and part families per AEC Q003.						
GL (for information only)	For AEC, AEC-Q100-006	**Electro-Thermally Induced Gate Leakage (GL):** 155℃, 2.0 min, +400/-400 V Per AEC Q100 Rev G, this test is performed for information only. *Timed RO of 96 hrs MAX.* *For all failures, perform unbiased bake (4hrs/125℃, or 2hrs/150℃) and retest; recovered units are GL failures.*	TEST @ R	6	0	0		
EMC	IEC 61967-2 - Radiated Emission Measurement (TEM Cell)	**Electromagnetic Compatibility (EMC)** Test per IEC 61967-2. Ta= Room Temp Vsupply = Typical operating voltage						

Covered device and BOM

Logic Part	Fab/Mask set	WAFER TECH CD	Assembly Site	PACK DESCRIPTION	DIE SIZE(mmxmm)	MOLD COMPOUND	EPOXY DESCRIPTION	Wire
AW60 Auto	FSL-CHD-FAB/M75B	E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	2.850X2.820	CEL-9200HF10M CU WIRE	DA SUMITOMO CRM-1064MBL	Cu, 25um
AW60 Auto	FSL-CHD-FAB/M75B	E025FXXQ	FSL-TJN-FM	LQFP 44 10*10*1.4P0.8/8256	2.850X2.820	CEL-9200HF10M CU WIRE	DA SUMITOMO CRM-1064MBL	Cu, 25um
AC16 Auto	FSL-CHD-FAB/M62J	E025FXXQ	FSL-TJN-FM	LQFP 44 10*10*1.4P0.8/8256	2.624X2.624	CEL-9200HF10M CU WIRE	DA SUMITOMO CRM-1064MBL	Cu, 25um
AC16 Auto	FSL-CHD-FAB/M62J	E025FXXQ	FSL-TJN-FM	LQFP 32 7*7*1.4P0.8/6300	2.624X2.624	CEL-9200HF10M CU WIRE	DA SUMITOMO CRM-1064MBL	Cu, 25um

Generic data

Quartz	Logic Part	Fab/Mask set/Wafer Tech CD	Assembly Site	PACK DESCRIPTION	DIE SIZE(mmxmm)	MOLD COMPOUND	EPOXY DESCRIPTION	Wire Description	CAB
197820	9S08GB60A(DRACO4)	TSMC3/N22A/E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	3.080X3.150	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10403228M
203037	9S08GB60A(DRACO4)	FSL-CHD-FAB/L11Y/E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	3.080X3.150	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu, 25um	10453590M
202057	S08JM60	FSL-CHD-FAB/M36H/E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	3.474X3.084	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu, 25um	10443516M
202062	MC9S08LL16	TSMC3/N21A/E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	2.472X2.672	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10443516M
202059	MC9S08LL16	FSL-CHD-FAB/M60K/E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	2.472X2.672	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10443516M
215084	MCF51AC256(Celis)	FSL-CHD-FAB/N03F/E025FXXQ	FSL-TJN-FM	LQFP 44 10*10*1.4P0.8/8256	5.077 X 4.472	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	11171391M
206678	MC9S08QE32	FSL-CHD-FAB/M49M/E025FXXQ	FSL-TJN-FM	LQFP 32 7*7*1.4P0.8/6300	2.783X2.653	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10443516M
NA	S08AW60	FSL-CHD-FAB/M75B/E025FXXQ	FSL-TJN-FM	LQFP 44 10*10*1.4P0.8/8256	2.850X2.820	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10453590M
NA	S08AC16	FSL-CHD-FAB/M62J/E025FXXQ	FSL-TJN-FM	LQFP 32 7*7*1.4P0.8/6300	2.624X2.624	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10443516M
216026	9S08DZ60	TSMC11/N88E/E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	3.385X3.334	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10453591M
206758	9S08DZ60	FSL-ATMC-FAB/M74K/E025FXXQ	FSL-TJN-FM	LQFP 64 10*10*1.4P0.5/8426	3.390X3.366	HITACHI 9200HF10M	SUMITOMO CRM-1064MBL	Cu 25um	10453591M

Revision	Date	Comments	Author
Rev. 1.0	14-Jun-13	Update Qual report	Nancy Long

S08DZ60, S08DZ128, S08AW60, S08AC16 Copper Wire Qualification

1. Objective

This report describes the 25um Cu wire for 48/64LQFP S908DZ60, 64LQFP S908DZ128, 44/64 LQFP AW60 and 32/44LQFP S908AC16 electrical distribution data versus baseline 25um Au wire.

Current Wire:
25um Au wire

Proposed New Wire:
25um Cu wire

2. General Information

Product Family: S908DZ60, S908DZ128, S908AW60 and S908AC16
Fab site: FSL-ATMC-Fab, and FSL-CHD-Fab
Mask set: M74K, M05C, M78G, M75B, M62J
Package(s): 32LQFP/ 44LQFP/ 48LQFP/ 64LQFP
Assembly Site: Freescale Tianjin, China

3. Method

Two data sets taken from selected key product, 30 units in each set at T0 analysis:

1. 30 units from 25um Cu wire diameter qual lot
2. 30 units from 25um Au wire diameter control lot

Both qualification and control lots are tested to standard production final test flow. Electrical distribution data generated from the selected key parametric tests with Freescale standard criteria CPK > 1.67 and shift ≤ 15%, justification will be provided if otherwise.

4. Data and Summary:

4.1. Electrical Distribution Table:

Selected Key Product: S908DZ60 (64LQFP) M74K

Hot Temperature				Baseline Time 0 Data (Gold Wire) 125C			Qual Time 0 Data (Copper Wire) 125C			Lower Spec Limit % Shift	Upper Spec Limit % Shift	
Parameter Name in Datasheet	Units	Lower Spec Limit	Upper Spec Limit	Avg	Std	Cpk	Avg	Std	Cpk	negative drift is toward LSL	positive drift is toward USL	Comment
RIDD (fBus = 20 MHz)	mA	na	24	15.12	0.24	12.46	14.83	0.27	11.17	na	3.27%	
RIDD (fBus = 8 MHz)	mA	na	11.4	7.74	0.09	12.97	7.58	0.13	9.90	na	4.15%	
S2IDD	uA	na	70	22.83	2.33	6.74	20.88	1.61	10.16	na	4.13%	
S3IDD	uA	na	90	31.31	3.06	6.39	30.00	2.09	9.56	na	2.23%	
RPU	Komh	20	65	23.71	0.46	2.67	23.84	0.51	2.52	3.37%	-0.30%	
RPD	Komh	20	65	22.96	0.26	3.74	23.26	0.35	3.11	10.18%	-0.72%	
|IIn| (VIn = VSS)	nA	na	1000	152.81	14.25	19.82	130.05	10.22	28.39	na	2.69%	
|IIn| (VIn = VDD)	nA	-1000	na	-24.24	3.23	100.72	-21.93	2.64	123.47	0.24%	na	
fdco_t	Mhz	31.36	32.64	31.92	0.03	6.12	31.92	0.03	6.93	-0.09%	0.07%	

Room Temperature				Baseline Time 0 Data (Gold Wire) 25C			Qual Time 0 Data (Copper Wire) 25C			Lower Spec Limit % Shift	Upper Spec Limit % Shift	
Parameter Name in Datasheet	Units	Lower Spec Limit	Upper Spec Limit	Avg	Std	Cpk	Avg	Std	Cpk	negative drift is toward LSL	positive drift is toward USL	Comment
RIDD (fBus = 20 MHz)	mA	na	24	14.98	0.26	11.58	14.62	0.23	13.77	na	3.91%	
RIDD (fBus = 8 MHz)	mA	na	11.4	7.79	0.08	14.65	7.68	0.12	10.68	na	3.20%	
S2IDD	uA	na	5	1.45	0.05	21.78	1.42	0.04	29.99	na	0.83%	
S3IDD	uA	na	5	1.52	0.07	17.30	1.48	0.04	26.39	na	1.07%	
RPU	Komh	20	65	25.10	0.34	5.03	25.40	0.46	3.94	5.86%	-0.75%	
RPD	Komh	20	65	23.56	0.34	3.53	23.83	0.39	3.26	7.69%	-0.66%	
|IIn| (VIn = VSS)	nA	na	1000	10.42	2.84	116.09	11.46	3.23	102.15	na	-0.11%	
|IIn| (VIn = VDD)	nA	-1000	na	0.89	3.02	110.38	-0.22	2.66	125.31	-0.11%	na	
fdco_t	Mhz	31.36	32.64	32.19	0.03	5.44	32.19	0.03	5.79	-0.29%	0.53%	

Cold Temperature				Baseline Time 0 Data (Gold Wire) -40C			Qual Time 0 Data (Copper Wire) -40C			Lower Spec Limit % Shift	Upper Spec Limit % Shift	
Parameter Name in Datasheet	Units	Lower Spec Limit	Upper Spec Limit	Avg	Std	Cpk	Avg	Std	Cpk	negative drift is toward LSL	positive drift is toward USL	Comment
RIDD (fBus = 20 MHz)	mA	na	24	15.01	0.22	13.62	14.73	0.25	12.35	na	3.18%	
RIDD (fBus = 8 MHz)	mA	na	11.4	7.81	0.13	9.31	7.64	0.16	7.99	na	4.76%	
S2IDD	uA	na	5	1.11	0.04	34.41	1.13	0.05	27.43	na	-0.56%	
S3IDD	uA	na	5	1.10	0.04	30.55	1.13	0.05	28.51	na	-0.75%	
RPU	Komh	20	65	26.20	0.42	4.90	26.40	0.43	5.00	3.27%	-0.52%	
RPD	Komh	20	65	24.70	0.37	4.18	25.03	0.51	3.30	6.91%	-0.81%	
|IIn| (VIn = VSS)	nA	na	1000	10.52	2.80	117.61	10.93	3.30	99.94	na	-0.04%	
|IIn| (VIn = VDD)	nA	-1000	na	0.51	2.80	119.25	0.74	2.96	112.68	0.02%	na	
fdco_t	Mhz	31.36	32.64	32.07	0.02	8.03	32.07	0.03	7.19	1.10%	-1.36%	

"Shift analysis" refers to analysis of shift of the distribution mean towards the nearest specification limit:
"% Shift (USL) = {Mean(new)-Mean(old)} / {Upper Spec Limit-Mean(old)}
% Shift (LSL) = {Mean(new)-Mean(old)} / {Mean(old)-Lower Spec Limit}

4.2. Summary:

From the above data, it was verified that the requirements and acceptance criteria was achieved.

5. Document History:

Rev	Date	Originator
O	June 19th 2013	Guo Donna

Appendix A: Justifications for any Shifts > 15%

Not applicable as no parameter shift > 15%.