SPC5606 (1M) and SPC5605 (768K), 100/144/176 LQFP Copper Wire Qualification (PCN 15964)

1. Objective

This report describes the Taiwan Semiconductor Manufacturing Company Fab 14 (TSMC14) fab site for 100LQFP/144LQFP/176LQFP SPC5606 (1M) and SPC5605 (768K) electrical distribution data on Cu wire versus baseline from Freescale Austin Technology Manufacturing Center (ATMC) fab site also on Cu wire.

Refer to the table below for current and proposed wire:-

Wafer FAB	ASSEMBLY SITES	PACKAGE TYPE	CURRENT WIRE	NEW WIRE
TSMC 14	ASECL	176LQFP	N/A	Cu 20um
TSMC 14	FSL-KLM-FM	144LQFP/100LQFP	N/A	PdCu 20um
FSL-ATMC	ASECL	176LQFP	Au 23um	Cu 20um
FSL-ATMC	FSL-KLM-FM	144LQFP/100LQFP	Au 23um	PdCu 20um

2. General Information

Product Family: SPC5606 (1M) and SPC5605 (768K)
Fab site: TSMC14
Mask set: N13E
Package(s): 100LQFP/144LQFP/176LQFP
Assembly Site: Freescale Kuala Lumpur, Malaysia and Advanced Semiconductor Engineering Chung Li, Taiwan

3. Method

Four data sets taken from selected key product, 30 units in each set at T0 analysis:

1. 30 units from 20um PdCu wire diameter qual lot from TSMC14 fab site
2. 30 units from 20um PdCu wire diameter control lot from ATMC fab site
3. 30 units from 20um PdCu wire diameter qual lot from ATMC fab site
4. 30 units from 23um Au wire diameter control lot from ATMC fab site

Both qualification and control lots are tested to standard production final test flow. Electrical distribution data generated from the selected key parametric tests with Freescale standard criteria CPK > 1.67 and shift ≤ 15%, justification will be provided if otherwise.

4. Data and Summary:

4.1. Electrical Distribution Table:

Selected Key Product: SPC5607B (100LQFP) N69H

				ATMC CU T0			TSMC14 Cu T0			T0 Mean Drift toward LSL	T0 Mean Drift toward USL	Comment
				Temp	150	C	Temp	150	C			
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**	Drift within +/- 1 sigma or less than +/- 15% to spec	Drift within +/- 1 sigma or less than +/- 15% to spec	
fSIRCVAR_LS_OSC_PAD 33	KHz	115.20	140.80	129.16	0.0001	52390.52	129.22	0.0001	54183.40	0.44%	0.52%	PASS
fSIRCVAR_Main_OSC_PAD 33	MHz	15.20	16.80	16.14	0.0004	618.89	16.07	0.0003	718.22	-7.57%	-10.82%	PASS
VLVDLVCORL	V	1.08	1.14	1.11	0.004	1.89	1.11	0.003	2.85	-5.00%	-6.89%	PASS
VLVDLVCORL	V	1.08	1.16	1.11	0.005	2.33	1.11	0.005	2.27	-4.72%	-3.44%	PASS
VLPREG_PAD 14	V	1.15	1.32	1.19	0.01	1.72	1.19	0.01	1.74	11.62%	3.02%	PASS
VLPREG_PAD 43	V	1.16	1.32	1.18	0.001	10.71	1.19	0.01	1.68	11.02%	1.98%	PASS
VMREG_PAD 14	V	1.16	1.32	1.19	0.001	8.65	1.19	0.002	4.92	-12.69%	-2.84%	PASS
VMREG_PAD 43	V	1.15	1.32	1.29	0.001	7.65	1.29	0.002	6.62	-2.83%	-12.84%	PASS
gmFXOSC_Margin1_5V5	mA/V	2.50	9.20	5.73	0.19	5.53	5.82	0.07	15.34	2.64%	2.46%	PASS
gmFXOSC_Margin0_5V5	mA/V	2.00	7.40	4.68	0.16	5.60	4.75	0.06	14.90	2.56%	2.52%	PASS
gmFXOSC_Margin1_3V3	mA/V	2.70	9.70	5.87	0.21	5.00	5.98	0.08	14.51	3.34%	2.77%	PASS
gmFXOSC_Margin0_3V3	mA/V	2.20	8.20	4.93	0.18	5.06	5.02	0.06	14.57	3.27%	2.73%	PASS
fFREE_ODF16x_PAD 33	MHz	1.56	7.81	5.75	0.28	2.49	5.92	0.24	2.64	4.16%	8.43%	PASS
fFREE_ODF8x_PAD 33	MHz	3.13	15.63	11.49	0.34	4.05	11.84	0.22	5.73	4.20%	8.50%	PASS

fPLLOUT_4x10MHz_PAD 33	MHz	39.53	40.32	40.00	0.00	NA	40.00	0.00	NA	0.00%	0.00%	Cpk NA because Stdev is 0
fPLLOUT_2x10MHz_PAD 33	MHz	19.80	20.20	20.00	0.00	NA	20.00	0.00	NA	0.00%	0.00%	Cpk NA because Stdev is 0
IDDRUN_64MHz_HVADC	mA	NA	125.00	7.58	0.18	218.23	7.18	0.16	245.78	NA	-0.34%	PASS
IDDRUN_64MHz_VDD_BV	mA	NA	125.00	71.70	0.43	41.64	70.70	1.02	17.76	NA	-1.88%	PASS
IDDRUN_64MHz_VDD_HV	mA	NA	125.00	9.22	0.06	674.27	9.09	0.12	329.42	NA	-0.11%	PASS
IDDSTDBY2_VDD_HV	uA	NA	1700.00	48.11	5.82	94.60	76.03	4.58	118.18	NA	1.69%	PASS
IDDSTDBY2_VDD_BV	uA	NA	1700.00	221.52	40.94	12.04	308.21	50.31	9.22	NA	5.86%	PASS
IDDSTOP_BV	mA	NA	14.00	6.50	0.48	5.24	7.46	0.94	2.31	NA	12.75%	PASS
IDDSTOP_HV	mA	NA	14.00	0.08	0.004	1054.26	0.07	0.004	1298.43	NA	-0.06%	PASS
IIWPUI_VIH_5V5	PAD_14 & PAD_17: lowest Cpk & largest shift among 58 pins.											
PAD_14	uA	10.00	250.00	30.88	0.19	36.28	27.75	0.18	32.52	-14.99%	-1.43%	PASS
PAD_70	uA	10.00	250.00	30.44	0.29	23.91	27.66	0.16	35.79	-13.59%	-1.27%	PASS
IIWPDI_VIH_5V5	PAD_70 & PAD_32: lowest Cpk & largest shift among 58 pins.											
PAD_70	uA	10.00	250.00	45.81	0.43	27.83	48.16	0.40	31.66	6.56%	1.15%	PASS
PAD_32	uA	10.00	250.00	45.49	0.39	30.25	48.23	0.36	34.95	7.73%	1.34%	PASS
IIWPUI_VIH_3V3	PAD_5 & PAD_75: lowest Cpk & largest shift among 58 pins.											
PAD_5	uA	10.00	150.00	17.94	0.24	11.09	16.80	0.13	17.71	-14.43%	-0.87%	PASS
PAD_75	uA	10.00	150.00	18.17	0.30	9.10	17.70	0.14	18.75	-5.71%	-0.35%	PASS
IIWPDI_VIH_3V3	PAD_42 & ILKG_L_Vpp: lowest Cpk & largest shift among 61 pins.											
PAD_42	uA	10.00	150.00	26.36	0.30	17.89	28.76	0.26	23.96	14.69%	1.94%	PASS
ILKG_L_Vpp	nA	NA	1000.00	685.94	47.82	2.19	642.15	37.57	3.17	NA	-13.94%	PASS
ILKG_L_Odd	PAD_58 & PAD_23: lowest Cpk & largest shift among 37 pins.											
PAD_58	nA	NA	1000.00	27.86	2.17	149.17	33.37	3.58	90.09	NA	0.57%	PASS
PAD_23	nA	NA	1000.00	26.93	2.58	125.51	33.72	3.34	96.49	NA	0.70%	PASS
ILKG_H_Odd	PAD_10 & PAD_21: lowest Cpk & largest shift among 37 pins.											
PAD_10	nA	NA	1000.00	53.39	5.36	58.82	63.84	7.05	44.27	NA	1.10%	PASS
PAD_21	nA	NA	1000.00	23.39	2.61	124.90	30.83	4.72	68.51	NA	0.76%	PASS
ILKG_L_Even	PAD_3: lowest Cpk & largest shift among 39 pins.											
PAD_3	nA	NA	1000.00	31.67	2.57	125.70	39.23	3.83	83.61	NA	0.78%	PASS
ILKG_H_Even	PAD_3 & PAD_7: lowest Cpk & largest shift among 39 pins.											
PAD_7	nA	NA	1000.00	53.13	4.99	63.20	63.39	7.27	42.96	NA	1.08%	PASS

PAD_3	nA	NA	1000.00	52.79	4.82	65.50	62.33	6.53	47.85	NA	1.01%	PASS
VOH	PAD_33 & PAD_10: lowest Cpk & largest shift among 60 pins.											
PAD 33	uA	4.00	NA	5.27	0.01	69.14	5.27	0.01	36.65	0.11%	NA	PASS
PAD_10	V	4.00	NA	5.42	0.003	145.49	5.41	0.003	184.28	-0.62%	NA	PASS
VOL	PAD_33: lowest Cpk & largest shift among 60 pins.											
PAD 33	uA	NA	0.50	0.27	0.01	15.12	0.25	0.01	9.11	NA	-6.98%	PASS

				ATMC Cu T0			**TSMC14 Cu T0**			**T0 Mean Drift toward LSL**	**T0 Mean Drift toward USL**	**Comment**
				Temp	-40	C	**Temp**	-40	C			
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**	Drift within +/- 1 sigma or less than +/- 15% to spec	Drift within +/- 1 sigma or less than +/- 15% to spec	
fSIRCVAR_LS_OSC_PAD 33	KHz	115.20	140.80	127.38	0.0001	55473.95	127.21	0.0001	54885.58	-1.40%	-1.27%	PASS
fSIRCVAR_Main_OSC_PAD 33	MHz	15.20	16.80	15.82	0.0003	639.22	15.87	0.0004	599.62	7.78%	4.97%	PASS
VLVDLVBKPL	V	1.08	1.16	1.10	0.004	1.72	1.10	0.003	1.99	-7.71%	-2.51%	PASS
VLVDLVCORL	V	1.08	1.16	1.10	0.004	1.72	1.10	0.003	1.99	-7.71%	-2.51%	PASS
VLPREG_PAD 14	V	1.15	1.32	1.21	0.01	2.74	1.22	0.01	3.76	2.56%	1.54%	PASS
VLPREG_PAD 43	V	1.15	1.32	1.21	0.01	3.31	1.22	0.01	3.80	6.12%	3.50%	PASS
VMREG_PAD 14	V	1.16	1.32	1.22	0.01	1.91	1.22	0.01	1.78	-5.52%	-3.45%	PASS
VMREG_PAD 43	V	1.16	1.32	1.22	0.01	1.96	1.22	0.01	1.79	-2.08%	-1.24%	PASS
gmFXOSC_Margin1_5V5	mA/V	2.50	9.20	5.87	0.43	2.57	5.78	0.13	8.33	-2.87%	-2.91%	PASS
gmFXOSC_Margin0_5V5	mA/V	2.00	7.40	4.78	0.35	2.46	4.70	0.11	8.43	-2.82%	-2.99%	PASS
gmFXOSC_Margin1_3V3	mA/V	2.70	9.70	5.87	0.47	2.23	5.77	0.14	7.22	-3.15%	-2.61%	PASS
gmFXOSC_Margin0_3V3	mA/V	2.20	8.20	4.92	0.40	2.27	4.84	0.12	7.38	-3.06%	-2.54%	PASS
fFREE_ODF16x_PAD 33	MHz	1.56	7.81	2.83	0.23	1.81	2.99	0.26	1.83	13.16%	3.33%	PASS

fFREE_ODF8x_PAD 33	MHz	3.13	15.63	5.65	0.12	7.27	5.98	0.30	3.18	13.10%	3.32%	PASS
fPLLOUT_4x10MHz_PAD 33	MHz	39.53	40.32	40.00	0.00	NA	40.00	0.00	NA	0.00%	0.00%	Cpk NA because Stdev is 0
fPLLOUT_2x10MHz_PAD 33	MHz	19.80	20.20	20.00	0.00	NA	20.00	0.00	NA	0.00%	0.00%	Cpk NA because Stdev is 0
IDDRUN_64MHz_VDD_HV	mA	NA	125.00	5.89	0.19	208.16	5.45	0.12	345.80	NA	-0.37%	PASS
IDDRUN_64MHz_VDD_BV	mA	NA	125.00	0.06	0.001	64145.97	0.06	0.001	82370.86	NA	-0.002%	PASS
IDDRUN_64MHz_HVADC	mA	NA	125.00	0.01	0.0004	109892.94	0.01	0.0003	148961.20	NA	-0.0001%	PASS
IDDSTOP_HV	uA	NA	900.00	8.64	0.86	346.42	8.81	0.74	400.77	NA	0.02%	PASS
IDDSTOP_BV	uA	NA	900.00	52.27	4.39	64.43	68.20	6.79	40.84	NA	1.88%	PASS
IDDSTDBY2_VDD_BV	uA	NA	100.00	4.10	0.26	122.06	5.27	0.54	58.80	NA	1.22%	PASS
IDDSTDBY2_VDD_HV	uA	NA	100.00	6.59	0.61	51.20	6.63	0.53	58.82	NA	0.05%	PASS
IIWPUI_VIH_5V5		PAD_70 & PAD_41: lowest Cpk & largest shift among 58 pins.										
PAD_70	uA	10.00	250.00	48.35	0.72	17.70	43.01	0.54	20.31	-13.91%	-2.64%	PASS
PAD_41	uA	10.00	250.00	51.01	0.70	19.46	44.90	0.56	20.68	-14.89%	-3.07%	PASS
IIWPDI_VIH_5V5		PAD_70 & PAD_73: lowest Cpk & largest shift among 58 pins.										
PAD_73	uA	10.00	250.00	85.13	1.27	19.72	83.64	1.10	22.29	-1.98%	-0.90%	PASS
PAD_70	uA	10.00	250.00	84.23	1.51	16.41	83.52	1.26	19.44	-0.95%	-0.43%	PASS
IIWPUI_VIH_3V3		PAD_70 & PAD_31: lowest Cpk & largest shift among 58 pins.										
PAD_70	uA	10.00	150.00	28.88	0.64	9.87	26.52	0.40	13.69	-12.52%	-1.95%	PASS
PAD_31	uA	10.00	150.00	29.89	0.52	12.71	26.99	0.32	17.91	-14.59%	-2.42%	PASS
IIWPDI_VIH_3V3		PAD_46 & PAD_14: lowest Cpk & largest shift among 62 pins.										
PAD_46	uA	10.00	150.00	41.27	0.93	11.22	43.16	0.55	19.93	6.05%	1.74%	PASS
PAD_14	uA	10.00	150.00	40.56	0.75	13.63	43.44	0.58	19.23	9.40%	2.63%	PASS
ILKG_L_Odd		PAD_24 & PAD_43: lowest Cpk & largest shift among 37 pins.										
PAD_24	nA	NA	200.00	0.14	0.49	136.25	0.37	0.49	135.36	NA	0.11%	PASS
PAD_43	nA	NA	200.00	0.08	0.37	178.87	0.02	0.70	94.70	NA	-0.03%	PASS
ILKG_H_Odd		PAD_8 & PAD_56: lowest Cpk & largest shift among 37 pins.										
PAD_8	nA	NA	200.00	0.39	0.71	94.05	0.17	0.54	122.30	NA	-0.11%	PASS
PAD_56	nA	NA	200.00	0.41	0.94	70.76	0.14	0.68	97.99	NA	-0.14%	PASS
ILKG_L_Even		PAD_62 & PAD_38: lowest Cpk & largest shift among 39 pins.										
PAD_62	nA	NA	200.00	0.01	0.45	146.71	0.17	0.31	214.77	NA	0.08%	PASS
PAD_38	nA	NA	200.00	0.05	0.63	105.53	0.05	0.47	141.06	NA	0.002%	PASS
ILKG_H_Even		PAD_20 & PAD_38: lowest Cpk & largest shift among 39 pins.										

PAD_20	nA	NA	200.00	0.44	0.61	109.68	0.22	0.46	143.52	NA	-0.11%	PASS
PAD_38	nA	NA	200.00	0.34	1.75	38.13	0.14	1.23	54.33	NA	-0.10%	PASS
VOH		PAD_33 & PAD_72: lowest Cpk & largest shift among 60 pins.										
PAD 33	uA	4.00	NA	5.26	0.04	9.90	5.31	0.03	14.76	3.93%	NA	PASS
PAD_72	V	4.00	NA	5.41	0.00	95.92	5.50	0.00	200.29	6.79%	NA	PASS
VOL		PAD_33 & VOL: lowest Cpk & largest shift among 61 pins.										
PAD 33	uA	NA	0.50	0.24	0.03	3.13	0.21	0.02	5.70	NA	-12.21%	PASS

Selected Key Product: SPC5607B (100QFP) M03Y

				Baseline Time0 (ATMC Au Wire)			Qual Time0 (ATMC Cu Wire)			T0 Mean Drift toward LSL	T0 Mean Drift toward USL	Comment
				Temp	150	C	Temp	150	C			
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**	Drift within +/-1 sigma or less than +/-15% to spec	Drift within +/-1 sigma or less than +/-15% to spec	
fFREE_ODF8x_PAD 33	MHz	3.13	15.63	10.85	0.48	3.33	11.49	0.34	4.05	8.34%	13.47%	PASS
fFREE_ODF16x_PAD 33	MHz	1.56	7.81	5.57	0.26	2.89	5.75	0.28	2.49	4.34%	7.77%	PASS
fPLLOUT_2x10MHz_PAD 33	MHz	19.80	20.20	20.00	0.00	NA	20.00	0.00	NA	0.00%	0.00%	Cpk NA because stdev is 0.
fPLLOUT_4x10MHz_PAD 33	MHz	39.53	40.32	40.00	0.00	NA	40.00	0.00	NA	0.00%	0.00%	Cpk NA because stdev is 0.
fSIRCVAR_Main_OSC_PAD 33	MHz	15.20	16.80	16.14	0.0003	642.20	16.14	0.0004	618.89	0.01%	0.01%	PASS
fSIRCVAR_LS_OSC_PAD 33	KHz	115.20	140.80	128.39	0.0001	53393.97	129.16	0.0001	52390.52	5.84%	6.21%	PASS
gmFXOSC_Margin0_3V3	mA/V	2.20	8.20	4.92	0.40	2.27	4.93	0.18	5.06	0.37%	0.30%	PASS
gmFXOSC_Margin1_3V3	mA/V	2.70	9.70	5.87	0.47	2.23	5.87	0.21	5.00	-0.01%	-0.01%	PASS
gmFXOSC_Margin0_5V5	mA/V	2.00	7.40	4.78	0.35	2.46	4.68	0.16	5.60	-3.81%	-4.05%	PASS
gmFXOSC_Margin1_5V5	mA/V	2.50	9.20	5.87	0.43	2.57	5.73	0.19	5.53	-4.16%	-4.22%	PASS
IDDRUN_64MHz_VDD_HV	mA	NA	125.00	9.18	0.08	510.69	9.22	0.06	674.27	NA	0.03%	PASS
IDDRUN_64MHz_VDD_BV	mA	NA	125.00	68.55	0.77	24.42	71.70	0.43	41.64	NA	5.59%	PASS
IDDRUN_64MHz_HVADC	mA	NA	125.00	7.35	0.28	139.19	7.58	0.18	218.23	NA	0.20%	PASS
IDDSTDBY2_VDD_HV	uA	NA	1700.00	39.14	4.57	121.04	48.11	5.82	94.60	NA	0.54%	PASS
IDDSTDBY2_VDD_BV	uA	NA	1700.00	193.45	23.58	21.29	221.52	40.94	12.04	NA	1.86%	PASS
IDDSTOP_BV	mA	NA	14.00	6.14	0.31	8.55	6.50	0.48	5.24	NA	4.67%	PASS

IDDSTOP_HV	mA	NA	14.00	0.03	0.0031	1478.98	0.08	0.0044	1054.26	NA	0.36%	PASS
IIWPDI_VIH_5V5	PAD_8 & PAD_41: lowest Cpk & largest shift among 58 pins											
PAD_8	uA	10.00	250.00	51.42	0.78	17.77	46.63	0.36	34.25	-11.56%	-2.41%	PASS
PAD_41	uA	10.00	250.00	51.00	0.71	19.36	46.13	0.36	33.37	-11.87%	-2.45%	PASS
IIWPUI_VIH_5V5	PAD_70 & PAD_32: lowest Cpk & largest shift among 58 pins											
PAD_70	uA	10.00	250.00	32.73	0.33	22.97	30.44	0.29	23.91	-10.07%	-1.05%	PASS
PAD_32	uA	10.00	250.00	32.45	0.38	19.70	30.47	0.24	27.87	-8.80%	-0.91%	PASS
IIWPDI_VIH_3V3	PAD_36 & PAD_41: lowest Cpk & largest shift among 58 pins											
PAD_36	uA	10.00	150.00	28.68	0.54	11.55	26.49	0.31	17.63	-11.70%	-1.80%	PASS
PAD_41	uA	10.00	150.00	28.72	0.52	12.08	26.35	0.27	20.36	-12.65%	-1.95%	PASS
IIWPUI_VIH_3V3	PAD_43 & PAD_75: lowest Cpk & largest shift among 58 pins											
PAD_43	uA	10.00	150.00	19.37	0.31	10.08	18.02	0.25	10.83	-14.34%	-1.03%	PASS
PAD_75	uA	10.00	150.00	19.25	0.29	10.50	18.17	0.30	9.10	-11.70%	-0.83%	PASS
ILKG_H_Even	PAD_7 & PAD_11: lowest Cpk & largest shift among 39 pins											
PAD_7	nA	NA	1000.00	14.86	3.62	90.65	53.13	4.99	63.20	NA	3.89%	PASS
PAD_11	nA	NA	1000.00	14.46	3.36	97.63	53.71	5.45	57.87	NA	3.98%	PASS
ILKG_L_Even	PAD_26 & PAD_11: lowest Cpk & largest shift among 39 pins											
PAD_26	nA	NA	1000.00	10.20	2.09	158.04	32.00	2.26	142.92	NA	2.20%	PASS
PAD_11	nA	NA	1000.00	11.04	2.43	135.61	31.77	2.60	124.30	NA	2.10%	PASS
ILKG_H_Odd	PAD_76 & PAD_69: lowest Cpk & largest shift among 37 pins											
PAD_76	nA	NA	1000.00	14.79	3.36	97.70	53.85	5.51	57.21	NA	3.96%	PASS
PAD_69	nA	NA	1000.00	10.97	3.06	107.86	40.88	4.03	79.27	NA	3.02%	PASS
ILKG_L_Odd	PAD_50 & PAD_76: lowest Cpk & largest shift among 37 pins											

PAD_50	nA	NA	1000.00	9.71	2.34	141.24	27.86	2.83	114.39	NA	1.83%	PASS
PAD_76	nA	NA	1000.00	10.84	2.61	126.12	32.39	2.67	120.66	NA	2.18%	PASS
ILKG_H_PAD_33	nA	NA	1000.00	43.07	11.30	28.24	145.83	14.48	19.67	NA	10.74%	PASS
ILKG_L_PAD_33	nA	NA	1000.00	9.72	1.96	168.53	39.94	4.58	69.85	NA	3.05%	PASS
ILKG_H_Vpp	nA	NA	1000.00	172.47	1.56	177.28	185.59	116.81	2.32	NA	1.59%	PASS
ILKG_L_Vpp	nA	NA	1000.00	191.97	9.54	28.23	203.69	47.82	5.55	NA	1.45%	PASS
VLPREG_PAD 14	V	1.16	1.32	1.19	0.01	2.01	1.19	0.005	2.02	-6.09%	-1.46%	PASS
VLPREG_PAD 43	V	1.16	1.32	1.19	0.004	2.55	1.19	0.004	2.41	-11.03%	-2.60%	PASS
VLVDLVBKPL	V	1.08	1.16	1.11	0.004	2.91	1.11	0.004	2.60	8.38%	5.61%	PASS
VLVDLVCORL	V	1.08	1.16	1.11	0.004	2.58	1.11	0.005	2.33	6.97%	4.53%	PASS
VMREG_PAD 14	V	1.16	1.32	1.29	0.002	5.69	1.29	0.001	7.65	-0.54%	-2.31%	PASS
VMREG_PAD 43	V	1.16	1.32	1.19	0.002	5.74	1.19	0.001	8.65	-2.66%	-0.62%	PASS
VOH	PAD_2 & PAD_33: lowest Cpk & largest shift among 60 pins											
PAD_2	V	4.00	NA	5.41	0.004	105.46	5.40	0.005	99.81	-0.94%	NA	PASS
PAD_33	V	4.00	NA	5.28	0.04	9.73	5.27	0.01	69.14	-0.74%	NA	PASS
VOL	PAD_33: lowest Cpk & largest shift among 61 pins											
PAD_33	V	NA	0.5	0.253	0.029	2.85	0.270	0.005	15.12	NA	7.12%	PASS

				Baseline Time0 (ATMC Au Wire)			Qual Time0 (ATMC Cu Wire)			T0 Mean Drift toward LSL	T0 Mean Drift toward USL	Comment
				Temp	-40	C	Temp	-40	C			
Parameter Name, as in Datasheet	**Units**	**Lower Spec Limit** (NA if no spec)	**Upper Spec Limit** (NA if no spec)	**Avg**	**Std**	**Cpk**	**Avg**	**Std**	**Cpk**	Drift within +/-1 sigma or less than +/-15% to spec	Drift within +/-1 sigma or less than +/-15% to spec	
fFREE_ODF8x_PAD 33	MHz	3.13	15.63	6.00	0.11	8.47	5.65	0.12	7.27	-12.08%	-3.61%	PASS
fFREE_ODF16x_PAD 33	MHz	1.56	7.81	3.00	0.23	2.12	2.83	0.23	1.81	-12.13%	-3.62%	PASS
fPLLOUT_2x10MHz_PAD 33	MHz	19.80	20.20	20.00	0.00	NA	20.00	0.00	NA	0.00%	0.00%	Cpk NA because stdev is 0.
fPLLOUT_4x10MHz_PAD 33	MHz	39.53	40.32	40.00	0.00	NA	40.00	0.00	NA	0.00%	0.00%	Cpk NA because stdev is 0.
fSIRCVAR_Main_OSC_PAD 33	MHz	15.20	16.80	15.89	0.0003	711.48	15.82	0.0003	639.22	-9.26%	-6.98%	PASS
fSIRCVAR_LS_OSC_PAD 33	KHz	115.20	140.80	127.74	0.0001	57227.89	127.38	0.0001	55473.95	-2.81%	-2.69%	PASS
gmFXOSC_Margin0_3V3	mA/V	2.20	8.20	4.84	0.34	2.61	4.92	0.40	2.27	3.14%	2.46%	PASS
gmFXOSC_Margin1_3V3	mA/V	2.70	9.70	5.77	0.40	2.57	5.87	0.47	2.23	3.25%	2.54%	PASS
gmFXOSC_Margin0_5V5	mA/V	2.00	7.40	4.68	0.30	2.99	4.78	0.35	2.46	3.95%	3.89%	PASS
gmFXOSC_Margin1_5V5	mA/V	2.50	9.20	5.74	0.36	2.96	5.87	0.43	2.57	4.01%	3.76%	PASS
IDDRUN_64MHz_VDD_HV	mA	NA	125.00	12.90	0.38	97.22	12.66	0.38	98.77	NA	-0.21%	PASS
IDDRUN_64MHz_VDD_BV	mA	NA	125.00	63.64	0.68	30.20	63.38	0.65	31.64	NA	-0.42%	PASS
IDDRUN_64MHz_HVADC	mA	NA	125.00	5.93	0.24	163.85	5.89	0.19	208.16	NA	-0.03%	PASS
IDDSTDBY2_VDD_HV	uA	NA	100.00	6.93	0.34	90.42	6.59	0.61	51.20	NA	-0.37%	PASS
IDDSTDBY2_VDD_BV	uA	NA	100.00	3.80	0.32	101.56	4.10	0.26	122.06	NA	0.31%	PASS
IDDSTOP_BV	uA	NA	900.00	46.26	6.82	41.76	52.27	4.39	64.43	NA	0.70%	PASS
IDDSTOP_HV	uA	NA	900.00	8.88	0.48	617.35	8.64	0.86	346.42	NA	-0.03%	PASS

IIWPDI_VIH_5V5	PAD_70 & PAD_72: lowest Cpk & largest shift among 58 pins											
PAD_70	uA	10.00	250.00	79.39	1.36	17.06	84.23	1.51	16.41	6.97%	2.84%	PASS
PAD_72	uA	10.00	250.00	78.36	1.28	17.79	83.37	1.31	18.60	7.32%	2.92%	PASS
IIWPUI_VIH_5V5	PAD_6 & PAD_70: lowest Cpk & largest shift among 58 pins											
PAD_6	uA	10.00	250.00	49.68	0.47	28.05	52.41	0.72	19.51	6.88%	1.36%	PASS
PAD_70	uA	10.00	250.00	47.31	0.42	29.30	48.35	0.72	17.70	2.79%	0.51%	PASS
IIWPDI_VIH_3V3	PAD_67 & PAD_70: lowest Cpk & largest shift among 58 pins											
PAD_67	uA	10.00	150.00	39.17	0.85	11.43	40.76	0.87	11.73	5.45%	1.43%	PASS
PAD_70	uA	10.00	150.00	39.49	0.90	10.96	41.12	0.92	11.22	5.50%	1.47%	PASS
IIWPUI_VIH_3V3	PAD_70 & PAD_75: lowest Cpk & largest shift among 58 pins											
PAD_70	uA	10.00	150.00	28.09	0.38	15.82	28.88	0.64	9.87	4.38%	0.65%	PASS
PAD_75	uA	10.00	150.00	29.06	0.50	12.66	30.47	0.60	11.35	7.43%	1.17%	PASS
ILKG_H_Even	PAD_38 & PAD_49: lowest Cpk & largest shift among 39 pins											
PAD_38	nA	NA	200.00	0.67	1.39	47.93	0.34	1.75	38.13	NA	-0.17%	PASS
PAD_49	nA	NA	200.00	0.13	0.95	69.92	0.90	0.54	123.12	NA	0.39%	PASS
ILKG_L_Even	PAD_38 & PAD_11: lowest Cpk & largest shift among 39 pins											
PAD_38	nA	NA	200.00	0.24	0.37	180.13	0.05	0.63	105.53	NA	-0.09%	PASS
PAD_11	nA	NA	200.00	0.03	0.31	216.54	0.30	0.43	156.38	NA	0.13%	PASS
ILKG_H_Odd	PAD_48 & PAD_50: lowest Cpk & largest shift among 37 pins											
PAD_48	nA	NA	200.00	0.49	1.69	39.44	0.71	0.47	141.52	NA	0.11%	PASS
PAD_50	nA	NA	200.00	0.10	1.28	51.95	0.64	0.84	78.73	NA	0.27%	PASS

ILKG_L_Odd	PAD_48 & PAD_21: lowest Cpk & largest shift among 37 pins											
PAD_48	nA	NA	200.00	0.13	0.38	175.44	0.54	0.38	173.96	NA	0.21%	PASS
PAD_21	nA	NA	200.00	0.16	0.37	180.67	0.17	0.57	117.89	NA	0.01%	PASS
ILKG_H_PAD_33	nA	NA	200.00	0.46	0.82	81.10	0.17	0.37	179.94	NA	-0.14%	PASS
ILKG_L_PAD_33	nA	NA	200.00	0.04	0.42	157.75	0.12	0.32	206.55	NA	0.04%	PASS
ILKG_H_Vpp	nA	NA	200.00	6.04	9.54	6.78	4.43	4.64	14.05	NA	-0.83%	PASS
ILKG_L_Vpp	nA	NA	200.00	0.45	5.66	11.75	0.62	2.73	24.32	NA	0.08%	PASS
VLPREG_PAD 14	V	1.15	1.32	1.21	0.01	3.75	1.21	0.01	2.74	0.32%	0.19%	PASS
VLPREG_PAD 43	V	1.15	1.32	1.21	0.01	3.71	1.21	0.01	3.31	-3.42%	-2.07%	PASS
VLVDLVBKPL	V	1.08	1.16	1.10	0.004	1.76	1.10	0.004	1.84	-8.36%	-3.01%	PASS
VLVDLVCORL	V	1.08	1.16	1.10	0.004	2.01	1.10	0.004	1.72	-8.01%	-2.91%	PASS
VMREG_PAD 14	V	1.16	1.32	1.22	0.01	2.20	1.22	0.01	1.91	-3.80%	-2.53%	PASS
VMREG_PAD 43	V	1.16	1.32	1.22	0.01	2.18	1.22	0.01	1.96	-7.49%	-5.05%	PASS
VOH	PAD_33: lowest Cpk & largest shift among 60 pins											
PAD_33	V	4.00	NA	5.40	0.01	37.29	5.41	0.01	41.69	0.36%	NA	PASS
PAD_33	V	4.00	NA	5.22	0.05	8.76	5.26	0.04	9.90	3.16%	NA	PASS
VOL	PAD_33: lowest Cpk & largest shift among 61 pins											
PAD_33	uA	NA	0.5	0.219	0.025	3.69	0.243	0.027	3.13	NA	8.35%	PASS

"Shift analysis" refers to analysis of shift of the distribution mean towards the nearest specification limit:
"% Shift (USL) = {Mean(new)-Mean(old)} / {Upper Spec Limit-Mean(old)}
% Shift (LSL) = {Mean(new)-Mean(old)} / {Mean(old)-Lower Spec Limit}

4.2. Summary:

From the above data, it was verified that the requirements and acceptance criteria was achieved.

5. Document History:

Rev	Date	Originator
O	1st Oct 2013	Chew Kim Seong

Appendix A: Justifications for any Shifts > 15%

Not applicable as no parameter shift > 15%.