AEC-Q100G Qualification Results

STRESS TEST Reference Test Conditions End Point

HTOL

UHST

ELFR

HTSL

THB

WBS

WBP

EDR

THB = 85°C/85%RH for 1008 hrs.

PC before THB (for SMDs only): Required

THB = Max Vdd

Bias = Max Vdd

AEC Ta = 125°C for 1008 hrs.

Timed RO = 96 hrs. MAX

Preconditioning (PC) : Required

Solderability (SD):

For AEC only: WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.

TEST GROUP A - ACCELERATED ENVIRONMENTAL STRESS TESTS

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Remarks</th>
<th>Lot ID -(#Rej/SS)</th>
<th>Customer Approval</th>
<th>Comments or Generic Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTSL</td>
<td>A103</td>
<td>High Temperature Storage Life (HTSL): 150°C for 1008 hrs.</td>
<td>Timed RO; not applicable</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
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<tr>
<td>HTSL</td>
<td>A104</td>
<td>High Temperature Operating Life (HTOL): AEC Ta = 150°C for 1008 hrs.</td>
<td>Test @ RHC 77 0 0 Not required</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
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<td></td>
</tr>
<tr>
<td>HTOL</td>
<td>A105</td>
<td>High Temperature Thermal Storage Life (HSTSL):</td>
<td>Test @ H 77 1 77 Lot A: 0/77</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
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</tr>
<tr>
<td>ELIR</td>
<td>A106</td>
<td>High Life Fatigue Rate (ELIR): AEC Ta = 125°C for all tests</td>
<td>Test @ RH 77 1 77 Lot A: 0/77</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
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<tr>
<td>EDIR</td>
<td>A107</td>
<td>NVM Endurance, Data Retention, and Operational Life (EDIR): AEC Ta = 70°C for 1000 hrs.</td>
<td>Test @ RC 77 1 77 Lot A: 0/77</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
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TEST GROUP B - ACCELERATED LIFETIME SIMULATION TESTS

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Remarks</th>
<th>Lot ID -(#Rej/SS)</th>
<th>Customer Approval</th>
<th>Comments or Generic Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>WBS</td>
<td>A108</td>
<td>Wire Bond shear (WBS)</td>
<td>Test @ R 77 0 0 Not required</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
<td></td>
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<tr>
<td>WBP</td>
<td>A109</td>
<td>Wire Bond Pull (WBP)</td>
<td>Test @ RC 77 1 77 Lot A: 0/231</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
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<tr>
<td>SD</td>
<td>A110</td>
<td>Wire bond resistance (SD)</td>
<td>Test @ RC 77 1 77 Lot A: 0/231</td>
<td>0.03 grams</td>
<td>Not Applicable</td>
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<tr>
<td>PD</td>
<td>A111</td>
<td>Package Defectivity (PD)</td>
<td>Test @ R 77 0 0 Not required</td>
<td>5 units</td>
<td>0</td>
<td>Not required</td>
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</table>

TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>End Point Requirements</th>
<th>Minimum Sample Size</th>
<th># of Lots</th>
<th>Total Units including spares</th>
<th>Remarks</th>
<th>Lot ID -(#Rej/SS)</th>
<th>Customer Approval</th>
<th>Comments or Generic Data</th>
</tr>
</thead>
</table>

Note: All surface mount devices prior to THB, HAST, AC, and ELIR, WBP after TC on 5 devices from 1 lot; 2 bonds per corner and one mid-bond per side on each device. Record which pins were used.

This testing is performed by Freescale Reliability Lab (KLM) unless otherwise noted in the Comments.

TESTS HIGHLIGHTED IN YELLOW WILL BE PERFORMED FOR THIS STUDY
### Test Group D - Die Fabrication Reliability Tests

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Conditions</th>
<th>Goal Points Requirements</th>
<th>Minimum Sample Size</th>
<th>% of Lots</th>
<th>Total Units Screening Spares</th>
<th>Results (Lot)</th>
<th>NA/FSL-ATMC/M09S/C90FG FAILS</th>
<th>Comments</th>
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</thead>
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<td>BOM: Approved</td>
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### Test Group E - Electrical Verification Tests

<table>
<thead>
<tr>
<th>Stress Test</th>
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<th>% of Lots</th>
<th>Total Units Screening Spares</th>
<th>Results (Lot)</th>
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### Electrical Distribution (ED)

- **Electro-Thermally Induced Gate Leakage (GL):**
  - Performs on all solder ball mounted packages e.g. PBGA, Chip Scale, Micro Solder Ball BGA, Flip Chip.
- **Latch-up (LU):**
  - Tests performed on lead frame and leadless packages.
- **Electro-Thermally Induced Gate Leakage (GL):**
  - Tests performed on lead frame and leadless packages.
- **Electro-Thermally Induced Gate Leakage (GL):**
  - Tests performed on lead frame and leadless packages.
- **Electro-Thermally Induced Gate Leakage (GL):**
  - Tests performed on lead frame and leadless packages.

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### Quality Assurance (QA)

- **Data/Quality Assurance (QA):**
  - Performs all QA activities on all qualified units.
- **Data/Quality Assurance (QA):**
  - Performs all QA activities on all qualified units.
- **Data/Quality Assurance (QA):**
  - Performs all QA activities on all qualified units.
- **Data/Quality Assurance (QA):**
  - Performs all QA activities on all qualified units.

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### Physical Information

- **FAB Mask Set/Part:**
  - Physical Information/Part Number (a)
  - Die Area (mm²)
  - Assembly
  - Package (Code)
  - Site Black
  - Wire Compound
  - Wire Description
- **Product Information:**
  - FAB Mask Set/Part
  - Product-Test Description/Part Number (a)
  - Die Area (mm²)
  - Assembly
  - Package (Code)
  - Site Black
  - Wire Compound
  - Wire Description